High-Pass Sigma-Delta Modulator

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Abstract

This paper presents a circuit including a high-pass ΣΔ modulator implemented in CMOS process and a time-interleaved high-pass ΣΔ analog to digital converter.

1. Introduction

Primarily because of advances in VLSI technologies, ADCs based on oversampling and sigma-delta (ΣΔ) modulation have become more and more attractive in applications requiring high resolution. Their popularity derives from their high dynamic, high linearity and their reduced analog processing and relaxed sensitivity to analog circuit errors [1]. The high-pass (HP) ΣΔ modulator is based on the same principle as the conventional ΣΔ modulator, i.e. the quantization noise is shaped away from the signal band by a loop filter. The first difference is the position of the signal band, that is now located at $f_s/2$, where f_s is the sampling frequency, compared with a pass-band at dc for the low-pass ΣΔ modulator. The second is that the HP ΣΔ modulator has a zero of the noise transfer function (NTF) at $f_s/2$. Those differences make the HP ΣΔ modulator completely immune to low frequency noise [2]. We note also that the band-pass ΣΔ modulator reduce also low-frequency noise, however the second-order structure band-pass ΣΔ modulator achieves only the first-order quantization noise shaping, whereas the second-order high-pass ΣΔ modulator achieves the second-order shaped noise.
The HP ΣΔ modulator can be used as a standalone modulator using the chopper-stabilized technique well suited to a low frequency small signal application [3]. Furthermore, it is very promising and beneficial in a time-interleaved ΣΔ converter, provided that the number of channels is even [4]. Finally, HP ΣΔ modulator is a promising solution for direct radio frequency sampling receiver.

2. Circuit presentation

The circuit presented in this paper includes a second order HP ΣΔ modulator implemented in CMOS process. More detail is presented in [3]. The block diagram of the modulator is illustrated in Figure 1. The second part of the circuit is a two channel time-interleaved HP ΣΔ converter [4]. The photomicrograph of the chip is presented on the left side of the Figure 1.

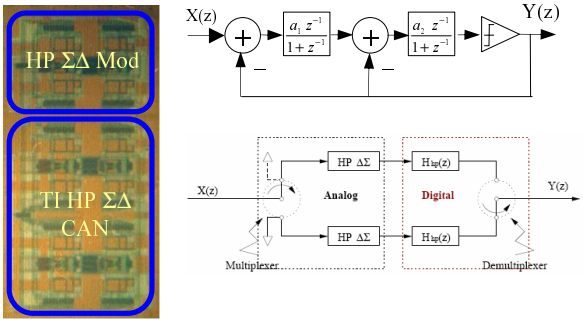

Figure 1: Photomicrograph of the chip on the left and on the right, the block diagram of the second order HP ΣΔ modulator and the time-interleaved HP ΔΣ converter.

3. Test setup and measurement results

The device under test is packaged in a 44-pin, J-leaded chip carriers. The test setup is presented in Figure 2. The most important test is the test of functionality of the high-pass modulator before measuring its performance and its advantages in the time-interleaved converter. The supply voltages are generated from the voltage regulator MC33275. Various regulated voltages shown in Figure 2 are generated through terminal adjustable regulators LM317L. The impulse generator makes it possible to have a clock signal for the circuit. The differential input is generated from waveform generator AWG 2021 by granting its two outputs in opposition of phase. The test of a ΣΔ modulator has to be proceeded in two steps: the static test and the dynamic test. The first test consists of verifying the right operation of bias circuit in assuring the transistors operating in the saturation mode. The expected consumption of a high-pass second-order ΣΔ modulator is 42 mW. The total power consumption of the chip is 83 mW. The second test is to measure the dynamic performances of the modulator. The output is measured through the logic analyzer HP 16500 B. The resulting data from the logic analyzer is transferred to PC and processed through MATLAB tool. These treatments will allow obtaining the spectrum of the output signal. A MATLAB program calculates the SNDR and SNR of the modulator. The measurement is taken while varying the amplitude of the input signal. This enables us to plot SNDR curves with the presence of the noise and harmonic distortion. Then, with a program developed in MATLAB, we can remove the

harmonics and we have the curve of the SNR as a function of the input signal amplitude. To verify the immunity of the high-pass modulator from low frequency noise, an offset or a low frequency noise source is added to one of the two reference voltages V_{+ref} or V_{-ref}, which are the output value of the DAC in the feedback of the modulator.

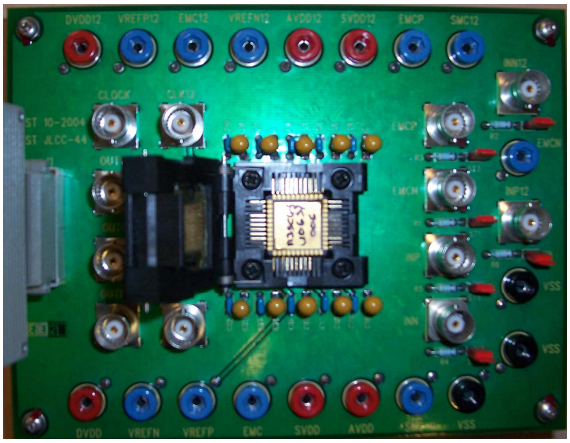

Figure 2: Test setup

The output of the time-interleaved high-pass converter is measured in the same manner. The output of each modulator is measured through the logic analyzer HP 16500 B. The resulting data is transferred to PC. It will be filtered by an optimal channel filter through a programme in MATLAB and demultiplexed to produce the final output signal. By this way, the performance of the converter is studied. The most important test is the immunity from channel offset. Undesired tones due to channel offset are completely drowned in the quantization noise.

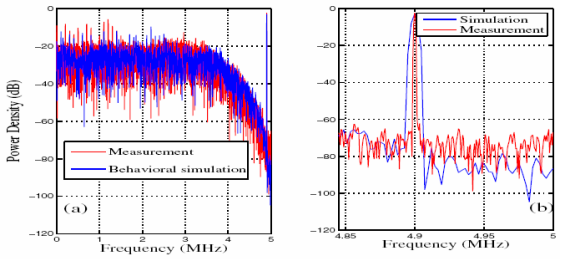

Figure 3: Measured vs. Simulated power spectral density of the HP ΣΔ modulator output.

Figure 3 shows the power spectral density of HP ΣΔ modulator output with a 4.9 MHz input signal and a 10 MHz sampling rate. Table 1 summarizes the measured performance of the second-order HP ΣΔ modulator. This performance is equivalent to that of conventional modulator with the advantage of immunity to low frequency noise.

Technology	0.35 µm CMOS process
Sampling Frequency	10 Mhz
OSR	32
Maximum SNDR	53 dB
Dynamique Range	59 dB
Size	0,9 mm²
Consumption power	42 mW

Table 1: Summery of the measured performance of the second order HP ΣΔ modulator

4. Conclusion

This paper illustrates the validation of the HP ΣΔ modulator concept and presents a second order HP ΣΔ modulator and its advantage over low-pass ΣΔ modulator. The high-pass ΣΔ modulator is a new concept of ΣΔ modulator with the advantage of immunity to low frequency noise and DC offset. This new kind of ΔΣ modulator is an interesting and promising solution for applications requiring high resolution and wide bandwidth. The idea in this concept is to use the time-interleaving to widen the conversion bandwidth, the ΣΔ modulation to have a high resolution and high-pass modulator (instead of low-pass modulator) to minimize the channel mismatch in the parallel architecture. The main objective of this circuit is to demonstrate the high-pass ΣΔ modulator and its advantage over the conventional ΣΔ modulator.
The measurement performance of the circuit is very good and in a complete agreement with simulation performance. The second-order high-pass ΣΔ modulator achieves a 59dB dynamic range with a 32 times oversampling ratio at 10 MHz sampling frequency.

5. References

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[2] V. T. Nguyen, "High-Pass ΔΣ Modulator and its Application to Time-Interleaved ΔΣ Converter", *Ecole Nationale Supérieur des télécommunications, PhD Dissertation*, 2004.
[3] V.T. Nguyen, J-F. Naviner and P. Loumeau, "High-Pass DS Modulator : from System Analysis to Circuit Design", pages 5379-5382, *Proc. of ISCAS 2006*.
[4] V.T. Nguyen, J-F. Naviner and P. Loumeau, "A CMOS implementation of time-interleaved high-pass ΔΣ modulator", pages 5387-5390, *Proc. of ISCAS 2006*.