Data Converter BIST Development Tools

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Abstract

Two tools are presented to support the design of MS-BIST solutions. A tool to generate the digital part of a BIST set-up for DACs in VHDL code and an analogue signal generator based on ΣΔ modulation.

1. Introduction

In this project, considerations were given to the development of evaluation systems to support the development and deployment of BIST circuit implementations for data converters, primarily Digital to Analogue Converters (DACs) [1-3]. Mixed-Signal Integrated Circuit (MS-IC) test remains a major problem in the microelectronics arena with the ever-increasing need for higher circuit design performance and lower product costs. The requirement is for the adoption of ever more sophisticated test methods to meet the design performance and cost reduction challenges. Design for Testability (DfT) and Built-In Self-Test (BIST) techniques have been successfully developed and demonstrated over the last few years for a number of specific circuit designs. In consideration of data converter DfT and BIST, a range of analogue and digital design parameters in nature, need to be determined through suitable on-chip circuitry that can support and/or replace specific ATE (Automatic Test Equipment) functions. Whilst the solutions identified have been suited for such targeted case studies, the need to adopt a more generic approach, similar to the techniques adopted in the digital logic and memory domains, requires serious consideration.

Two EDA (Electronic Design Automation) tools developed will be demonstrated in order to provide a means to support the design and integration of Mixed-Signal BIST (MS-BIST) solutions. Firstly, a software tool to generate the digital part of a BIST architecture for Digital to Analogue Converters (DACs) in RTL level VHDL code will be presented. The second, a hardware-software analogue signal generator based on memory-based techniques using sigma-delta modulation will be presented.

The following two EDA tools have been developed in order to support the design and integration of Mixed-Signal BIST solutions in both discrete systems and potential SoC (System on a Chip) integration:

DAC-BIST Generator – A PC based EDA tool for allowing the creation of synthesisable VHDL code for Digital to Analogue Converter (DAC) BIST.

Memory Based Analogue Test Stimulus Generator – A PC based EDA tool and supporting development hardware for creating and implementing Sigma-Delta (ΣΔ) bit-streams targeting Analogue to Digital Converter (ADC) BIST.

2. DAC-BIST Generator

This purpose of this system is to support the generation of synthesisable VHDL code in order to implement the digital part of a BIST solution for DAC designs. The user will set specific design parameters to form the final VHDL code model that can target both programmable logic and ASIC technologies. The final system will be formed with a predefined communications protocol, allowing for an attached circuit to communicate with the BIST. The basic arrangement is shown in *figure 1*. This is supported through a software application that allows a developer to enter their particular requirements that are then mapped onto the DAC-BIST architecture. Currently, the system is considered to develop RTL level VHDL code that can be synthesised for programmable logic or an ASIC implementation. The system is set-up so that the digital core interfaces to the external communications port (digital I/O) of commercially available DACs, where the internal architecture of the DAC is unknown and access is via the existing DAC interface. Consideration also needs to be given to an embedded BIST within the DAC package itself. The approach does not allow for all possible data converter parameters to be determined, but targets specific operations as a step in the direction of attempting to realise a full-BIST approach.

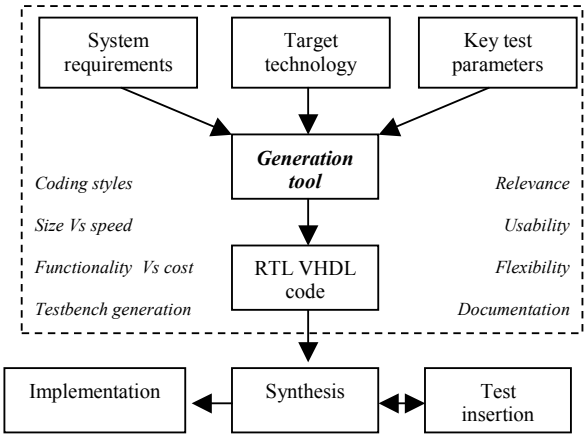

Figure 1: DAC-BIST design overview

3. ΣΔ Based Analogue Stimulus Generator

This system was developed to support the enhancement and development of memory based analogue test stimulus generation that could form part of a BIST solution for Mixed-Signal ICs. To provide maximum benefit to the development process, both simulation studies and hardware realisations need to be considered and integrated into a single platform. This system allows for a high-level behavioural model simulation be compared to an analogue circuit simulation model and a hardware implementation.

The system uses the memory based signal generation technique [4-7] in order to create a required analogue signal waveform. In memory based analogue signal generation, an analogue signal is encoded into a Pulse Density Modulated (PDM) bit-stream pattern using Sigma-Delta (ΣΔ) modulation techniques. This bit-stream pattern, containing a periodic cycle of the analogue input signal, is downloaded to memory on the hardware. The bit-stream pattern is continuously read and applied to a DAC. The output of the DAC is then passed through an analogue filter, which removes the quantization noise, in order to produce the final analogue test stimulus.

In order to develop the analogue signal generator using ΣΔ modulation techniques, there is a need to understand and utilise a number of design tools, both at the system level and at the circuit level. To utilise the ΣΔ modulation techniques and become familiar with the design issues from the algorithm through to the circuit implementation level, an evaluation system, based on a hardware-software system as shown in *figure 2*, was developed. This system allows for a higher-level behavioural model simulation be compared to an analogue circuit simulation model and a hardware implementation. The system is based on MATLAB®, SIMULINK®, and HSPICE® modelling, simulation and hardware implementation. A software user interface allows the user to undertake the following key tasks:

- develop a ΣΔ modulator model to encode an analogue signal into a PDM bit-stream pattern.
- perform MATLAB® and HSPICE® analysis of the PDM pattern.
- select a bit-stream pattern based on a given optimisation criteria (SNR/ SFDR).
- download the selected pattern to memory on the evaluation hardware for analysis.

4. Conclusion

In this project, considerations were given to the development of evaluation systems to support the development and deployment of BIST circuit implementations for digital to analogue converters. One aspect has developed an automatic RTL level VHDL code generator for the digital part of a DAC-BIST structure. The second aspect developed a system based on ΣΔ modulation techniques for analogue test stimulus generation. These are based around the development and utilisation of hardware-software evaluation systems, identifying both simulation and physical hardware issues and operation.

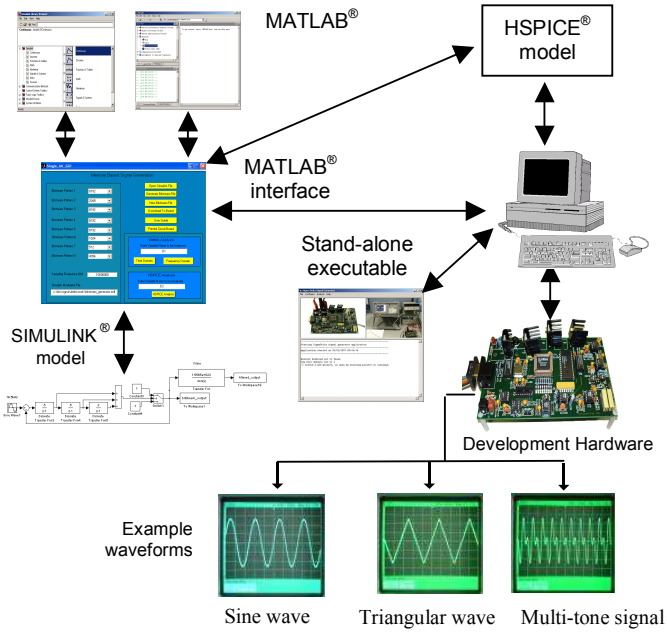

Figure 2: Overview of the ΣΔ evaluation system

5. References

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Acknowledgement

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