# The VISION Project: SysXplorer (FZI)

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## Abstract

*In the automotive area as well as in the area of mobile communications, the ability to integrate a multitude of new functions in a distributed system scenario has become a condition for market survival. And this – naturally – without a decrease in productivity, while keeping in mind high safety and quality requirements as well as commercial aspects. The research of a cross-domain design methodology for distributed microelectronic systems while considering complex environmental conditions and more efficient application-specific design processes is therefore the goal of VISION.*

## 1. VISION Project

VISION addresses the design of networked microelectronic systems in the areas of automotive electronics and mobile communications. For the first time, the project supplies an integrated view of networked systems that are already in early design phases. This will allow it to master the new requirements listed in the markets named successfully. Consideration of system integration at the beginning of the design process will result in the discovery of integration errors in the specification phase. This will lead to a strong increase in productivity as well as the ability to significantly improve the methodical design of highly-networked microelectronic systems in the future in the extremely important discipline of system integration in Germany. Since system integration in the automotive and telecommunication sector possesses a very high share in the value chain, direct positive microeconomic and macroeconomic effects are obvious.

The Project will present the latest results of the Research Activities of its Partners.

The project partner FZI presents the SystemC-based architectural exploration framework SysXplorer which provides formal performance and communication analysis of a given SystemC design with respect to an underlying target platform. SysXplorer can be used to detect bottlenecks, deadlocks data losses, and access conflicts on communication resources as well as the calculation of worst case/best case response time of an entire system without needing testbenches. Based on analysis results, the tool performs automated bus allocation and binding to guarantee conflict-free bus accesses.