FAUST, an Asynchronous Network-on-Chip based Architecture for Telecom Applications

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Abstract

We present the FAUST chip (20 NoC nodes and units in a 130µm technology) and the FAUST platform addressing Telecom applications. The demo shows the feasibility of a complex GALS NoC architecture.

1. Introduction

With many tens of million transistors available on a single chip, the era of System-on-Chip has become a reality. Design and IP reuse is mandatory : chips integrate processor cores, DSPs, on-chip memories, IP-blocks, etc… A globally shared bus cannot meet the increasing demands of System-on-Chip interconnects, because the long-wire loads and resistances result in slow signal propagation. Alternative synchronous solutions, such as bus hierarchy, crossbars, still face the same issues : difficulties in timing validation and in connecting blocks running at different speeds, limited throughput versus power efficiency.

On the other hand, the advantages of "Network-on-Chip" (NoC) are numerous : high scalability and versatility, high throughput with good power efficiency. By separating communications from computations, NoC based architecture and packet switching provides dynamic communication possibilities. For very large scale integration, NoC are fully scalable because the number of nodes can be increased to provide higher global throughput, without degrading local network link performances, while the dissipated power is reduced to only active NoC links.

The NoC distributed communication architecture is perfectly adapted to the Globally Asynchronous Locally Synchronous (GALS) paradigm where the NoC nodes and links are implemented using asynchronous logic while the NoC functional units are implemented with standard synchronous design methodologies [1,6,7].

2. An Asynchronous NOC protocol

We have proposed and developed ANOC, a complete Asynchronous NoC architecture adapted to GALS systems, using virtual-channels to provide low latency and Quality-of-Service (QoS), and which is implemented in Quasi-Delay-Insensitive (QDI) asynchronous logic [1].

The ANOC communication architecture is composed of nodes, links between nodes, and computation resources (Figure 1). The NoC asynchronous nodes are the basic switching elements of the network : they are responsible to handle the wormhole protocol and arbitrate between any conflicting packets. The resources built the complete system; they can be configurable hardware IP blocks (FFT, MPEG…) or generic blocks (CPU, DSP, memories…).

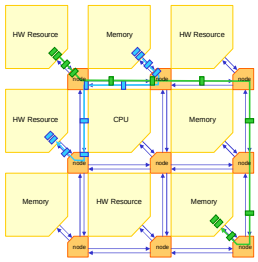

Figure 1: ANOC Architecture

To integrate any synchronous IP within ANOC architecture (Figure 2), the dedicated Network Interface performs two main tasks : the synchronization between the synchronous and asynchronous logic domains using ad-hoc decoupling FIFOs [2]; and also provides all facilities to access the NoC communication infrastructure : network routing path programming, network data packet generation, IP core configuration. The NOC synchronization scheme allows a secured integration of the IPs and eases the application programming of the final SoC [3].

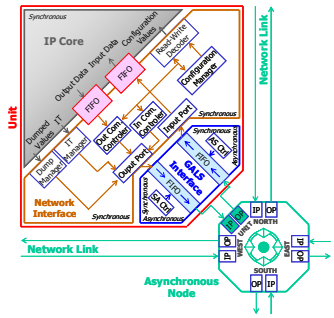

Figure 2: IP integration within ANOC Architecture

3. SystemC/TLM design Methodology

When addressing complex SoC and designing a new communication protocol such as ANOC, it is mandatory to offer to designers and architects a high level modelling strategy and all associated simulation/debug facilities. SystemC language and Transaction-Level-Modelling (TLM) methodology are good candidates for such challenges, and have been used to develop a TLM model and environment of the proposed NoC protocol [1,3].

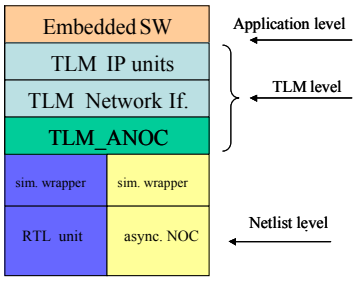

Figure 3: SystemC/TLM mixed-level framework

The environment comprises the TLM model of the NOC protocol (TLM_ANOC C++ classes), the TLM model of the Network Interface (TLM_NI C++ classes), on the top of which can be modelled any IP unit connected to the NOC. The environment can then integrate embedded SW executed on the NOC TLM platform. For low level verification, the environment allows co-simulation of HW units (either Synchronous RTL units or either the Asynchronous NoC model) within the TLM platform using simulation adapters.

4. FAUST Chip Architecture

The proposed asynchronous NoC architecture and design methodology has been successfully applied to the design of a prototype chip in a 130µm STMicroelectronics CMOS technology. The FAUST chip (Flexible Architecture of Unified System for Telecom) integrates 20 asynchronous NoC nodes, 23 synchronous units including an ARM946 core, embedded memories, various IP blocks, re-configurable data-paths engines, and one clock management unit to generate the 23 distinct unit clocks (Figure 4).

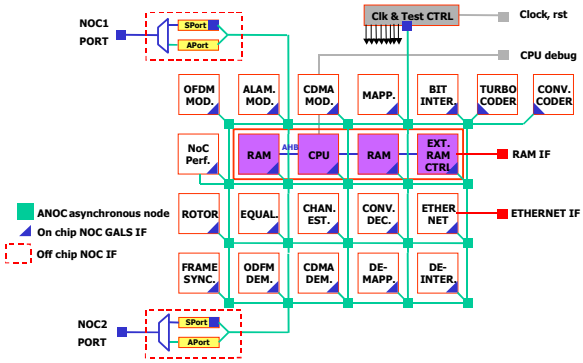

Figure 4: FAUST chip architecture

The FAUST chip [4] integrates more than 3Mgates and 3.5Mb of embedded RAM, which corresponds to a chip area of 79.5mm2. The 20-node NoC represents about 15% of the overall area and the average complexity of the 23 IP connected is close to 300Kgates. The maximum NoC throughput between 2 adjacent nodes is 5.12Gb/s per link. The synchronous unit frequencies can be programmed between 160MHz and 250MHz. In terms of power consumption, the transceiver consumes 640mW in TX mode and 760mW in RX mode, while the NoC power consumption represents only 6% of this overall consumption. Due to the 23 distinct clock domains, EMI is expected to be very low.

5. FAUST Open NoC Platform

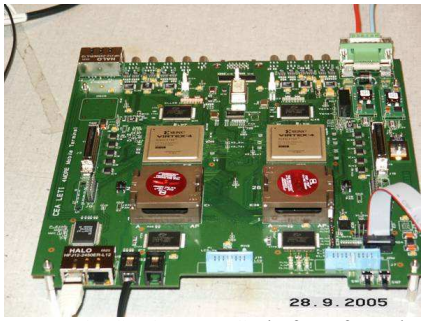

Figure 5: FAUST Open NoC Platform for Telecom

A complete FAUST prototyping platform (Figure 5) has been developed, which integrates 2 FAUST chips and 2 FPGAs connected with the same unified NoC protocol. The FAUST Open NoC Platform addresses Software-defined-Radio (SDR) applications, and currently implements a 4G Telecom MC-CDMA MIMO application (htttp://ist-4more.org) [5].

6. Conclusion

An advanced NoC protocol for GALS system has been presented and developed. The FAUST chip and prototyping platform proves that current GALS techniques are mature enough to address the design issues of today's complex SoCs, and that NoC based architecture can address throughput demanding dataflow applications. Current research aims at developing dynamic configurable mechanisms and advanced DVS/DFS low power strategies.

5. References

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