GRAPES System Explorer

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Abstract

GRAPES System Explorer (GRAPES-SE) is a design exploration framework providing at the same time modeling and optimization capabilities at the system-level

1 Introduction and motivation

The evolution of semiconductor industry makes it possible for designers to implement Multiprocessor Systems-on-Chip (MPSoCs), where multiple heterogeneous processor cores are integrated in the same chip. Due to the increasing complexity of such systems, a detailed software simulation is the easiest and cheapest way to explore design options and it is almost essential for evaluating new research ideas.

The use of C++ and SystemC [1] for hardware descriptions combined with the use of multiple cycle-based Instruction Set Simulators (ISSs) can be a viable technique to cope with the development of such complex simulators and design frameworks. This is the approach used in most of the recent MPSoC simulators and development frameworks. Although the clear progress in designing and simulating MPSoCs, these systems are evolving at a tremendous rate. Each new generation adds not only performance but also new functionalities. The time required to build a new complex simulation and design infrastructure can make the simulated architecture easily obsolete. We believe that further evolutions in the development of design and modeling framework for MPSoCs requires flexibility, scalability and modularity as well as simulation speed, accuracy and designer interaction. Although we do not pretend to be the first attempt in this direction, we strongly believe that the problem is far from being solved and it needs further investigation.

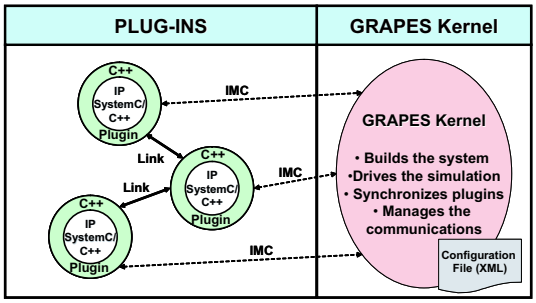

Figure 1. GRAPESim Framework

Our proposed solution to cope these problems is *GRAPES-SE* a system-level framework to model at cycle-level heterogeneous MPSoC platforms (GRAPESim) and to optimize (STShell) the system performances.

2 GRAPESim

GRAPESim is a structural modeling framework: the design can be decomposed into several modules (Plug-ins), each one corresponding to an hardware block. The GRAPES framework is composed of the GRAPES kernel and the Plug-ins (as shown in Figure 1).

A light and fast C++ kernel (GRAPES Kernel) manages the different plug-ins – wrapped C++/SystemC IPs – composing the target system. The GRAPES kernel has been designed to be relatively light-weight with respect to the SystemC kernel, to manage only the set of functionalities related to the plug-in interfaces and thus guaranteeing fast simulations. The plug-in shell has been developed in C++ and designed to wrap generic IP modules such as, ISSs, memories buses and so on. When loaded and connected together, the plug-ins create the simulated system model. The different IP system modules, wrapped

by the plug-ins, can be developed by using C++ or SystemC language and can coexist simultaneously within the framework. Plug-ins provide a standard Interface Method Calls (IMC) to support cycle-based simulation, configuration/reconfiguration and the communication with the kernel. The communication between plug-ins is implemented by using a port-based communication. The port-based communication is based on the principle that two modules communicate by exchanging data or signals, instead of calling the methods on the other modules. Each port is bidirectional, since it can be useful to describe communication protocols without using any other port description. The communication protocol is not a characteristic of the described module but only of its port. This means that the behavior of the module is decoupled from the communication description and so the redefinition of the connection between the modules or the communication protocols, requires only the redefinition of the communication part. The kernel loads and configures plug-ins as dynamic libraries realizing the binding among them. All the necessary information to perform these operations are provided by a configuration file that is parsed during the simulation boot phases. During the simulation, the kernel triggers the action for each plug-in at every clock cycle and it exchanges data (which are represented as metadata) between them using the IMC interfaces. During the simulation, the kernel annotates the execution statistics like performance of each internal module and of the overall described system.

One of the main characteristic of the approach is that it is based on a structural modeling framework. It is possible to understand how the modularity of the approach increases the reusability of the parts of a system model or an the other side to easily explore different architectural solutions only performing a plug-ins substitution. We conclude this overview focusing on an implicit aspect of this framework which is the possibility to develop, to maintain, and to compile all entities in the framework independently to each other by supporting also an easy distribution and sharing of plug-ins library, without necessarily releasing modules source code.

3 STShell

For the automatic exploration of the design alternatives, the GRAPESim can be coupled with a design environment featuring multi-objective optimization capabilities called System Tuning Shell, STShell. It uses a variety of state-of-the-art optimization techniques to explore the system configurations, ranging from gradient-based methods to genetic algorithms.

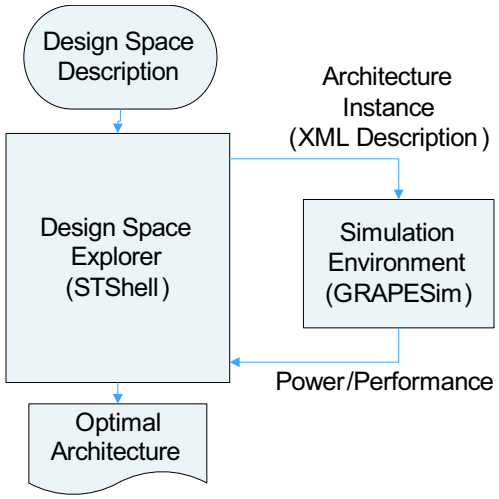

Figure 2. GRAPES-SE

As shown in Figure 2, STShell interacts externally with GRAPESim on defining the architecture instance to model and receiving the performance results. This enables the automatic exploration and optimization of the architecture design space given as input to STShell.

4 Conclusions

This short overview presents GRAPES-SE, our proposed solution to cope with modeling, simulation and exploration challenges for MPSoC systems. The framework is based on modular interfaces and a dynamic library-based approach to increase flexibility and scalability from the modeling point of view and an automatic system explorer for the optimization step.

The GRAPES-SE has been recently used to model and optimize complex MPSoCs based on Network on-Chip and shared memories [3, 2]. GRAPES kernel source code as well as some examples of plug-ins can be free downloaded on the web at `http://savane.elet.polimi.it/grapes`.

References

[1] *SystemC 2.0 User's Guide*. 2002.

[2] M. Monchiero, G. Palermo, C. Silvano, and O. Villa. Efficient synchronization for embedded on-chip multiprocessors. *IEEE Transactions on VLSI Systems*, 14(10), 2006.

[3] M. Monchiero, G. Palermo, C. Silvano, and O. Villa. Exploration of distributed shared memory architectures for noc-based multiprocessors. *Journal of System Architectures*, 24(3), 2007.