MORPHEUS
Multi-purpOse dynamically Reconfigurable Platform for intensive HEterogeneoUS processing

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Abstract

The European MORPHEUS project (IST 027342) addresses a technology breakthrough for embedded computing by developing a reconfigurable platform and the corresponding toolset.

1. Introduction

MORPHEUS [1] copes with the challenges of rising complexity and the enlarging design productivity gap by developing a global solution based on a modular heterogeneous System-on-Chip (SoC) platform providing the disruptive technology of dynamically reconfigurable computing including completed by a software oriented design flow and a consistent toolset (see [5]). MORPHEUS strives to establish the European foundation for a new concept of flexible "domain focused platforms", which are positioned between general purpose flexible HW and general purpose processors, and provide breakthroughs in performance and cost-effectiveness for embedded computing systems. This three-year project will finally provide a modular silicon demonstrator in 90nm technology composed of complementary run-time reconfigurable building blocks on which four complementary test-cases will be mapped.

2. Toolset

MORPHEUS tools are organized in three main parts.
"*Retargetable compilation"* deals with the compilation of the highest level C program including calls of accelerated operations and optimising the scheduling of the configuration of these operations at design time
"*Dynamic control design"* optimizes the scheduling of the calls at run-time.
"*Spatial design"* manages data remapping between main and local memories. It promotes standardized, open formats to express input code, and output circuits after synthesis. Specification associates SPEAR framework with C code, plus formal methods to enhance and ease validation aspects.
The tools are available for presentation as well as the plans for an integrated MORPHEUS toolset

3. Architecture

The MORPHEUS architecture is a SoC containing an ARM9 controller and different heterogeneous reconfigurable engines (HRE) for data processing. Communication is performed via a flexible interconnect structure based on a Network-on-Chip topology. Further, a predictive configuration manager will minimize the configuration overhead. Three reconfigurable engines, namely M2000's FlexEOS [2] embedded FPGA, ST-ARCES' PiCoGA-III [3], PACT's XPP [4] array provide different computational granularities, which are required to support heterogeneous applications.
To allow early evaluation and platform monitoring, a common simulation environment integrating proprietary HRE tools with a SystemC/LISATek CoWare infrastructure has been developed by STM. It will be presented as basis for the final silicon implementation in STM CMOS 90nm technology.

4. Applications and Demonstrators

The suitability and the efficiency of the final MORPHEUS platform will be validated by a set of four complementary test cases:
(1) Mobile broadband wireless access, based on the emerging IEEE 802.16j standard, (2) network routing, (3) image (pre-)processing and compression of HD video/digital film and (4) intelligent cameras, i.e. systems able to interpret information from a flow of images.
Test platforms of application partners based on components of the shelf (COTS) as microprocessors, FPGAs are intended to be a state-of-the-art benchmark and reference for the final MORPHEUS platform. These platforms and their capabilities can be demonstrated.

5. Conclusion

Within the MORPHEUS project, partners from academia (Univ. Karlsruhe, Univ. di Bologna, Univ. de Bretagne Occidentale, TU Delft, TU Braunschweig, Univ. Chemnitz) and industry (TRT, DTB, Lucent, TOSA, ICOM, ST, PACT, M2000, CEA, ACE, Critical Blue,) work in tight cooperation to meet the final project goals, which are a scalable reconfigurable SoC platform and the corresponding toolset supporting the rapid implementation of algorithms of the targeted application domains. The contribution will be organized by ITIV, University of Karlsruhe and academic partners. Also, all other partners will actively support the booth for date 2007.

6. References

[1] www.MORPHEUS-IST.org
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[4] www.pactxpp.com
[5] J. Becker, R. Hartenstein: Configware and Morphware going Mainstream; Journal of Systems Architecture JSA 49(2003) 127-142, (Special Issue Reconfigurable Systems), Elsevier, October 2003