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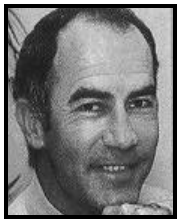

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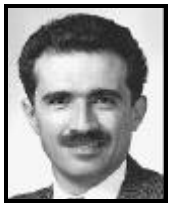

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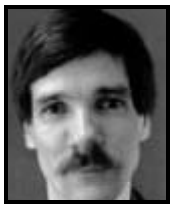

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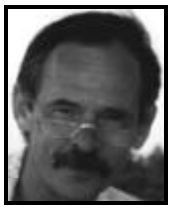

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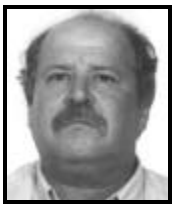

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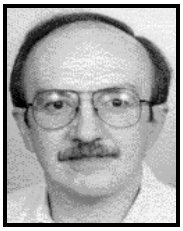

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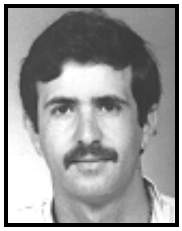

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Welcome to Date 2003

On behalf of the Executive and Technical Program Committees, we take great pleasure in welcoming you to Munich and to **DATE 03**, the single, most comprehensive European Conference and Exhibition event bringing together academic researchers, industry specialists, users and vendors in the fields of Design, Automation and Test of electronic circuits and systems.

The endless quest for faster, cheaper, smaller electronic products, particularly for the growing consumer and communications markets, dictate that increasingly complex designs be generated in continuously shrinking time scales. Design automation is a strategic technology for modern electronic systems, from simple ASICs via embedded IP cores to large systems on chip made of heterogeneous processors communicating via on-chip networks. The use of embedded processors in SoCs requires an ever-increasing emphasis on embedded software development techniques as part of the design process of state-of-the-art electronic systems. Testing of these complex electronic systems remains a challenge.

DATE has become the pre-eminent European conference addressing research and development activities in the field of design technology. World leading companies in multimedia, wireless communications, and automotive industries have led to the emergence of recognised European specialities in Embedded Systems as well as Intellectual Property and System-on-Chip Technologies, particularly with a strong mixed-signal content. These are three of the most important driving forces behind the explosive growth of Information Technology and the main contributors to accelerate the pace of electronic integration allowing complex systems to be built into a single chip. **DATE** is a unique event where the latest scientific and technological developments are brought to the public from the leading players in the field. **DATE**, therefore, offers a once-in-a-year occasion to find out more about the technical and architectural trends of circuits and systems, small and large, and the design, automation and test challenges they bring to tool vendors and PCB companies as well as semiconductor and IP providers alike.

A total of 590 submissions were received for **DATE 03**, a close to 10 percent increase over the previous edition. After careful consideration, the Program Committee has selected 98 papers for long presentations, 54 papers for short presentations and 49 papers for presentation as posters. An additional 36 papers will be presented in the Designers' Forum, a technical program track devoted to the presentation and discussion of practical, industry-oriented design experiences and methodologies using state of the art design tools. New at **DATE 03** is the Embedded Software Forum, a technical program track covering the 3 days of the conference, dedicated to all aspects of embedded software. Last but not least, 12 Special Sessions have been chosen to bring stimulating insights and vibrant discussions in state-of-the-art topics.

Another innovation is the **DATE** Focus on Business and Industry, a presentation theatre located on the exhibition floor, offering exhibition visitors and conference delegates a fresh view on some key technical and non-technical issues in the current electronic systems design market. In complement to the main technical and scientific program, we have designed a number of valuable education activities in the days before and after the conference. These are the Pre-Conference Tutorials on Monday and two full day Master Courses on Friday. The organization of many Hands-on-Tutorials, a PCB Symposium, a University Booth, fringe meetings, and social events offer a wide variety of extra opportunities to meet and exchange information on relevant issues for the design, automation and test communities.

Many volunteers have given their best efforts to make this Conference and Exhibition an outstanding event. We would like to thank all the members of the Sponsors Committee, the Executive Committee, the Program Committee, the Vendors Committee and the Exhibitors, as well as all the Authors, Speakers, Session Organizers, Session Chairs, and Reviewers for their continued interest, energy and support to **DATE**. We hope that you will enjoy the **DATE 03** Conference and Exhibition as much as all of us have enjoyed organising it for you.

Diederik Verkest, General Chairman
Norbert Wehn, Program Chairman

Best Paper Awards

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the most outstanding papers of the previous year's conference. The selection is performed by an award committee, based on the results of the reviewing process, the quality of the final paper and the quality of the presentation.

The paper selected as the most outstanding in the field of CAD (track A) is:

Analysis of Nonlinearities in RF Front End Architectures Using a Modified Volterra Series Approach

by Michaël Goffioul, Piet Wambacq, Gerd Vandersteen and Stéphane Donnay of IMEC, Belgium

The paper selected as the most outstanding in the field of Tools (track B) is:

Using Problem Symmetry in Search Based Satisfiability Algorithms

by Evgueni I. Goldberg of Cadence Berkeley Labs., USA
Mukul R. Prasad of Fujitsu Labs of America, USA
Robert K. Brayton of UC Berkeley, USA

The paper selected as the most outstanding in the field of Test (track C) is:

Reducing Test Application Time through Test Data Mutation Encoding

by Sherief Reda and Alex Orailoglu of UC San Diego, USA

Congratulations to the winners!

Tutorials

A1: System Modelling with SystemC

Organizer: Rachael Mahoney, Doulos, UK
Speaker: John Aynsley, Doulos, UK

Complexities of present systems or SoC designs are forcing the movement to a higher level of abstraction than RTL. With most of the system containing a large portion of software, the present languages, methodologies and tools are not adequate to tackle system-level design. SystemC is a C++ class library aimed at modelling systems with hardware and software content at many different levels of abstraction and using mixed models of computation. SystemC is already being proven in an industrial context for the transaction-level modelling of bus and processor based systems, where it excels.

This tutorial includes an overview of SystemC, an introduction to the key features of SystemC version 2.0, a discussion of the main abstraction levels, and a case study showing the practical use of SystemC for transaction-level modelling. A case study example design is refined from an abstract untimed functional (UTF) model using abstract fifo channels through a timed functional (TF) model to a transaction-level bus model, and finally to a cycle-accurate (CA) model including both hardware and software elements. A simple example of hardware-software partitioning is shown. The SystemC refinement process is discussed, including the use of SystemC interfaces during communication refinement. The issues of performance and accuracy of the SystemC simulation are considered in the context of the various abstraction levels.

B1: Recent Advances in Verification, Equivalence Checking and SAT-Solvers

Organizer: Dhiraj Pradhan, Bristol U, UK
Speakers: Dhiraj Pradhan, Bristol U, UK; Magdy Abadir, Motorola, US; Li-C Wang, UC Santa Barbara, US

This tutorial provides an overview of recent developments as well as basic principles in verification, equivalence checking and SAT-Solvers. It also provides a perspective of practical industrial experiences in the use and development of the tools.

In the first part the design flow and the role of RTL verification will be described. An overview of techniques will be given, including simulation-based techniques, basic concepts of equivalence checking, combinational equivalence checking, ATPG-based techniques. Also an overview of solvers will be given (structural verification, BDD-based solvers, SAT-based solvers). The role of Decision Diagrams (BDDs, zBDDs, mBDDs) will be discussed. In the second part concepts of SAT solvers are discussed, and some new EDA-related techniques are presented. Finally, the tutorial will give an overview of various commercially available tools and their applicability. Also future challenges will be lined out, such as design for verifiability, and potential new directions will be given.

C1: Mixed-Signal Design Using Verilog-AMS and VHDL-AMS

Organizer: Olaf Zinke, Cadence, US
Speaker: Olaf Zinke, Cadence, US

With the evolution towards highly integrated systems (SoC's) in ultra deep submicron CMOS technologies, more and more of these systems become mixed-signal, containing also analogue and/or RF parts. The design complexity for these mixed-signal systems requires new design methodologies.

This tutorial will give an introduction to language-based mixed-signal design methodologies. The tutorial will point out how the different analogue and digital design styles converge in the design environment. The use of Verilog-AMS as a design language and VHDL-AMS as a modelling language will be demonstrated. Examples are given on how the mixed-signal capabilities of these languages can be used to reduce the simulation time of mixed-signal systems.

D1: Infrastructure IP for SoC Yield

Organizer: Dimitris Gizopoulos, Piraeus U, GR
Speaker: Yervant Zorian, Virage Logic, US

In addition to the functional IP cores, today's Systems on Chip (SoC's) necessitate embedding a special family of IP blocks, called Infrastructure IP blocks. These are meant to ensure the manufacturability of the SoC and to achieve adequate levels of yield and reliability. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase.

This tutorial analyses the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitates the use of such Infrastructure IP. Then it concentrates on several examples of such embedded IP's for detection, analysis and correction.

This Tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2003.

A2: Reconfigurable Computing: Fundamentals, Architectures and Tools

Organizer: Andreas Koch, TU Braunschweig, DE
Speaker: Andreas Koch, TU Braunschweig, DE

Reconfigurable computing is an important architectural approach in a time of growing chip capacities and increasing demands on flexibility. This tutorial aims to introduce professionals experienced with conventional chip and system design methods to the concept of Reconfigurable Computing. The audience should be familiar with HDLs such as Verilog and have at least a passing acquaintance with programming in a software language such as C. The lecture will discuss tool flows and show examples of inputs and outputs.

In the first part of the tutorial fundamentals of reconfigurable computing will be discussed and its use will be motivated by some successful examples. The second part will examine different architectural choices for integrating reconfigurable components into a large hardware system, and will present a practical example of a reconfigurable co-processor. The third part discusses design flows for reconfigurable systems. This will cover both manual HDL-based programming as well as programming by automatic compilation from a high-level language. It will also be discussed how to exploit the reconfigurability aspect of such a system. Finally, some practical considerations will be given with an overview of commercial reconfigurable off-the-shelf devices, reconfigurable IP blocks and software tools.

B2: Performance Analysis in Communication-Centric SoC Design

Organizer: Rolf Ernst, TU Braunschweig, DE
Speakers: Rolf Ernst, TU Braunschweig, DE; Andreas Herkersdorf, IBM, CH; Lothar Thiele, ETH Zurich, CH

Performance simulation is current industrial practice in complex system design. As is well known, there are serious limitations concerning run-time and simulation coverage. On the other hand, there has been major progress in analytical methods that may complement or even replace performance simulation. This tutorial presents these new analytical methods and demonstrates them on a practical design case.

The first part of the tutorial will give an overview on the problem of performance modeling and estimation, starting from a single process to complex communication-centric heterogeneous systems. The second talk will introduce an important application domain of network processors in which performance evaluation is of highest importance for design optimisation and verification analysis has proven itself. The third talk will demonstrate how to apply formal analysis to network processor design.

C2: Modelling and Simulation Methods for High-Frequency Systems

Organizer: Georges Gielen, KU Leuven, BE
Speakers: Joel Phillips, Cadence, US; Luis Miguel Silveira, TU Lisbon, PT

The frequencies in many electronic systems keep on increasing. This involves both the clock speeds in digital systems, as well as the operating frequencies in RF circuits.

This tutorial is concerned with physical modelling and verification of high-frequency systems. Topics to be covered include parasitic and substrate modelling as well as modelling of sub-systems including frequency-described modules. The presenters will also discuss various issues in simulation, including model order reduction and algorithms for analysis and verification of RF circuits.

D2: Failure Modes in Nanometer Technologies

Organizer: Dimitris Gizopoulos, Piraeus U, GR
Speakers: Chuck Hawkins, New Mexico U, US; Jaume Segura, Balearic Islands U, ES

Process technology scaling has brought current manufacturing processes to the 100 nm region and below. The behavior of IC devices and the interconnect system in nanometer technologies brings new physical effects that, in addition to traditional well-known failure modes, open new challenges in IC testing. In this tutorial we will describe the electronic and physical basis to understand the varieties of CMOS failure mechanisms in up-to-date scaled technologies.

The tutorial will start with an overview of the traditional defect models and test solutions, leading to an analysis of the failure mechanisms in nanometer technologies. Finally, the appropriate test strategies will be presented.

This Tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2003.

Master Courses

M1: Multiprocessor Systems and Networks on Chip

Organizer: Ahmed Jerraya, TIMA, Grenoble, FR
Speakers: Giovanni De Micheli, Stanford U, US
Sungjoo Yoo, TIMA, Grenoble, FR;
Luciano Lavagno, Politecnico di Torino, IT
Ahmed Jerraya, TIMA, Grenoble, FR

Modern system-on-chip (SoC) design shows a clear trend towards integration of multiple processor cores on a single chip. Typical multiprocessor SoC applications like network processors, multimedia hubs and base-band telecom circuits have particularly tight time-to-market and performance constraints which require a very efficient design cycle. The trend is then to build large designs as a Network-on-Chip. The game is now to interconnect standard components as we used to do for boards a few years ago. This evolution is creating several breaking points in the design process.

This course will address the four main challenges for the design community:

- Prof. Giovanni DeMicheli will consider systems on chips (SoCs) that will be designed and produced in five to ten years from today, with gate lengths in the range 50-100nm. He will talk about the essential problems of interconnect in advanced technologies and the need to address them with a layered methodology that builds upon the experience in networking. He will provide some examples of design practices.

- Dr. Sungjoo Yoo will overview the on-chip communication architecture schemes covering software and hardware parts. The software part includes operating system, device driver, and hardware abstraction layer (HAL). The hardware part may include communication coprocessors such as DMA, bus/network interfaces, communication networks consisting of dynamic/static routers, and memory. He will also explain communication interface architectures such as virtual interface architecture (VIA), intelligent I/O (I2O), etc. in the context of SoC design.

- Prof. Luciano Lavagno will cover the basic concepts of platform-based design, explaining how the separation it offers between users (system designers) and implementers (IP providers) maximises flexibility and re-use, while minimising time to market.

- Dr. Ahmed Jerraya will introduce a component-based design approach to build complex architectures from basic IP modules. The approach provides a natural way to abstract hardware/software interfaces for multiprocessors and network on chip applications. This includes hardware interfaces to adapt components to the communication network and software layer including OS to isolate the software application from the architecture.

M2: Design and Design Methods for RF/Mixed-Signal Integrated Systems

Speakers: Piet Vanassche, KU Leuven, BE
Domine Leenaerts, Philips, NL
Rob Rutenbar, Carnegie Mellon U, US
Walter Daems, KU Leuven, BE
George Papadopoulos, Patras U, GR

Advances in ultra-deep submicron CMOS technology allow the integration on chip of entire systems, including both the digital cores and the analogue interface circuits. The latter provide for the communication or interaction with the outside world. Integrated systems for applications like communications, wireless, consumer, multimedia, biomedical, etc., are therefore increasingly becoming mixed-signal, containing also analogue and/or RF parts. This master course focuses on the design of such RF/mixed-signal systems. The full design flow from system requirements to silicon layout is described, and design methods and tools that support this flow are presented. This is illustrated with several practical design examples, both from existing as well as new emerging wireless applications.

This master course will address the following topics:

- The design flow for RF/mixed-signal systems from system specification to silicon layout will be reviewed and the different design steps will be identified. Architectural front-end exploration methods will be reviewed, and an overview of simulation methods for wireless circuits will be given, including steady-state analysis, phase noise analysis, etc.

- This will then be illustrated with some practical design examples from real-life industrial wireless applications such as Bluetooth and WLAN. The choices for the system architecture will be described, the design of different circuits will be presented, and the design choices and trade-offs that were taken to reduce power and cost will be explained.

- An overview will then be given of existing and emerging design methods and tools that exist to improve the quality and/or increase the productivity in the design of RF/mixed-signal systems. This includes tools for both circuit optimisation and layout synthesis of both mixed-signal and RF blocks, such as VCO's, data converters, etc.

- Finally, the emerging area of ubiquitous, ultra-small, ultra-low-power sensory-based wireless devices with ad-hoc networking capabilities will be described. Examples are body-area sensory networks, security monitoring devices, and so on. Both the radio aspects and the networking aspects will be reviewed and illustrated.

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DATE 04

Conference and Exhibition: March 29-April 2, 2004
CNIT, Paris, France
Call for Participation

Scope of the Event

The seventh DATE conference and exhibition is the main European event bringing together design automation researchers, users and vendors, as well as specialists in the design, test and manufacturing of electronic systems and circuits.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers (oral and interactive presentations), panels, hot-topic sessions, tutorials, and master courses as well as a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services. The organisation of a designer forum, user group meetings, fringe meetings, a university booth, hands-on tutorials, vendor presentations and social events offer a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community.

Areas of Interest

Within the scope of the conference, the main areas of interest are: Design methodologies, CAD languages, algorithms and tools, Testing of electronic circuits and systems, and Designer experiences. Topics of interest include, but are not restricted to:

- System and SoC Design Methods
- Modelling and Design Languages
- Formal Verification
- Platform-Based Design, IP Reuse
- HW/SW Co-Design
- Embedded System Design
- Embedded Software Techniques
- Reconfigurable Computing
- Design of Low-Power Systems
- Analog, RF and Mixed-Signal Design
- Simulation and Emulation
- Architectural and Logic Synthesis
- Physical Design and Verification
- Interconnect Modelling, EMC
- Test and Design for Testability
- Testing Cores and Systems
- Design Techniques for Emerging Technologies

Designers' Forum

As in previous years, a special track for papers presenting design experiences will be organised. Please watch the conference web site at http://www.date-conference.com/ for special instructions.

Submission of Papers

Papers have to be submitted electronically before September 14th, 2003, via the conference web page : http://www.date-conference.com/

Conference Secretariat

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