Behavioral Modeling and Simulation of a Mixed Analog/Digital Automatic Gain Control Loop in a 5 GHz WLAN Receiver

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Abstract

Wireless LAN (WLAN) operating in the 5-6 GHz range, become commercially viable only, if they can be produced at low cost. Consequently, tight integration of the physical layer, consisting of the radio front-end and the digital signal processing part, is a must. Especially with respect to mixed-signal feedback loops, with automatic gain control as a recurring example, existing tools have major difficulties in offering efficient ways of modeling and simulation. We present a modeling approach where the complexity of the analog behavioral model has been reduced to the minimum required by the digital receiver, namely its steady-state responses and a 'worst-case' time delay. Moreover, we show how this mixed-signal receiver model can be used in an end-to-end communication link simulation to provide the designer insight into statistical information such as transient delays and gain tolerances. For this model, we set up a co-simulation of two existing in-house tools, one for the analog part, the other for the digital system part.

1 INTRODUCTION

The ultimate goal for wireless transceivers is, more than for wired solutions, low–cost, which translates into the need for high integration and low implementation losses. The reason for this cost lies mainly in the traditional design partitioning. Worst case assumptions for analog non-idealities require large design margins per circuit. Circuits are designed separately and merged afterwards. Hence, individual design margins add up leading to high margins for the system and result in larger power consumption. While a circuit-level simulation of a complex front-end may simply take too long, a behavioral simulation of the front-end, which focuses on the most important contributions only, allows trading off individual margins against each other.

To solve this problem, we need to build a joint view at the analog and digital parts that translates into a modeling and simulation approach adapted to both the analog, the digital, and the systems' designer's needs. In existing tools (e.g Ptolemy alone [1], ADS [2] or SPW [3]) we find three shortcomings that discourage full system level simulations: poor modeling support, low simulation efficiency for mixed-signal, or a missing direct link towards digital implementation.

Furthermore, modeling complexity should be reduced as much as possible in order to save simulation effort. Variable-gain amplifiers (VGA) are sometimes modeled as time-varying systems [4]. However, this modeling approach has been limited to linear systems only and it does not take into account the influence of input and output impedances at RF. In our VGA model, we take into account these effects. Still, we could reduce model complexity from a full time-variant model down to a switched time-invariant approach through a common look at the analog and the digital side.

This paper reflects this partitioning. Section 2 starts with a description of the WLAN system under test. Section 3 develops dedicated models of the RF section, the time-variant variable-gain amplifier in it, and the mixed-signal AGC loop. Section 4 illustrates the model implementation in FAST and OCAPI. In Section 5, we return to the system designer, presenting simulation results achieved with this model.

2 THE WLAN SYSTEM UNDER TEST

We will use a wireless LAN end-to-end link as a system under test throughout this paper. For the purpose of mixed-signal exploration, we deliberately limit the scope to the analog and digital physical layer.

The end-to-end link consists of the mixed-signal transmitter and receiver, and the radio channel model in between (Fig. 1). The boundary of our example is the interface between multiple-access control (MAC) and physical layer (PHY), where payload data is presented in the form of data packets. This allows us to model complete transmission bursts at the physical layer.

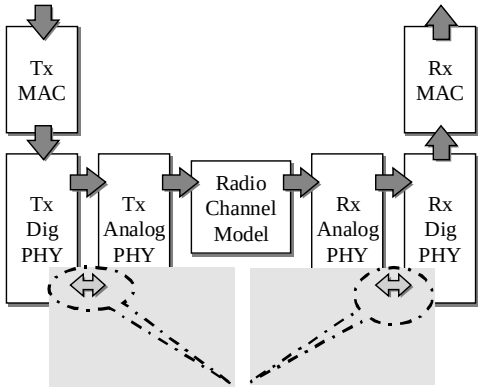

Fig. 1: The design of communications systems requires end-to-end link tests including transmitter, receiver, and channel.

The radio channel model provides it signal to the receiver (Fig. 2), consisting of a zero-IF receiver front-end followed by a digital OFDM baseband demodulator. The receive chain starts with an RF section containing LNA, controllable RF VGA and filters, providing an RF section to a pair of direct down-conversion mixers. The downconverted in-phase and quadrature signals are filtered and amplified in controllable baseband VGAs before digitized in A/D converters.

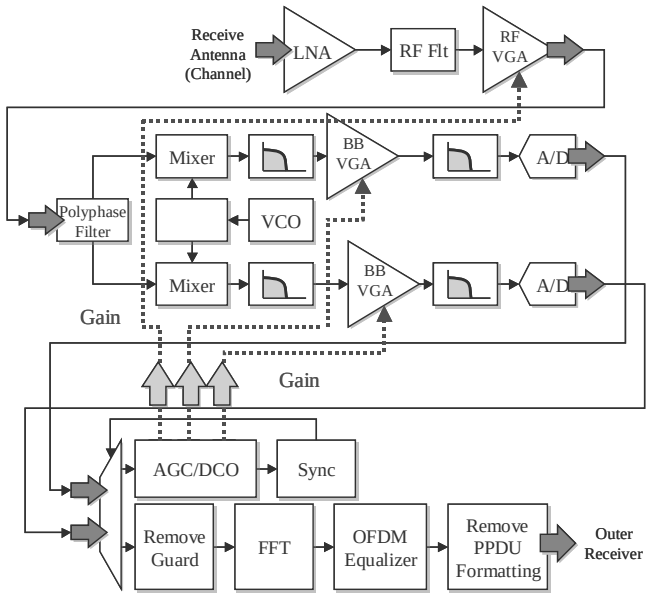

Fig. 2: The receiver is based on a zero-IF topology and a digital OFDM baseband demodulator.

Dedicated Automatic Gain Control and DC Offset Compensation (AGC/DCO) and synchronization detect incoming packets based on the packet preamble [1]. Once synchronization has been established, the cyclic prefix is removed for each OFDM symbol and the FFT transforms the time-domain signal into a multi-carrier frequency domain spectrum followed by the equalization process. Subsequently, payload is extracted and passed on to the outer receiver and the MAC.

3 MODELING

When addressing design methodology with a concrete example, two questions arise. First, we have to identify the design challenges the designer faces with this particular design. Secondly, we have to address modeling challenges that appear because we limit ourselves to abstract, behavioral models. We will see that both problems are correlated.

First, we address the modeling of the RF VGA itself. Secondly, we integrate it into a model of the entire RF section. Finally, we describe the architecture of the digitally controlled automatic gain control loop. The implementation of the models (e.g. the translation of the continuous-time blocks such as linear transfer functions and S-parameters into digital filters) is addressed in Section 4.2.

3.1 Modeling of the RF VGA

The VGA model reflects measurement results of an existing 5 GHz BiCMOS RF VGA design [6]. This circuit switches between two gain values (low and high) by selecting one out of two differential pairs that each have a different bias current. High and low gain setting are controlled digitally.. The dependency of the input matching S11 on the gain setting was specifically targeted due to its large impact on the gain (Fig. 3).

values in dB	*5.25 GHz* Lo / Hi	*10.5 GHz* Lo / Hi	*15.75 GHz* Lo / Hi
S11	-10.9 / -5.0	-0.16 / -0.19	-0.17 / -0.27
S12	-13.0 / -16.6	-53.1 / -56.4	-49.5 / -55.8
S21	-2.44 / 6.76	-46.9 / -36.0	-65.8 / -39.8
S22	-23.2 / -13.5	-5.0 / -5.0	-3.65 / -3.64

Fig. 3: The model was designed to reflect the major properties of a measured 5 GHz RF VGA.

The VGA is treated as a 3-port with external ports (x1,x2), (y1,y2) and (c1,c2). These are the RF input, RF output and control input, respectively. Indices 1 indicate incident waves, 2 indicate reflected waves (Fig. 4).

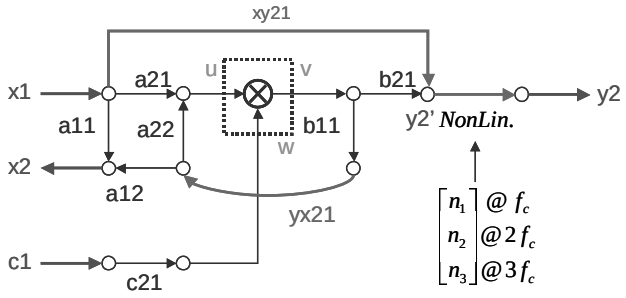

Fig. 4: The VGA model starts from an ideal 3-port model (ports u,v,w) encapsulated by a frequency-dependent set of S-parameters and a cubic nonlinearity at the output.

The model includes a core 3-port with ports (u,v,w) performing the gain multiplication. In steady state, the time-domain multiplication can be treated as a constant multiplication instead of a convolution in the frequency domain. When considering the digital receiver later, we will see that we are not interested in modeling transient effects accurately. Consequently, we only have to model these two steady states accurately, each corresponding to one gain setting. For simulation efficiency, we can now translate the time-variant 3-port into two time-invariant 2-ports. In each model, the gain control node translates into an internal constant.

We can neglect intermodulation products between RF signal and gain control since transients at the gain control input are neither too short nor too long. Moreover, gain changes are issued from the digital receiver which inserts a tolerance time period for any sort of transient effect following a gain change. Hence, we don't need to model the transient effects accurately. We can consider the VGA output y2' explicitly as linear in its two steady states and model the output compression behavior of y2 as a polynomial nonlinearity following y2'.

Between internal nodes (u,v,w) and external nodes, S-parameter networks are placed to represent the effect of input and output impedances at RF. The input dependency on the actual gain and RF feed-through effects are modeled using explicit branches yx21 and xy21, respectively. Matching the measurements, reflected waves at the baseband gain control input and the output were neglected, resulting in a set of two transfer functions (1).

$$\begin{aligned} y_2' &= \left(\frac{xy_{21}}{c_1} + \frac{a_{21} b_{21} c_{21}}{1 - a_{22} yx_{21} b_{11} c_{21} c_1} \right) (c_1 x_1) \\ x_2 &= \left(a_{11} + \frac{a_{21} a_{12} yx_{21} b_{11} c_{21} c_1}{1 - a_{22} yx_{21} b_{11} c_{21} c_1} \right) x_1 \end{aligned} \quad (1)$$

Finally, the RF VGA is represented by two transfer functions per gain setting c1 (2).

$$\begin{aligned} y_2' &= \beta_{xy}(c_1) x_1 \\ x_2 &= \beta_{xx}(c_1) x_1 \end{aligned} \quad (2)$$

3.2 Modeling of the RF section

The RF receiver section starts with the antenna followed by the LNA, a bandpass filter and the previously described RF VGA (Fig. 5). The RF VGA finally connects to the downconversion mixer. This section can be treated as a 3-port with the antenna and the gain control signal as inputs and the mixer input as output.

For behavioral simulation, frequency-dependent S-parameter models can be used to describe the linear time-invariant behavior only. Our RF VGA model however is time-variant and nonlinear. Hence, we cannot apply linear systems theory to translate the cascade into an I/O transfer functions.

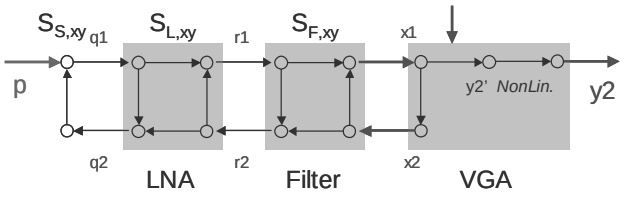

Fig. 5: A cascade of LNA, filter, and the already discussed RF VGA represent the RF section between antenna and downconversion mixer.

Still, we can represent the steady-state responses for the VGA in high and low gain mode and hence transform the iVGA into two two-port models. The model in Fig. 4 allows to decouple the cascade into a linear section up to node y2' followed by a nonlinear transfer function to produce y2. The linear part can be solved numerically when the S-parameters are given. Our specific case is also analytically tractable. Skipping the lengthy result for the general case, we only report the result (3) for the special case when conjugate matching is applied to the LNA input and the filter output and no return loss in the VGA (β_{xx}=0) is present.

$$\Rightarrow y_2' = \frac{S_{F21} S_{L21} \beta_{xy}}{(1 - S_{L11}^{\ 2})(1 - S_{S22}^{\ 2})} p \quad (3)$$

Obviously, the forward gain consists of the cascaded forward gains of its components and the input and output matching losses only.

3.3 Modeling the Mixed-Signal Automatic Gain Control Loop

The AGC loop contains two modeling problems: crossing the analog/digital boundary in both directions and correct implementation of the loop delay.

We propose a digital architecture (Fig. 6) containing a run-time controller that handles all saturation scenarios and a configuration mapper that uses both run-time information obtained through digital estimators but also design-time information [7]. Digital estimators provide signal power and DC offset estimates during acquisition phase. An extended cascade analysis at design-time provides the optimum front-end configuration for each RF input power level to the configuration mapper. The configuration mapper controls the VGAs in the front-end. This control signal closes a mixed-signal feedback loop. AGC and DCO become thus subject of both the overall impulse response of the involved analog forward and feedback paths, and the digital implementation and algorithm delays.

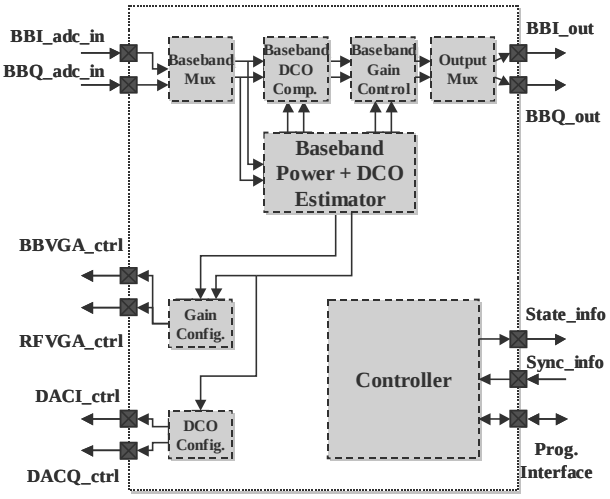

Fig. 6: The AGC/DCO protocol timing and the estimation are digital. Gains and DC offsets are adjusted through a mixed-signal interface.

Our solution is non-continuous in time and thus insensitive to the shape of the impulse response, but it requires the analysis of the overall impulse response (Fig. 7). The first 2 µs of the acquisition preamble is subdivided into three phases, each consisting of an estimation and compensation phase. The configuration mapper will adapt the VGA gain at the start of each compensation phase. For the quality of the digital estimates, it is better to reduce the number of estimation samples than to take into account samples that are affected by the gain change transients.

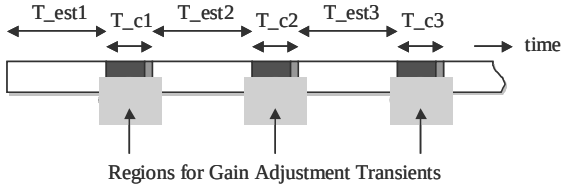

Fig. 7: The compensation phase length depends on the gain adjustment transients of the VGA, the filters, and the digital implementation delays.

Using our more accurate joint analog/digital receiver model, we can now refine the results of the statistical cascade analysis. Moreover, from the mixed-signal model we can obtain timing parameters such as loop delay and settling time, which is not possible with the cascade analysis.

4 IMPLEMENTATION IN A HETEROGENOUS SIMULATION METHODOLOGY

We propose a heterogeneous methodology for the behavioral modeling, exploration, and simulation of communications transceivers. It fully integrates digital and analog components into a system model applying dataflow process networks [8], but addresses the specific needs on signal processing granularity for the analog parts and datapath/control co-simulation for the digital part. Our methodology has been instantiated based on two existing C++ based tools: OCAPI, optimized for digital VLSI signal processing [9], and FAST, which has been optimized for the description of nonlinear analog models [10]. An interfacing layer couples the kernels of FAST and OCAPI, which both use dataflow scheduling [11]. The tools offer C++ class libraries to the user supporting this computational model. However, as discussed below, class abstraction level and scheduling approach differ.

4.1 Describing Digital Systems in OCAPI

The OCAPI technology supports gradual refinement of an object-oriented C++ model of a digital system starting from a behavioral dataflow model towards a synthesizable register-transfer (RT) level description. The RT level consists of a combination of finite state machines and datapaths (FSMD). OCAPI supports mixed simulation of dataflow and RT models. In [12], it is shown that an integration of dataflow semantics with a digital multi-processor architecture can handle parametrizable physical layers, such as the one for OFDM Wireless LAN, in an efficient way.

4.2 Describing Analog Systems in FAST

Analog systems cover a large range of frequencies, here starting with the RF at 5-6 GHz and resulting in the baseband signals around DC. Therefore, we have to take into account harmonics and out-of-band intermodulation products generated through nonlinear behavior. The program FAST uses a local multi-rate, multi-carrier (MRMC) representation of signals [10]. Here a signal is considered as a set of one or more modulated carriers, corresponding to the wanted signal, harmonics, and out-of-band intermodulation products. Each modulated carrier is represented with a complex lowpass model. Harmonics and out-of-band intermodulation products are thus explicitly addressed as individual signals. Further, all linear transfer functions that occur in the analog models, such as the S-parameters or the formulas (1)-(3), are translated into digital filters prior to the actual simulation.

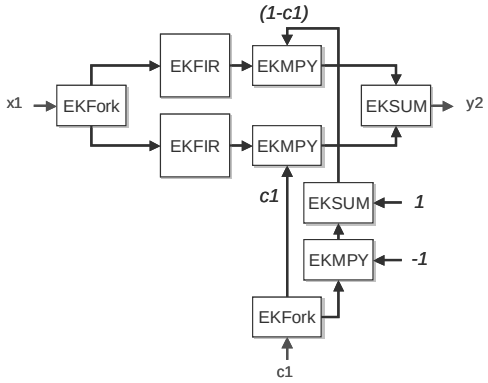

Fig. 8: The computational graph of the RF section links execution kernel library objects with signal queues.

This results in a computational graph consisting of operations such as filtering, rate transformations, time/frequency transformations, and summations. FAST libraries provide efficient implementations for these operations. As these operations do not involve any control, the FAST scheduler applies static dataflow (SDF) semantics [13]. Although analog models show a high granularity, i.e. they instantiate a large number of similar operations, this results in high computational efficiency.

The computational graph of the RF section (Fig. 8) shows a typical model consisting of library kernel blocks with basic signal processing functions and queues linking these blocks to each other. In this example, two filters (EKFIR) implement the transfer functions for high and low gain of the RF section between the antenna input x1 and the VGA output x2. Their respective results are then interpolated depending on the transient weights of the step response on the gain control input c1. The nonlinear part is not shown.

4.3 Co-simulation of FAST and OCAPI

For mixed-signal simulations involving two simulators, we can either perform co-simulation with a common co-simulation backplane or perform a true mixed-signal simulation using a single kernel. We decided for keeping separate FAST and OCAPI domains since they differ strongly in functional granularity, and the interaction between the two domains is only a fraction of the overall dataflow communication.

The FAST scheduler controls more fine-grain objects. Hence, to limit its sensitivity to interfacing and scheduling overhead in the FAST-OCAPI link, the FAST scheduler is granted master control over the OCAPI schedulers. OCAPI subsystems are embedded in special encapsulation objects. Each OCAPI scheduler keeps its full local scheduling capabilities and file I/O behavior.

The exchange of data between FAST and OCAPI is straight-forward since both simulators implement C double as data type primitive. Data synchronization is an intrinsic part of the dataflow implementation.

5 SIMULATION RESULTS

Simulation results for two typical questions, a system designer will ask about a WLAN receiver, are presented. All results involve the full end-to-end model simulation.

5.1 End-to-end Bit Error Rate Evaluation

An full transmit/channel/receive end-to-end simulation of for 80,000 payload bits takes about 25s on a Pentium III with 512 MB RAM including all pre- and postprocessing. Results can be immediately translated figures showing relevant design information (Fig. 9).

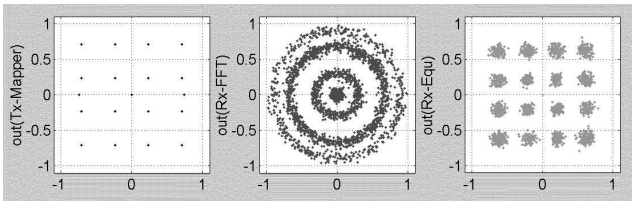

Fig. 9: Constellation plots for the mapper (Tx), before equalization (Rx-FFT), and after equalization. Part of the distortion on the 16-QAM signal can be removed (S/N = 21 dB).

5.2 Gain Range Optimization for the VGA

Besides the optimum timing, mixed-signal automatic gain control allows also trade-offs regarding the required gain range. Gain range, step size and tolerance of the

VGA have an impact on the average signal level at the A/D converter. The dependency of the BER on the RF input signal level has been analyzed with 10 bit A/D quantization, -8 to +8 dB gain range in 2 dB steps for the digital baseband VGA.

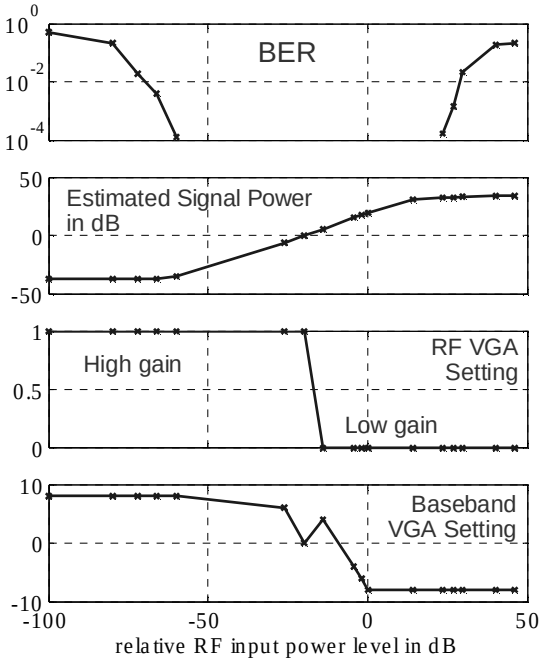

Fig. 10: The full model allows the verification of the actual receive range of the receiver in detail. Saturation and noise effects are revealed.

The run-time estimator determined the optimum setting for each power level (Fig. 10). For low input power levels, quantization and noise effects become visible while, for high input power levels, saturation effects come into play. The linear signal power estimator becomes biased both for weak and strong input signals, urging the need for the other nonlinear branch of our AGC algorithm.

6 CONCLUSIONS

We have shown how a joint consideration of the analog and the digital part of a receiver results in an efficient behavioral mixed-signal model including effects such as frequency selective S-parameters, time-variance, nonlinearities, and an analog/digital feedback loop. At the same time, the front-end modeling complexity was reduced to the minimum required by the digital processing: its steady-state responses and a 'worst-case' time delay. This simplification results in very fast yet accurate enough simulation.

We illustrated the benefits of this methodology with the development of a behavioral RF VGA 3-port model, its integration into a compact RF section model, and its co-simulation with the digital receiver in and end-to-end link simulation using two in-house tools, FAST and OCAPI. To prove efficiency and applicability of our approach, we selected two representative cases of design exploration tasks that a system designer faces in wireless communications systems. End-to-end link BER analysis involving analog nonidealities and a mixed-signal optimization problem around the VGA accuracy were successfully demonstrated. In all simulations, the mixed analog/digital automatic gain control loop is involved at the beginning of each receive burst to find the optimum gain within the constraints specified by the designer.

For the analog part, a number of manual steps (in FAST) are still required to come up with an efficient computational graph. Work is ongoing to generate and optimize these graphs automatically starting from user-defined boundary conditions such as desired accuracy.

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