Modeling and Evaluation of Substrate Noise Induced by Interconnects

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Abstract

Interconnects have deserved attention as a source of crosstalk to other interconnects, but have been ignored as a source of substrate noise. In this paper, we evaluate the importance of interconnect-induced substrate noise. A known interconnect and substrate model is validated by comparing simulation results to experimental measurements. Based on the validated modeling approach, a complete study considering frequency, geometrical, load and shielding effects is presented. The importance of interconnect-induced substrate noise is demonstrated after observing that, for typically sized interconnects and state-of-the-art speeds, the amount of coupled noise is already comparable to that injected by hundreds of transistors.

1. Introduction

Coupling through the silicon substrate in submicron integrated circuits is known to be a severe source of problems and performance limitation. The trend towards SoC integration, where highly sensitive analog sections including RF receivers, GHz oscillators and huge digital processing sections coexist in the same die, does nothing but increase the concern for this problem. As a consequence, there is an urgent demand for accurate CAD tools that allow prediction of substrate noise limitations at design stage, the earlier the better. These tools must take into account the most important mechanisms of noise injection to the substrate in current and near-future technologies. In the last decade there has been an important effort to determine the most significant sources of substrate noise [1],[2] and provide models and extraction tools for them [3],[4],[5]. Nevertheless, as signal frequencies move into microwave ranges, the sources of noise and models must be revisited, and the extraction tools adapted to the new conditions.

In recent years, tools that extract substrate parasitics are being commercialized, and their performance and accuracy are progressively improved. These tools are often based on the finite-difference method, and obtain a substrate model consisting of a mesh of impedances between circuit-substrate ports. The mesh of impedances can then be included as a subcircuit in a netlist for a full-circuit analog simulation. The extracted substrate mesh includes ports wherever a noise injection or reception point is expected. These usually are transistors and substrate contacts. Other noise injection points are commonly ignored, although their importance has not been demonstrated to be negligible. These include coupling from large metal areas like capacitors, pads and interconnects.

Intuition says that long interconnect lines driving GHz switching clocks may be a significant source of noise coupled to substrate, and coupling between these interconnects and substrate worth being modeled. Up to now, there is no known numerical study evaluating this source of coupling. In this paper, we model this coupling with a RC distributed interconnect model linked to a substrate mesh extracted with SubstrateStorm™ [6]. The interconnect-substrate model has been validated by comparing to measurements on test structures. Section 2 in this paper presents the model, and section 3 presents the experimental results compared to simulations With the validated model, the importance of this source of substrate noise is evaluated, in function of frequency, geometry, load and shielding conditions, which is presented in sections 4 and 5. Finally, section 6 draws the main conclusions from the work.

2. Modeling coupling from interconnects

Substrate extraction tools based on the finite-difference method obtain a model consisting of a mesh of impedances between circuit ports. In circuit extraction, interconnects are usually modeled ideally as a single node, in the best of cases capacitively coupled to ideal ground for delay computation purposes. In our case we want to couple the interconnects to the substrate mesh, and we use the classical distributed R-C model illustrated in Fig. 1 [7], which is now referenced to substrate instead of ideal GND. Each interconnect segment of length ΔL is instanced as two serial resistors R and a capacitance C coupled to a port of the substrate model. The values of R and C can be computed from geometrical and technology information, as

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$$R = R_{\square}\frac{\Delta L/2}{W}$$
$$C = C_{area}\Delta L \cdot W + C_{perim}2\Delta L \quad (1)$$

where ΔL and W are the length and width of the segment, $R_{\square}$ is the sheet resistance, and C_{area} and C_{perim} are the area and perimeter capacitances. The distributed RC model may be easily extended to an RLC when inductance effects are important [8],[9]. According to transmission-line theory, RLC modeling for a 500 µm long interconnect is only necessary above 15 GHz [9].

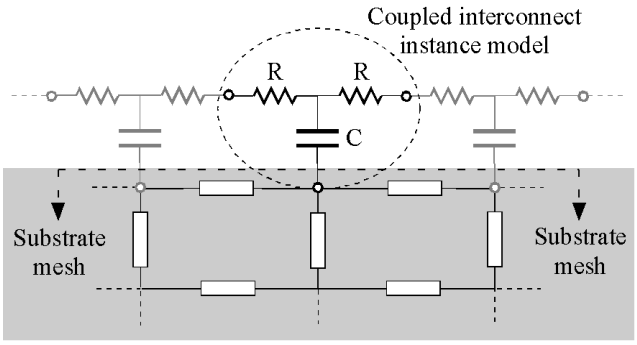

Fig. 1. Equivalent circuit model for an interconnect coupled to substrate.

We have implemented our proposed interconnect model in the flow of the substrate extraction tool SubstrateStorm™ from Cadence [6], using a 0.35 µm technology design kit. This tool extracts a substrate model consisting of a mesh of resistances between access ports, which is valid for frequencies up to some GHz. We have created new layout layers that allow to define which interconnects we are interested to extract, and the segment divisions in each interconnect. The extraction rules file was modified to identify the selected interconnects and save important geometrical data. From these data, the resistance and capacitance values where computed according to (1). Then each interconnect segment was associated to the instance model in Fig. 1, where the R and C are parameterized to the values computed. We also defined the operation of SubstrateStorm™ to create substrate ports associated to every interconnect segment instance. As a result, we are able to extract the substrate parasitics of any circuit including coupling from interconnects, and to control the accuracy (number of segments) of the interconnect model.

3. Validation of the substrate-interconnect model

The former modeling approach has been validated by comparing AC analysis simulations to experimental measurements on three test structures.

3.1. Description of the test structure

Fig. 2 shows a photograph of the test structures manufactured in a 3-metal, 0.35 µm technology on a substrate of 10 Ω·cm resistivity. The structures consist of 500 µm long interconnects, connected at both ends to pads to allow probe access. The interconnects are (left to right) 1 µm wide in metal-1 layer, 1 µm wide in metal-3, and 10 µm wide in metal-1, respectively. Near every interconnect there are two 60×60 µm^2 pads, on which coupling will be sensed. The pad at the right of every line is contacted to the substrate, i.e. allows measurement of noise on the substrate surface. The pads at the left of the lines have no direct contact to the substrate, and are coupled only through their parasitic capacitance. The pads have been accessed with GSG probes, that's why all of them are escorted by two other pads connected to ground, as seen in Fig. 2. All the structure is enclosed inside a grounded ring of substrate contacts.

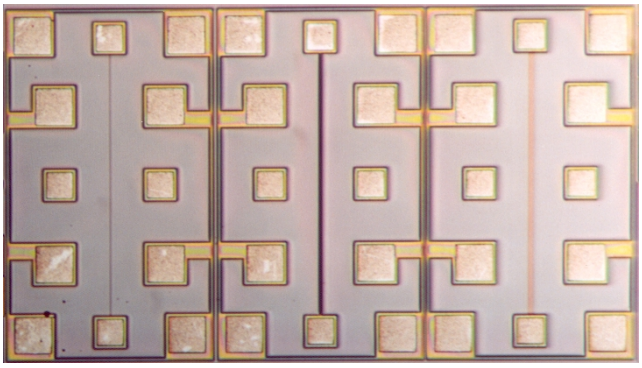

Fig. 2. Test structures implemented in a 0.35 µm technology to measure coupling from interconnects.

3.2. Measurement results

A HP 8510C network analyzer and Picoprobe 40A-GSG probes were used to measure S-parameters between line ends and the nearby pads. From these measurements, the voltage gain (coupling) between the input and output pads is derived by using Mason's rule [10], and imposing Z_L=Z_S=Z_O=50 Ω. This leads to the simple expression:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{S_{21}}{1+S_{11}} \quad (2)$$

This voltage gain determines the amount of noise that reaches the sensor pad (out) coupled through the substrate from the interconnect (in). This voltage gain is compared to that obtained from AC circuit simulations of the test structures extracted as described in section 2, including a 50 Ω load at the sensor pad to account for the impedance of the measurement equipment. The parasitic capacitances of all the pads have also been extracted and coupled to the substrate model. Coupling capacitances for the pads and the interconnect model have been obtained from geometri-

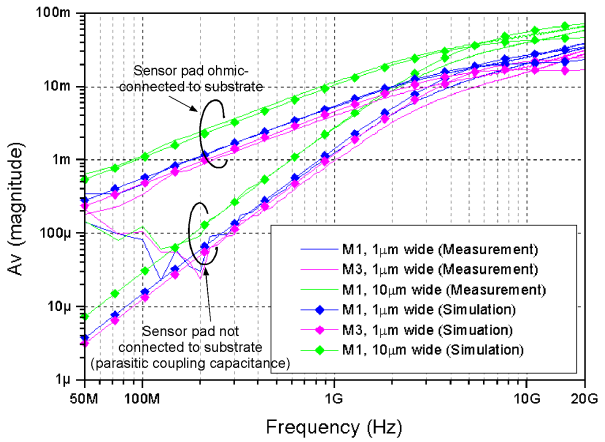

Fig. 3 Voltage coupled from the interconnects to the sensor pads. Interconnect is open-ended.

cal and technological data with the help of a 2D electromagnetic field solver. Also, a substrate resistivity profile has been reconstructed from the manufacturer's data.

Fig. 3 shows the measurement results compared against simulation results for the three test structures, when the far end of the interconnect is left open circuit. Two set of measurements and simulations are represented, one in which the output is the pad with an ohmic connection to the substrate, and another in which the output is the pad coupled to the substrate through its parasitic capacitance. An excellent agreement between simulation and measurements is verified. The agreement is lost for frequencies near 10 GHz, where the validity of the purely resistive substrate model is lost, and the interconnect starts to acquire transmission-line behavior.

Measurements with the open line present a high reflection coefficient which might lead to inaccurate results. This doesn't seem to be our case since measurements were performed on different samples and in different days, giving in all cases very little dispersion. Probe-to-probe coupling was also verified to be about 30 dB below the substrate coupling. In spite of that, we repeated the measurements now loading the far end of the interconnect with 50 Ω, with the help of a third probe. Results are shown in Fig. 4, again showing excellent agreement with the simulations.

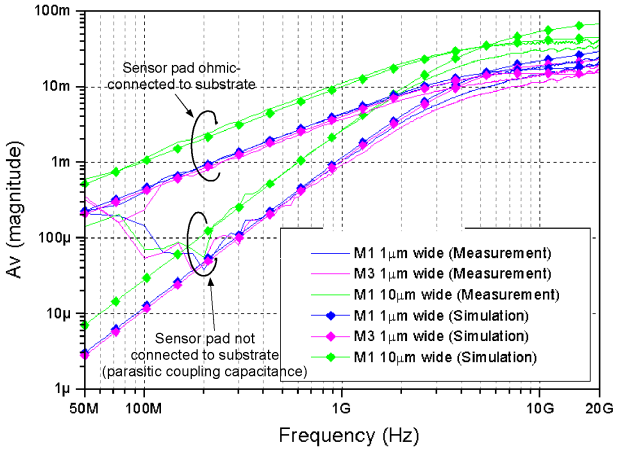

Fig. 4 Voltage coupled from the interconnects to the sensor pads. Interconnect is 50 Ω loaded.

Both in Fig. 3 and Fig. 4, a sustained increase of noise coupling with frequency is observed, due to the capacitive nature of the coupling, up to frequencies around 5 GHz. Then, coupling saturates to a level between 40 mV and 15 mV for a 1 V excitation, depending on the interconnect characteristics. These are fairly large noise levels taking into account that the output nodes are low-impedance (due to the 50 Ω probe connection).

4. Interconnect coupling quantification

4.1. Relative noise level in the substrate

Once the modeling approach has been validated, we will extend the range of situations studied and quantify the importance of substrate noise induced by interconnects. We will keep based on the layout of the structures studied in the former section, now removing all the pads except for the two output ones. Fig. 5 represents a sketch of the resulting layout. All the remaining elements have been extracted and simulated in the same accuracy conditions as in the former section.

Circuit extractions for 1-µm wide and 10-µm wide interconnects laid in metal-1, metal-2 and metal-3 are made. These extractions are simulated in an AC analysis, with the interconnect driving a realistic load consisting of 4 basic inverters of the 0.35 µm technology used. Noise is sensed on the pad with an ohmic connection to the substrate, which is equivalent to measuring the noise level in the substrate at the pad location. Fig. 6 shows the curves obtained, now in a linear scale to better appreciate the magnitude of the coupling.

It may be seen that coupling levels increase from very

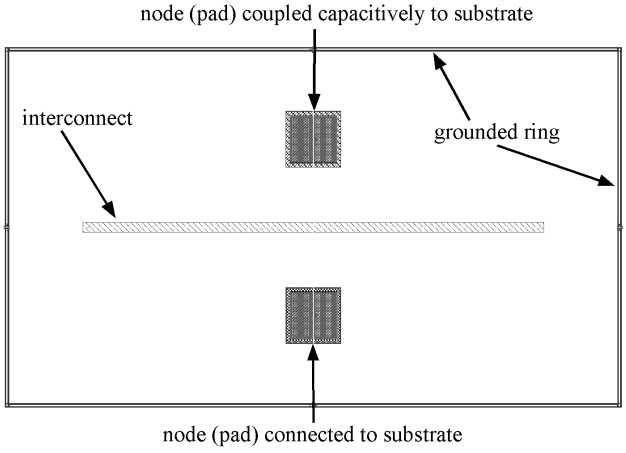

Fig. 5. Layout of the basic test structure used in the simulations.

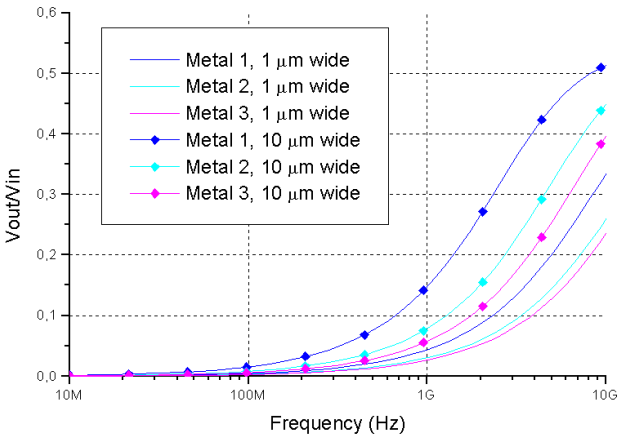

Fig. 6. Noise levels coupled to substrate when a 1 V signal is applied to lines of different widths and metal layers.

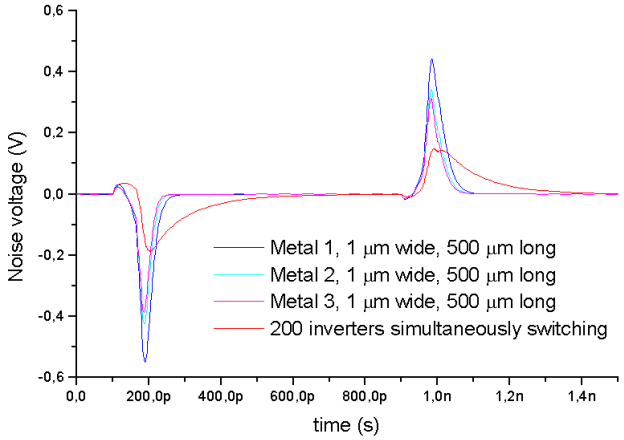

Fig. 7 Noise waveforms originated by switching interconnects compared against those originated by 200 simultaneously switching CMOS inverters.

low levels for tone frequencies below 100 MHz to surprisingly high values at frequencies around and above 1 GHz. Lines with higher capacitance to the substrate (wider interconnect, lower metal layer) present higher coupling levels. Nevertheless, the overall observation is that, for tone frequencies above GHz, interconnects couple a very important fraction of their voltage to the substrate. It must be reminded that appreciable tones of 10 GHz are already found in 2 GHz clocks [9], and tones of 2 GHz are present in clocks well below 400 MHz. Moreover, multi-GHz tones are common in CMOS RF ICs, where substrate coupling is also a concern.

4.2. Interconnect-induced noise vs. transistor-induced noise

The results in Fig. 6 suggest that interconnects are an important source of substrate noise, particularly in the GHz range. Nevertheless, to give real significance to these numbers, a comparison with other noise sources should be provided. To compare with noise injected by active devices, we have replaced the line by an array of 200 inverters simultaneously switching. The inverters are minimum-size (W/L_{NMOS}=1/0.3, W/L_{PMOS}=2.5/0.3). We drive the transistors with a square signal with 0.1 ns rise/fall time, 1.6 ns period, 3.3 V amplitude. The noise injected is compared against the noise injected by lines 1 µm wide, 500 µm long, in different metal layers. Given that transistor-induced noise is coupled from output drains, we drive the line also with 200 inverters in parallel. Thus, the switching waveforms coupled to the substrate are identical in both cases. Transistors or lines have the same fanout of 4, and are set in the same layout conditions. For a fair comparison, no substrate contacts are included with the NMOS cells. A BSIM3 model is used to simulate the extracted transistors. Fig. 7 shows the time-domain noise waveforms obtained.

It can be seen that the noise injected by the lines is between two and three times larger than the noise injected by the 200 inverters. Noise coupled directly from transistors has been traditionally considered to be the 2nd most important source of substrate coupled noise (the 1st one to be switching noise in GND and V_{DD} lines). The results in Fig. 7 indicate that noise injected by global interconnects can be at least as important as noise coupled by important amounts of switching transistors. Therefore it is a noise source that cannot be ignored by circuit designers nor by CAD developers.

5. Layout and circuit considerations

5.1. Geometrical and loading effects

Noise levels reached in Fig. 6 may be found amazingly high for some readers, which is a consequence of the layout and loading conditions of the test structures. Nevertheless, the reason of the high levels is not the short distance between the interconnect and the measuring point in Fig. 5 (approximately 100 µm), but the relative distance of the measuring point to the noise source (the interconnect) and quiet ground. To support our discussion, we will use the simplified equivalent circuit depicted in Fig. 8.

Essentially, in every situation of coupling between an interconnect and a given node in the layout, we will find a coupling capacitance between the interconnect and substrate (C_{line}); a substrate impedance between the interconnect location and the sensor node location (Z_{coup}); a substrate impedance between that node and GND contacts (Z_{gnd}); and another impedance between the sensitive node location and the sensitive node itself (Z_{sens}), which may be a resistance (sensitive node is a p-diffusion) or a capacitance (sensitive node is an n-diffusion or metal).

Let's first assume that the sensor node has no external load ("sensor load" in Fig. 8 is open circuit). Then, the disturbance sensed will be equal to the disturbance present

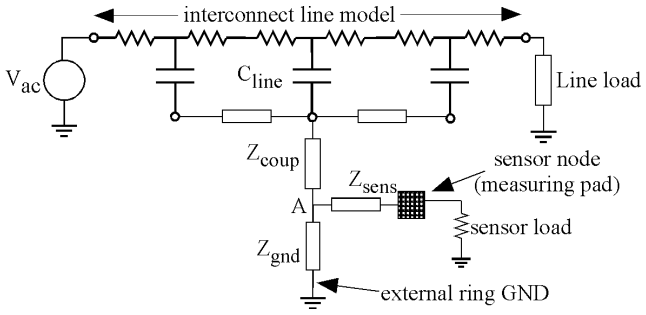

Fig. 8. Simplified equivalent circuit for a noisy interconnect coupled through the substrate to a surface node (bottom half of structure in Fig. 5).

in the substrate location below the pad (node A in Fig. 8), whichever the value or nature of Z_{sens}. The substrate node A sees a path to GND and another path to the voltage source driving the line. The amount of noise in the substrate node will be determined by the impedance ratio between those two paths. At low frequencies, the impedance to the interconnect is very high due to the series capacitance C_{line}, thus the path through Z_{gnd} dominates and the low noise appreciated in Fig. 6. At very high frequencies, the capacitance impedance is negligible, and coupling reaches its maximum. At some frequency between these two extremes, the impedances of both paths become comparable and the transition between the two situations is produced. This explains the behavior seen in Fig. 6.

In this unloaded situation, the maximum amount of noise reached at very high frequencies depends on the ratio between Z_{coup} and Z_{gnd}, which is essentially determined by the (average) distances between the sensor and the interconnect, and the sensor and ground contacts. Given the symmetry of the test structure in Fig. 5 respect to the sensor pads, the relative voltages seen in Fig. 6 saturate about 0.5 at very high frequencies. A scaled version of the test structure, keeping proportions, would lead the same maximum coupling, independent of absolute dimensions. On the contrary, the relative position of the sensor node determines the noise level. A different distribution of ground contacts in our test layout could give less concerning results, but a non-ideal ground connection including package parasitics would give worse noise levels [5].

5.2. Effect of a load impedance in the sensor node.

In the previous sections, we have quantified the noise present at the substrate surface. Nevertheless, these noise levels will be attenuated when coupled to a sensitive device, both because of the coupling impedance to that device (Z_{sens} in Fig. 8) and because its load (sensor load in Fig. 8). The lower the sensor load and the higher the coupling impedance, the lower the noise levels at the device. In order to quantify how much of the substrate noise is coupled to a sensitive device, now we measure noise on

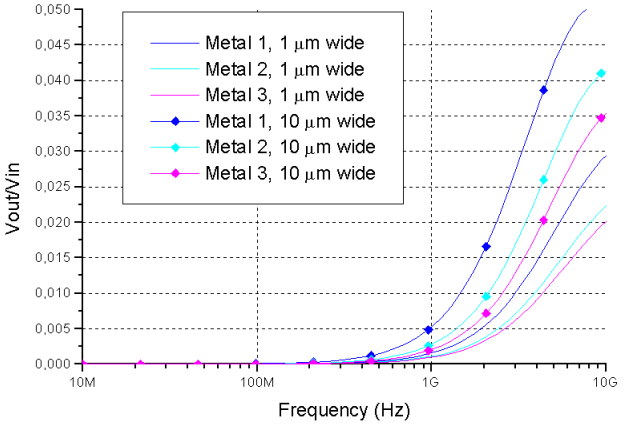

Fig. 9. Noise coupled to a sensitive device through parasitic capacitance, when a 1 V signal is applied to lines of different widths and metal layers.

the pad capacitively coupled to the substrate. The parasitic capacitance between the pad and substrate corresponds to the drain junction capacitance of a relatively large transistor, about 68 µm wide[1]. We have loaded the pad with the output of a voltage reference formed with saturated transistors of W/L=68/0.3. The results in Fig. 9 show how the effect of the load reduces the noise levels that reach the sensitive node between one and two orders of magnitude (the ratio is not frequency-constant). These noise levels match the expected amount of substrate-coupled noise, and are consistent with the levels observed in the measurements (Fig. 3), where the output node was loaded with a 50 Ω impedance.

5.3. Shielding effect of lower-layer interconnects.

We have demonstrated the potential of interconnects as substrate noise injectors. Nevertheless, this does not mean that the thousands of interconnects in an IC will all be injecting substrate noise. Those used for local routing are very short, while global nets laid in upper metal layers usually have other nets below, which will shield coupling to the substrate. Nevertheless, these general rules are not always accomplished, and some long interconnects may be found which inject noise, for example when routing from the digital core to I/O or other circuit sections. Also, it is easy to find wide and non-shielded power-supply lines, which will couple switching noise to the substrate.

We want to quantify how lower-layer interconnects reduce the amount of noise injected to the substrate by upper lines. This will quantify the importance of noise injection in shielded situations or, read in another way, the efficacy of shields to reduce coupling. We repeated the simulations for the 1 µm wide lines laid in metal-2 and metal-3 layers,

[1] Remember that coupling through junction capacitances is only one of the mechanisms by which MOS transistors are sensitive to substrate noise, being body effect of comparable importance [1], [2].

now superposed to other lines in all the remaining lower layers. Noisy and shielding interconnects are aligned and have identical dimensions, thus fringing fields from the upper line still allow coupling to the substrate. Again, we used a field simulator to obtain the capacitance matrices for these particular situations. We considered three different loading conditions for the shielding lines. A saturated small NMOS driver (W/L=1/0.3) provided a high impedance load. A large NMOS transistor (W/L=100/0.3) provided a medium impedance load. A direct connection to GND provided a low impedance load. Fig. 10 shows the results in all these conditions, compared against the results with no shield. It may be seen that the shields driven by a high impedance do not reduce the coupling to the substrate significantly. On the contrary, shields driven by large drivers or connected to ground do achieve a significant noise reduction, between 50% and 60% at high frequencies. This reduction, although significant, will probably not be enough to eliminate substrate noise problems. Thus, the conclusions from the plot in Fig. 10 are twofold. First, a single interconnect routed below a noisy line does not eliminate substrate noise injection. Second, to a make an interconnect shield effective, it should be grounded and be significantly wider than the switching interconnect, in order to collect also its fringing fields.

6. Conclusions

A model for noise coupling between integrated signal interconnects and silicon substrate has been proposed and integrated in the SubstrateStorm™ substrate extraction flow. Simulation of interconnects injecting noise to the substrate show excellent agreement to measurements of several test structures implemented in a 0.35 µm technology. The validated simulation procedure has been used to evaluate the importance of interconnects as a source of substrate noise. It has been determined that, for typical medium-sized interconnects and GHz speeds, the amount of coupling is very important, exceeding the noise coupled from hundreds of MOS transistors.

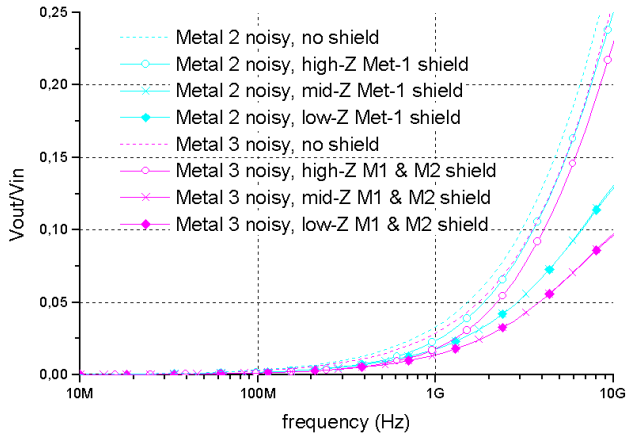

Fig. 10. Noise levels coupled to substrate when a 1 V signal is applied to 1-µm wide lines in metal-2 or metal-3. These lines are shielded by lower-layer metal lines, driven by high, medium or low impedances.

Like any parasitic coupling through the substrate, the amount of noise received in a circuit node increases with increasing load impedance and decreasing distance to the noise source. Shielding offered by single lines has been shown to be insufficient to eliminate coupling. From the frequency dependence, it is expected that interconnect-induced coupling will gain importance in near-future technologies and become a dominant source of substrate noise, an extra source of power dissipation, and a potential reason for circuit malfunctioning. Therefore, its consideration by designers and substrate parasitics extraction tools should not be ignored anymore.

Acknowlegments.

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