Recent Advances and Future Prospects in Single-Electronics

Christoph Wasshuber
Texas Instruments
PO. Box 650311
Dallas, TX 75265
wasshub@ti.com

ABSTRACT
We will introduce new developments in single-electron logic technology and review a few clever applications made possible when single-electron transistors are combined with CMOS.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and design styles – *advanced technologies.*

General Terms
Design

Keywords
single-electron logic, random background charge, MOSFET, SET

1. INTRODUCTION
Single-Electronics is a technology where one electron is sufficient to define a logic state. Instead of working with currents and voltage levels, which are defined by millions of electrons in today's CMOS technology, one can realize the limit of calculating with single electrons. However, single-electron logic has been considered in the past as unrealistic due to its random background charge sensitivity. Any trapped charge or moving charge in proximity to a logic gate could flip its state making the outcome unreliable. This problem lead to research focusing on single-electron memories, rather than logic, where several known solutions to this fundamental random background charge problem exist. Recent advances in single-electron logic warrant a fresh new look at its potential future prospect.

We are also going to briefly look at a few very interesting applications of how a single-electron technology could be combined with CMOS and provide a lot of functionality with few devices and small chip area.

No matter how good a single-electron technology might turn out to be, it is hard to imagine that it will outright replace CMOS technology. The biggest benefits seem to lie in the clever combination of both.

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2. SINGLE-ELECTRON LOGIC
Probably the biggest disadvantage of a single-electron transistor (SET) is it's large charge sensitivity. For sensors that is a great thing. One can build super sensitive electrometers that way. But for logic this is pretty bad. It is so bad that many believe it is impossible to ever build a VLSI circuit using single-electron technology. Any trapped charge or nearby charge movement could easily flip the state of a gate producing an error. It has been reported that measured SET characteristics shifted over a period of a few minutes to hours because of some background charge movement. It would of course be conceivable to add redundancy into the logic and provide error correction. However, the random background charge noise level can be too high to make error correction or even error detection work. It might also be possible to resort to inherently redundant hardware, such as neural networks. Unfortunately such hardware is not considered as a general replacement for standard logic. It would also be conceivable to use an 'operating point refresh' which adjusts the SET bias conditions to account for any background charges. But non of these schemes provides a clean and efficient solution to the random background charge problem.

However, there is one feature of a SET which does not change with changing background charge, and this is the periodic Id-Vg characteristic. The phase of this IV-characteristic changes with changing background charge, period and amplitude do not. So in order to build a random background charge independent logic one has to code information into the period or amplitude of this Id-Vg characteristic. How this can be done is described in detail in R. Klunder's recent thesis [1].

The period and amplitude of the transfer function of a current biased SET are functions of gate and junction capacitance. In order to modulate amplitude and or period according to some input signal one requires a way to modulate capacitance. This is of course not so easy to implement in a real device, because we are talking nanometer scale here. But one could imagine to use a pn-junction capacitance which can be modulated by its applied bias or perhaps a suspended gate whose distance to the SET can be modulated and thus gate capacitance can be modulated.

It is therefore possible to build a random background charge independent logic using amplitude or frequency modulation schemes to code information. Such logic has to be slower than a direct coding of information into current or voltage levels, because to determine a logic state several periods will have to be used. However, the fundamental speed limit of SETs is linked to the speed of quantum mechanical tunneling which is a sub-pico-second process and offers therefore plenty of room to realize a fast SET logic. Chip area (cost) and power advantages are the real

strong points of a single-electron technology, which would not be altered by a modulation scheme.

It is therefore conceivable, assuming that an AM-FM SET (a SET where gate capacitance can be modulated) can be manufactured, that a random background charge independent single-electron VLSI logic technology is feasible.

There are still several serious engineering hurdles to be overcome before large scale integration and large scale designs are possible. One other weak point of a SET is its voltage gain, which is given by the ratio of gate capacitance to junction capacitance. Gains of >1 have been reported but are also associated with lower operating temperatures due to increased total node capacitance. That is why a combination with MOSFETs as gain elements can be a very viable alternative.

Achieving room temperature operation requires structures in the few nanometer regime. We don't know today how we are going to manufacture millions of such small structures reproducibly. Ideas are floating around from thousands of parallel STM tips to self-assembled nanostructures using DNA or other macro-molecules. All of these are great and wonderful ideas but have yet to be demonstrated, proven and tested.

3. APPLICATIONS

One of the unique key features of a single-electron transistor compared to a conventional CMOS transistor is its periodic Id-Vg characteristic. This periodicity is inherent and random background charge only influences the phase of this characteristic but not its period or amplitude.

If one would like to replicate a similar IV-characteristic in CMOS, one would need many transistors, not just one as in the single-electron case. This functional disparity between a single-electron transistor and CMOS opens up the possibility to pack more functionality into less devices and less chip area.

Two recent examples of such clever exploitation of single-electron transistors are described in [2] and [3]. Both circuits use essentially the same critical circuit element, a series connection of a MOSFET with an SET, albeit at different operating points, to realize a quantizer and a random-number generator, respectively. The periodic IV-characteristic also lends itself to various multi-valued logic schemes.

The MOSFET provides the necessary gain element, since gain is difficult to achieve with single-electronics, and the SET provides high functionality through its periodic IV-characteristic.

In the case of the random-number-generator [3] the numbers are pretty impressive. Power consumption of the SET-MOS implementation is seven orders of magnitude less, at eight orders of magnitude smaller occupied area. One of the reasons for this stellar performance is the large (four orders of magnitude higher) telegraphic noise of the root-mean-square value of 0.12V achieved in the SET.

4. CIRCUIT ANALYSIS

To test out these and other ideas and analyze single-electron circuits or hybrid MOS-SET circuits two types of simulators are available. One is an extension of SPICE with special SET models as the one in [4] or [5]. And the other are dedicated single-electron simulators such as described in [6] and available from [7].

The SPICE based simulators have the advantage to simulate large circuits in a well known and familiar tool environment, but are not yet able to deal with interacting SETs or other sometimes important physics such as higher-order tunneling effects or quantum mechanical phenomena.

Detailed Monte-Carlo simulators, such as SIMON [6][7], capture all the necessary physics but are limited in terms of circuit size and circuit element types.

Therefore a combination of both simulator types is desirable. It allows detailed analysis of small circuit parts as accurately as we are able today, as well as the simulation of large designs with reasonable accuracy and speed.

5. REFERENCES

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