On-chip Thermal Engineering for Peta-scale Integration

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Abstract

Heat removal is already a significant manufacturing issue in the current product engineering of VLSI systems. The problem will get much more serious in peta-scale integrated systems with much higher energy consumption and complex interconnect structures, potentially including optical interchip and even intrachip communications. New thermal engineering is much needed for both performance and reliability. In the current product development-quality CAD practice, few tools can provide accurate electrothermal analysis of integrated circuits, let alone optical interconnects. The conventional circuit level and timing analyses use uniform temperatures estimated from the ambient temperature, average power consumption of the chip and the thermal conductivity of the package. It has been shown that under poor thermal design seemingly perfect circuit can fail due to rather significant temperature differential. This was a case for a 10bit adder surrounded by a high power module on one side and a moderate power module on the other side. Yet the conventional method using an average power dependent uniform temperature for simulation, even in the worst case, fail to capture the malfunction of the circuit. In this case the uneven temperature profile of the circuit caused skew in signal propagation delays enough to cause what should be a clean digital voltage switching to be a voltage glitch. Product development managers in semiconductor industry have reported such problems.

Electromigration (EM) reliability also critically depends on local temperature. Thus the estimation of interconnect temperatures and their impact on EM reliability besides propagation delays becomes important. Both accuracy and computational efficiency should be achieved in the development of new CAD capability. Optical interconnects (OI) on chip or chip-to-chip has been discussed over the last few decades. And its commercial applications have been slow in coming. However, the need for OI has been slowly increasing as evidenced by the recent creation of optoelectronics business sector in Intel Corporation. In a peta-scale system, optical interconnects are likely to be essential, especially for 3D interconnects with high signal fidelity. Computer-aided design of OI systems using novel compact models for laser diodes and photodetectors should become as routine as the current VLSI design practice that relies on SPICE-like simulation tools and high-level simulation tools, such as Rsoft's LinkSIM.

Equally important issue is how to solve the local hot spot problems in energy efficient manner. The recent development of thermionic cooling by A. Shakouri of UC Santa Cruz provides an inroad for electronically controllable local cooling of hot spots. However, such hot spots should be predicted with realistic assessment based on specific environmental conditions such as the substrate system, thermal conductivity of package, and on-chip power consumption. P. Mazumder of UC Berkeley introduced a novel method for cooling using nanotubes. Based on the thermal and electrical measurements of individual or small bundles of nanotubes, a composite can be designed for the desired electromagnetic and thermal properties. Microfluidic devices have been used to align nanotubes in a certain direction. Carbon nanotubes can be mixed with monomer solutions and then injected into such microfluidic devices to align carbon nanotubes in the desired spatial pattern. These are some examples of potential methods for thermal engineering.

In this talk, we will review recent efforts for thermal engineering and consider what design methods and technologies may become available options for peta-scale integration with high-performance and reliability.

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