Variable-Segment & Variable-Driver Parallel Regeneration Techniques for RLC VLSI Interconnects

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ABSTRACT

Repeaters are now widely used to enhance the performance of long On-Chip interconnects in CMOS VLSI. For RC-modeled interconnects, parallel repeaters have proved to be superior to serial ones. In this paper, a Variable-Segment Regeneration Technique is introduced and compared with a Variable-driver Parallel Technique, a recently proposed transparent repeater and with three conventional techniques. HSpice Simulations using a 0.25 µm TSMC technology show that both the variable-segment and variable-driver techniques feature 62% time delay saving and 354% Area-Delay product saving over the transparent repeater, and are superior to all conventional techniques. However, our new variable-segment technique is characterized by a 116% Area-Delay product saving over the variable-driver technique. Thus, making it the most performant in the field of high-performance RLC interconnect regeneration. The simulation results confirm the superiority of the parallel regeneration technique over the serial ones.

Keywords

VLSI, RLC Interconnect, Parallel Regeneration, Repeater.

1. INTRODUCTION

The rapid growth of the VLSI technology has led to the constant reduction of the feature size of VLSI devices and thus high levels of integration. The speed of on-chip circuitry is so fast that a significant portion of the total delay in a processing unit comes from the time required for a signal to travel from one chip to anoth-

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er and from one part to another part inside the chip [1]. The driver resistance, the interconnect and loading capacitance, and the interconnect resistance are the parameters that determine the interconnect delay [2].

In the last years, technological advances made the On-Chip inductance of interconnect to be of significance especially with the usage of new low resistance materials in the fabrication of interconnect lines, in addition to the invention of new dielectrics which contribute in the reduction of the interconnect capacitance. Also, the usage of higher operating frequencies contributes in increasing the importance of inductance as well [3,4]. The importance of On-Chip inductance is increasing because of faster rise time signals and longer wires [4].

Multiple solutions for driving highly capacitive loads such as the High-Drive (HD) buffer [5], or cascaded tapered buffers [6] have been proposed. Complete descriptions of the approaches for driving highly resistive RC interconnects, such as repeaters, can be found in [2,7-9]. Secareanu et al. [8] proposed a high-drive CMOS buffer circuit characterized by a voltage transfer characteristic (VTC) with low threshold voltages & hysteresis and a capability of restoring slow transition times and distorted input signals with a minimum delay penalty. This circuit was modified to implement a High-Drive Transparent Repeater (HDTR) which is a parallel regeneration structure. It was used by Secareanu and Friedman [9] with a variable-length segment methodology to drive highly resistive RC interconnects. However, they partitioned the interconnect using 4 design phases, which unnecessarily complicates the usage of such technique by designers. Also, some phases are no longer applicable in sub-micron technologies as the limit of interconnect length, beyond which regeneration improves interconnect delays, decreases when technology is scaled down [7].

Only two works are found to be related to regenerating RLC interconnects. The first was proposed by Ismail and Friedman [10], in which they applied a conventional serial technique. The second work was performed by Awwad and Nekili [11], where a parallel technique was applied in an RLC context. We proved the parallel technique to be superior over the serial and non-regeneration techniques.

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In this paper, a new Variable-Segment Regeneration Technique VSRT is introduced, and compared to the Variable-Driver Parallel Regeneration Technique previously introduced by Nekili et al. [12] and the transparent repeaters introduced by Secareanu and Friedman [9] which were previously used to regenerate RC interconnects and applied here in an RLC context. Also, in this paper, we compare the performance of these three parallel configurations with the non-regeneration, serial regeneration and parallel regeneration techniques [11], in terms of Silicon area and propagation delay.

A motivation of this paper lies in the following. The HDTR is expected to add zero delay to the interconnect [9]. However, the large number of transistors composing this type of repeater affect the interconnect by their parasitic capacitances. It becomes interesting to compare it to the Variable-Driver Parallel Regeneration Technique, which proved to be superior to the serial and non-regeneration techniques in an RC context [12].

The rest of the paper is structured as follows. Sections II & III respectively describe the Variable-driver Parallel Regeneration & the High-Drive Transparent Repeater techniques. Section IV summarizes the simulation results, introduces the Variable-Segment parallel Regeneration Technique and compares it to all other techniques.

2. A VARIABLE-DRIVER PARALLEL REGENERATION TECHNIQUE (VPRT)

Figure 1 shows the basic circuit of a parallel regenerator that led to this structure. It was used by Nekili and Savaria [7] to regenerate an RC interconnect which allows an enhancement of performances compared to conventional methods. Awwad and Nekili [11] used this circuit to drive an interconnect where inductance is significant.



Figure 1. Parallel Regenerator Basic Circuit

The network shown in Fig. 1 is any arbitrary pass gate network. A p type transistor PMOS1 is used to pre-charge the line. A logic level "0" generated from the network will discharge the line in the evaluation phase. A transistor mounted in parallel with the line can accelerate the discharge as soon as a sense gate detects this transition. Since the discharging transistor has to be activated by the falling transitions on the line, it must be related to the line through an inverter. This configuration needs a precharge signal to operate correctly [7].

The regenerator of Fig. 1 adds, a priori, no delay to the line if inserted at regular intervals, in parallel with the line as shown in Fig. 2. Nevertheless, it is important to notice that each of the regenerator transistors affects the line delay by its parasitic capacitance. It is then useful to select adequately the channel widths w_1 , w_2 , w_3 and w_4 of these transistors. According to Nekili and Savaria [7], a functional analysis of the circuit in previous Fig. 1 has shown that only w_2 and w_3 are critical to the performance.

The spacing interval is called l_{seg} . The optimization process consists of finding the triplet (w₂, w₃, l_{seg}) that gives the minimal delay for a line with a length l_{line} . The complete analysis and optimization criteria are presented in [7] and [11,12].

In this paper, we are using the Variable-driver Parallel Regeneration Technique (shown in Fig.2 and called VPRT) which was proposed by Nekili et al. [12] to regenerate RC interconnects.



Figure 2. Parallel Regeneration Technique

The VPRT configuration used here starts at $w_3=25 \ \mu m$ for the first stage and ends with $w_3=12.8 \ \mu m$ in the nth stage. The decreasing factor from one stage to the next one is calculated according to the following equation presented by Nekili et al. [12] (from left to right):

- the first regenerator has a size of α ,

- at each of the following stages, the regenerator size is linearly decreased, by an amount of $(\alpha - \beta)/(n_s - 1)$ until we reach the last regenerator whose size is β . The parameter β is the optimal regenerator size when a regenerator drives only one interconnection segment.

We follow the approach proposed by Nekili et al. [12] to determine the sizes of the 4 transistors of each stage. Also, the segmenting criteria l_{seg} for this configuration is based on the same criteria used in [11].

3. A HIGH-DRIVE TRANSPARENT REPEATER (HDTR)

Figure 3 shows the basic circuit of a high-drive transparent repeater. This circuit is a modified High-Drive Repeater (HDR) buffer with low threshold voltages and minimum line loading. It detects slow or fast transitioning input signals early in the transition process by employing a VTC featuring low threshold voltages and hysteresis [8]. This can be done by implementing a 3 stage transistor-level schematic of the proposed HDTR circuit as shown in Fig. 3. Several circuit details and sizing strategies employed for different trade-offs and important in implementing the desired function of the HDTR are described in [5,8,9].



RLC Interconnect Line

Figure 2. High Drive Transparent Repeater Basic Circuit

In this paper, we used two methodologies to optimize and setup the HDTR configuration. In the first methodology, and after several simulation attempts, we found that 10 equal segments can be used to partition the 10 cm line. The width sizes of the HDTR transistors Qu, Qd, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8 are respectively $5.4 \ \mu m$, $16.2 \ \mu m$, $10.8 \ \mu m$, $32.4 \ \mu m$, $32.4 \ \mu m$, $3 \ \mu m$, 8 μm , $44 \ \mu m$, $130 \ \mu m$. We used equal repeater sizes with equal segment lengths.

In the second methodology, we used equal repeater sizes with variable-length segments. The complete interconnect is partitioned into monotonically length-increasing segments. The first segment (SEG1) is the shortest while the last one (SEGn) is the longest. The criteria of partitioning the interconnect is based on empirical experimentation. SEGn is controlled and regenerated by the first HDTR repeater then the second segment is controlled and regenerated by both the first and second HDTR repeaters, continuing this way until SEGn which will be controlled and regenerated by all HDTR repeaters.

4. SIMULATION RESULTS AND DISCUSSION

Simulation results are shown in Table 1, which lists the propagation delays associated with the 10 cm line length and $0.9 \,\mu m$ line width using the VPRT and HDTR configurations. Table 1 also shows the results obtained from [11] using Non-Regeneration (NRT), Serial Regeneration (SRT) and Parallel Regeneration (PRT) techniques for the same line length and width, where type-10, type-13 and type-30 correspond to a configuration with 10 equal segments, 13 different segments (based on the above-mentioned second methodology) and 30 equal segments respectively. To set the optimum number of segments, several empirical values were attempted through simulations.

From Table 1, on one hand, one observes that VPRT-30 features 62%, 12%, 22%, 568% time delay savings over the HDTR-10, HDTR-13, SRT-30 and NRT configurations respectively. This is due to smaller total parasitic capacitances contributed by VPRT regenerators to the interconnect compared with the other techniques. Indeed, as the size of repeaters decreases towards the end of the interconnect, the parasitic capacitance of repeaters decreases too. On the contrary, with the HDTR repeater, for example, the parasitic capacitance of repeaters remains constant throughout the interconnect. On the other hand, the VPRT-30 features a worse delay than PRT-30, i.e., 8.7% time delay saving of PRT-30 over VPRT-30. This is due to a better ratio of driving capability and parasitic capacitance of PRT. Also, increasing this ratio does not substantially improve PRT over VPRT, while unnecessarily increasing the area.

Table 1: Propagation Delays and Silicon Area Comparisons Associated with HDTR, VPRT, PRT, SRT and NRT for 10 cm Line Length and $0.9\mu m$ Line Width.

	HD- TR- 10	HD- TR- 13	VPRT- 30	PRT - 30	SRT - 30	NRT
t _{pd} (nsec)	8.1	5.6	5.0	4.6	6.1	33.4
Area (µm) ²	815	1059	262	339	529	

Moreover, Table 1 shows that the HDTR with 10 equal segment lengths is the slowest among other regeneration techniques. This is due to the fact that each HDTR loads the line with a large parasitic capacitance. The large number of transistors in the repeater, which are connected to the line, contribute to this performance degradation. However, this configuration is still useful since it features 310% time delay saving over the non-regeneration technique.

Also, Table 1 shows comparisons between the repeater-based regeneration techniques in terms of Silicon area occupied by the inserted repeaters, accounting only for the active channel areas of the transistors, as a first order approximation. We observe that VPRT-30 configuration features 211%, 304%, 29%, 102% Silicon area savings over the HDTR-10, HDTR-13, PRT-30, SRT-30 configurations respectively. Not only initial conditions are needed to reset the output stage of HDTR (sequential circuit), which adds up more complexity to its design, but it has also the worst Silicon area than the other regeneration techniques. In addition, one observes that the VPRT-30 (for the case of $w_3=25\mu m$), since the geometrical size reduction of the VPRT regenerators along the interconnect leads to a reduction of the total area.

Table 2 indicates the Area-Delay product (AT) savings for the five different regeneration techniques. As seen from this table, VPRT uses the least Area-Delay product among all other techniques investigated in this paper. This superiority of VPRT is due to the relatively high ratio of driving capability to parasitic capacitance and its geometrical size reduction along the interconnect.

Table 2: Area-Delay Product (AT) Savings associated with HD-TR, VPRT, NRT & PRT for 10 cm Line Length and $0.9\mu m$ Line Width.

	HD- TR- 10	HD- TR- 13	VPRT- 30	PRT- 30	SRT
AT (*10 ⁻¹⁸) m ² sec	6.6	5.9	1.3	1.6	3.2

4.1. A Variable-Segment Regeneration Technique (VSRT)

The regeneration structure (Fig. 2) introduced in [12], used the Variable-driver Parallel Regenerator inserted at regular intervals in the interconnect to be regenerated, thus dividing the interconnect into equal segments. To ensure a uniform driving capability for all segments of the interconnect, the size of the regenerator was decreased as we move towards the interconnect end. Another way to keep this uniformity is to divide the interconnect into variable segment lengths, while maintaining the same equal sizes of inserted PRT regenerators. Figure 4 shows our new Variable-Segment Regeneration Technique (VSRT).



Figure 3. A Variable-Segment Regeneration Technique (VSRT)

Let us assume that:

-the interconnect is partitioned into N different segment lengths.

-the first segment length (percentage of the total interconnect length) is L_1 .

-the uniform difference in segment lengths between any two successive segments is δ , such that:

$$L_2 = L_1 + \delta$$
$$L_3 = L_2 + \delta = L_1 + 2\delta$$
$$\dots$$
$$L_N = L_1 + (N - 1)\delta$$

thus,

$$L_1 + L_2 + \dots + L_N = 1$$
$$L_1 + (L_1 + \delta) + (L_1 + 2\delta) + \dots + (L_1 + [N - 1]\delta) = 1$$

which becomes,

$$NL_1 + \delta \sum_{i=1}^{N-1} i = 1$$

This equation can be simplified into,

$$NL_1 + \delta \cdot \frac{N(N-1)}{2} = 1$$

And hence,

$$\delta = 2 \cdot \frac{1 - L_1 N}{N(N - 1)}$$

As δ is positive, this equation assumes that N >1 and $L_1 < \frac{1}{N}$.

One strategy of investigating the performance of VSRT versus VPRT configuration, is to maintain the same Area-Power (AP_0) product for both of them and then perform a comparison of propagation delays.

Note that the Silicon area of one PRT regenerator ($w_3=25\mu m$) is $11.3*10^{-6} \mu m^2$, a VSRT with a Silicon area of $A_0=262*10^{-6} \mu m^2$, which is needed to regenerate the 10 cm interconnect, requires 23 segments. Table 3 shows the propagation delays associated with the 10 cm line length and 0.9 μm line width using an A_0 -area VSRT with N=30, 23 and 10.

A 30-segment A_0 -area VSRT requires a w_3 of 18.87 μ m for each of the inserted PRT regenerators, while a 10-segment VSRT requires a w_3 of 61.85 μ m.

From Table 3, one observes that, for a specific number of segments, as L_1 is decreased, the propagation delay becomes smaller since the load provided by the segment L_1 is reduced. However, as L_1 crosses a certain limit, which corresponds to the point where the non-regeneration technique performs better than putting a driver per segment, the propagation delay gets worse.

Moreover, Table 3 shows that, as the number of segments of VSRT increases, the propagation delay decreases as well.

Table 3: Propagation Delays associated with VSRT occupying (A_0) total Silicon area, for 10cm Line Length and $0.9\mu m$ Line Width.

N	L ₁ (%)	δ*10 ⁻⁴	t _{pd} (nsec)	
30	3.2	91.95	5.0	
30	2	9.2	5.1	
30	1	16.09	5.2	
23	4.3	4.35	5.2	
23	3.5	7.7	5.1	
23	1	30	5.4	
10	9	22	14.8	
10	5	111	6.5	
10	1	200	7.2	

A possible explanation of this observation is as follows. Assume a driver i sees the interconnect up to a certain distance, d_{lim} , which is realistic because, for example, the effect of the 1st driver on the last segment is negligible compared to the effect of driver N-1 on the last segment, all the drivers having the same driving capability. Increasing the total number of segments increases the number of drivers from driver i within the distance d_{lim} . The probability that the effect of driver i becomes negligible, when compared to one of the additional drivers (the farthest from driver i), increases. The consequence is a reduction of d_{lim} for driver i and therefore a lower propagation delay. It all happens as if driver i was driving a smaller interconnect.

The analysis above assumes that, after increasing N, the driving capability of driver i remains constant. Actually, assuming a constant-AP₀ strategy, the driving capability of all drivers should decrease. However, the propagation delay decreases linearly with the driving capability and quadratically with the interconnect length. Therefore, if both the driving capability of driver i and d_{lim} decrease in the same proportion, the propagation delay will still decrease.

Another strategy of investigating the performance of our VSRT versus VPRT configuration, is to seek optimum design parameters through empirical trials to obtain the best Area-Power (AP) product saving and/or the best propagation delay saving. Table 4 lists the propagation delays and Area-Delay products associated with the 10 cm line length and 0.9 μ m line width using our new VSRT configuration.

 Table 4: Propagation Delays and Area-Delay products

 associated with VSRT occupying variable total Silicon area,

 for 10cm Line Length and 0.9μm Line Width

N	L ₁ (%)	w ₃ (μm)	Total Area (µm) ²	t _{pd} (nsec)	AT
10	1	12.8	61.7	9.8	0.6
23	1	12.8	141.8	6.4	0.91
23	3.5	12.8	141.8	6.1	0.86
23	1	8	94.1	7.5	0.71
23	3.5	8	94.1	7.2	0.68
26	1	25	293.8	5.1	1.5
26	1	12.8	160.3	6.1	0.98
26	1	8	106.4	9.1	0.97
30	2	25	339	4.8	1.6

Note that the unit used for the Area-Delay (AT) product in this table is $(*10^{-18})$ m²sec.

Table 4 shows that, on one side, VSRT (the case of N=30, $w_3=25$ and $L_1=2\%$) features 4.2% propagation delay saving than VPRT-30. However, it is worse in terms of Silicon Area consump-

tion than VPRT-30. On the other side, VSRT (the case of N=10, w_3 =12.8 and L_1 =1%) has a much better Silicon Area saving than VPRT-30, however, the later features 95% propagation delay saving than the former. For this specific case, our new VSRT has much better Area-Delay product saving (116%) than VPRT-30. Designers can choose among the various configuration parameters to achieve the required optimum goal.

As seen from Tables 1, 2, 3, and 4, VSRT uses the least Silicon area, thus consumes the least power and has the fastest speed which makes it more performant in the field of high-performance interconnect regeneration than the other techniques discussed in this paper.

5. CONCLUSIONS

In this paper, a Variable-Segment Regeneration Technique is introduced and compared with five existing regeneration techniques. The comparison criteria were Silicon area usage and propagation delay. From the comparative analysis, it is found that both our new regeneration technique and the VPRT use the least Siliconarea, consume the least power and have the least propagation delay than the existing regeneration techniques. However, a careful optimization makes our variable-segment technique to be more performant in terms of Area-Delay product than the VPRT, and therefore the most suitable in the field of high-performance RLC interconnect regeneration. This paper also confirms the superiority of the Parallel Regeneration Technique over the serial ones.

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