Low Swing Dual Threshold Voltage Domino Logic

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ABSTRACT
A low swing domino logic technique is proposed to decrease power consumption without sacrificing noise immunity. With the proposed low swing domino logic circuit technique, active power consumption is reduced by up to 9.4% while improving the noise immunity by 2.6% as compared to standard domino logic circuits. It is also shown that by applying a low swing contention reduction technique, the power savings can be further increased by 6.7% while the delay can be improved by 8.6%. A simple and efficient dual threshold voltage (dual-V_t) circuit technique that incorporates low swing signals is also proposed. It is shown that the proposed dual-V_t technique reduces the standby leakage current by approximately 235 times while offering enhanced delay characteristics as compared to a standard low threshold voltage implementation.

Keywords
Domino logic, low voltage swing, dual-V_t, low power, dynamic circuits.

1. INTRODUCTION
The application of aggressive circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity digital systems. The power consumed in high performance integrated circuits has increased to levels that impose a limiting factor on the system performance and functionality [1]. An effective method for reducing the power consumption is to lower the supply voltage. Lowering the supply voltage, however, also degrades the circuit speed due to the reduced current drive. Threshold voltage reduction has therefore emerged as a popular method accompanying the scaling of the supply voltage, permitting speed enhancements while maintaining the dynamic power consumption within acceptable levels [1].

This research was supported in part by the DARPA/ITO under AFRL Contract F29601-00-K-0182, grants from the New York State Office of Science, Technology & Academic Research to the Center for Advanced Technology – Electronic Imaging Systems and the Microelectronics Design Center, and by grants from Xerox Corporation, IBM Corporation, Intel Corporation, Lucent Technologies Corporation, Eastman Kodak Company, and Photon Vision Systems, Inc.

GLSVLSI '02, April 18-19, 2002, New York, New York, USA.

Compared to a typical static gate, a domino logic gate operates at a higher speed and occupies less area while implementing the same function [2]. However, deep submicrometer (DSM) domino logic circuits utilizing low power supply and threshold voltages have decreased noise margins [1] - [12]. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [1], [2], [7].

A low swing domino logic circuit without a keeper is compared to a standard full swing domino logic circuit without a keeper in terms of power and delay in [8]. However, noise issues have not been addressed. The circuit proposed in [8] is not effective in increasingly noisy high performance integrated circuits. A low swing domino logic circuit is proposed in this paper to reduce the power consumption without degrading the noise immunity. The low swing concept is also applied to the domino circuit keeper to further reduce the power consumption while enhancing speed. A simple and efficient circuit technique is proposed for a dual threshold voltage (dual-V_t) implementation of the proposed low swing circuits. Significant reductions in standby mode leakage power without incurring a delay penalty in the active mode are observed as compared to completely low threshold voltage (low-V_t) circuits.

Challenges in the design of reliable domino logic circuits together with active and standby power reduction techniques are reviewed in Section 2. The operation of the proposed low swing circuits and related simulation results characterizing the delay, power, and noise immunity are described in Section 3. The proposed dual-V_t low swing circuits and related simulation results are presented in Section 4. Finally some conclusions are offered in Section 5.

2. BACKGROUND
Domino logic circuit techniques have been extensively applied in recent high performance microprocessors due to the superior speed and area characteristics of domino circuits as compared to static CMOS circuits [3] - [6]. A standard domino logic circuit with a keeper (SDK) is shown in Fig. 1a. The voltage on the dynamic node can be degraded due to charge sharing, coupling noise, and/or charge leakage [2], [7]. Since the dynamic node is not actively driven, the state of the dynamic node cannot be recovered once the output is erroneously switched. Furthermore, threshold voltage scaling is extensively applied to domino logic circuits with reduced supply voltage in order to preserve the speed advantages. Hence, domino logic circuits are further sensitive to noise as the supply and threshold voltages are scaled [1], [7], [10], [11], [12]. The voltage transfer characteristics of SDK for different threshold voltages are shown in Fig. 1b. The decreased noise immunity of domino logic gates with reduced threshold voltages is clearly displayed. In addition to the increased noise sensitivity of domino logic circuits, the effect of coupling noise on reliable circuit operation increases with reduced feature sizes, increased

interconnect aspect ratios, and higher circuit operating frequencies [2], [7]. Error free operation of deep submicrometer domino logic circuits has, therefore, become a challenge. Low power domino logic techniques should address noise issues in modern high performance integrated circuits. A low swing domino logic circuit technique is proposed in this paper to reduce active power consumption without degrading noise immunity. The noise immunity characteristics of the proposed low swing circuits are evaluated in detail.

The low swing circuit technique has become an attractive method to reduce power in high performance integrated circuits. This technique has primarily been applied to I/O drivers and long interconnects [13]. However, static CMOS circuits driven by low swing input signals dissipate excessive static power while displaying poor delay characteristics. Specialized voltage interface circuits are therefore required to transfer signals between static CMOS circuits operating at different voltage levels [13]. The circuit delay and complexity of low swing static CMOS circuits increase while the power reduction attained by lowering the node voltages diminish due to these additional voltage interface circuits. Therefore, low swing circuit techniques have not been applied to modify the voltage swing of signals driving CMOS static gates. Low swing circuit techniques, however, can be effective in domino logic circuits. In a domino gate, the input signals are only applied to the NMOS transistors in the pull-down path, while a single pull-up PMOS transistor is driven by a separate clock signal. Therefore, a low swing signal that transitions between ground and a second sufficiently high voltage level to effectively turn on an NMOS transistor does not impose any functional or static power consumption problems in domino logic circuits. Low swing circuit techniques are shown in this paper to significantly reduce the power consumption of domino logic circuits.

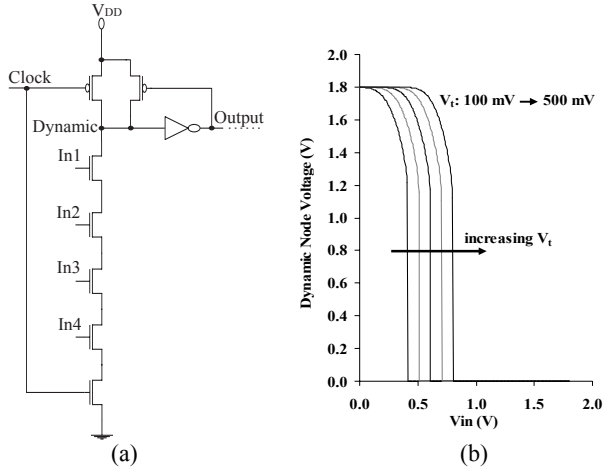

Fig. 1. Domino logic circuit and voltage transfer characteristics (VTC). (a) Standard domino logic circuit with a keeper (SDK). (b) VTC of SDK for various threshold voltages.

The dynamic power consumption dominates the total power consumption in an active circuit [10]. Alternatively, in an idle circuit, subthreshold leakage is the primary source of power consumption. Leakage power is an important issue primarily in portable systems with extended idle periods. Moreover, as constant field scaling and threshold voltage reduction trends continue, the leakage power is expected to exceed the dynamic power [1], [10], [14]. Therefore, leakage reduction techniques are required in low power systems.

The use of multiple threshold voltages in CMOS circuits (MTCMOS) has been proposed in [14] to reduce the subthreshold leakage currents. The circuit operation is divided into active and standby modes of operation. It has been shown that the leakage currents of a circuit can be reduced by placing the circuit into a controlled standby mode when the circuit is idle. However, MTCMOS degrades the circuit performance due to the additional high threshold voltage (high-V_t) switches between the logic circuit and the power supplies. A similar technique for leakage reduction is the dual-V_t technique. A dual-V_t circuit is divided into critical and non-critical paths, where high-V_t transistors are used on non-critical paths while low-V_t transistors are used on the critical paths [1], [10]. In dual-V_t circuits, the threshold voltages of existing transistors are modified (there is no need for additional high-V_t switches), and the high-V_t transistors are used only on the non-critical paths. Dual-V_t techniques, therefore, reduce the leakage power while incurring a smaller speed penalty as compared to the MTCMOS technique [10]. Application of dual-V_t techniques to domino logic is particularly attractive because of the fixed transitions in domino circuits during the precharge and evaluation phases [10]. Dual-V_t domino logic circuits have been proposed in [10] - [12]. In this paper, low swing domino logic circuits with controlled standby mode of operation are proposed. The dual threshold voltage concept is applied to the proposed low swing circuits. Significant reductions in standby leakage power and improved delay characteristics are observed as compared to standard low-V_t circuits.

3. LOW SWING DOMINO LOGIC

Low swing circuit techniques are applied to domino logic circuits in order to reduce the dynamic power. The voltage swings at the internal nodes of domino logic circuits are modified. The first proposed low swing domino circuit with a fully driven keeper is introduced in Section 3.1. A second proposed domino circuit reduces both the voltage swing at the output node and at the gate of the keeper. The operation of the second proposed low swing domino logic circuit with a weak keeper is described in Section 3.2. Simulation results are presented in Section 3.3.

3.1 Low Swing Domino Logic Circuit with Fully Driven Keeper (LSDFDK)

A four input AND gate implemented using the proposed low swing domino logic circuit technique, LSDFDK, is shown in Fig. 2a. LSDFDK reduces the voltage swing at the output node using the NMOS transistor (N6) as a pull-up. The output voltage swings between ground and V_{DD} - V_{tn}. The keeper (P2) is driven with a full swing signal for improved noise immunity.

3.2 Low Swing Domino Logic Circuit with Weakly Driven Keeper (LSDWDK)

A reduced keeper gate drive technique has been proposed in [9] to improve the delay and power characteristics of domino circuits while maintaining robustness against noise. This technique reduces the contention current by lowering the gate voltage of the keeper transistor. A second low swing domino logic circuit, proposed here and shown in Fig. 2b, utilizes a similar weak keeper. The weak keeper is critical in low swing circuits since the effects of the contention current on the evaluation delay and switching power are worse due to the reduced gate drive of the pull-down

network transistors. LSDWDK produces two different voltage swings. The output voltage swing is between ground and V_{DD} - V_{tn}. The gate voltage swing of the keeper (P2) is also modified using the PMOS transistor, P4. The gate voltage of P2 swings between $|V_{tp}|$ and V_{DD} (assuming $|V_{tp}| \leq V_{tn}$). This voltage swing reduces the contention current as compared to LSDFDK, thereby, lowering the evaluation delay and the dynamic power. The tradeoff is a reduced noise margin due to the weaker keeper transistor.

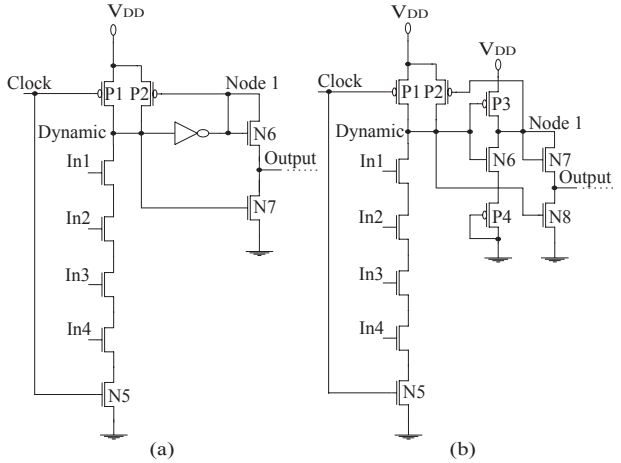

Fig. 2. The proposed low swing domino logic circuits. (a) Low Swing Domino Circuit with Fully Driven Keeper (LSDFDK). (b) Low Swing Domino Circuit with Weakly Driven Keeper (LSDWDK).

3.3 Simulation Results

The SDK, LSDFDK, and LSDWDK circuit techniques are evaluated for a three stage pipeline (see Fig. 3) composed of four input AND gates assuming a 0.18 µm CMOS technology. V_{tn} and $|V_{tp}|$ are assumed to be 200 mV. Each AND gate drives the four inputs of the following stage AND gate (the inputs of each AND gate are tied together and driven by the same signal). The third stage of the LSDFDK and LSDWDK pipelines is assumed to be a four input SDK AND gate to recover the full swing signal at the output of the pipeline. A 1 GHz clock signal with a 50% duty cycle is applied to each pipeline.

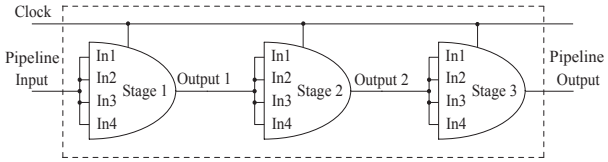

Fig. 3. Three stage pipeline of four input domino AND gates.

The size of the transistors in the pull-down network is critical for improving the evaluation delay of the domino logic circuits. The width of the keeper is minimum (W_{min}) for each circuit. The equivalent width of the pull-down network (PNEW) is a multiple of the keeper width and is varied to evaluate the delay, power, and noise immunity tradeoffs. The evaluation delay is calculated from 50% of the signal swing applied at the input of the first stage AND gate to 50% of the signal swing observed at the output of the third stage AND gate within each pipeline. To evaluate the noise immunity, the noise signal is assumed to be a square wave with a 450 ps duration. The maximum tolerable noise amplitude (MTNA) is defined as the signal amplitude at the input of the first stage AND gate that induces a 10% drop in the voltage at the dynamic node of the second stage AND gate. The pull-down NMOS transistors and the foot transistor (N5) are the same size. The active power, evaluation delay, and MTNA for each of these three domino circuits are shown in Fig. 4. Normalized results (for PNEW = 3) are listed in Table 1.

The simulation results show that the proposed low swing circuit technique is effective for lowering the power consumption of domino logic circuits. As shown in Fig. 4a, LSDFDK reduces the power consumption by up to 9.4% as compared to SDK with increasing PNEW. LSDWDK offers an additional power savings since the contention current is decreased by weakening the keeper (reduced current drive for the same size keeper as compared to both LSDFDK and SDK). LSDWDK reduces the power consumption by up to 12.4% as compared to SDK. The power savings of both LSDWDK and LSDFDK increase as compared to SDK with increasing PNEW. For all three circuits, the active power consumption increases as the size of the pull-down network increases.

Increased PNEW reduces the evaluation delay due to the increased current drive of the pull-down network. However, as shown in Fig 4b, both LSDWDK and LSDFDK sacrifice some speed for reduced power. As listed in Table 1, the evaluation delay is 46% higher for LSDFDK, and 38% higher for LSDWDK as compared to SDK (for PNEW = 3). LSDWDK offers enhanced delay characteristics as compared to LSDFDK due to the reduced contention current. As shown in Fig. 4b, the LSDWDK evaluation delay is up to 8.6% lower than the LSDFDK evaluation delay.

Table 1. Normalized dynamic power, evaluation delay, and MTNA (PNEW = 3).

	Power	Delay	MTNA
SDK	1.00	1.00	1.00
LSDFDK	0.91	1.46	1.03
LSDWDK	0.88	1.38	0.98

Another tradeoff for increased performance of each circuit with increasing PNEW is reduced noise immunity. As shown in Fig. 4c, the maximum tolerable noise amplitude decreases with increasing PNEW. LSDFDK not only lowers the power consumption but also displays higher noise immunity characteristics as compared to SDK. This behavior is due to the noise suppressing effect of the NMOS transistor providing the pull-up at the output (N6 in Fig. 2a) as the noise signal is transferred to the following gates. The MTNA of LSDFDK is up to 2.6% higher than the MTNA of SDK, and up to 10.9% higher than the MTNA of LSDWDK. Since the keeper of LSDWDK is weak, the MTNA of LSDWDK is 8.7% less than the MTNA of SDK for PNEW = 1.2. With increasing PNEW, the relative effect of the keeper on the noise immunity of the domino circuits is reduced. The difference between the MTNA of LSDWDK and SDK therefore is reduced to 2.1% from 8.7% as the PNEW increases from 1.2 to 3. Similarly, the MTNA advantages of LSDFDK as compared to SDK increases from 1.3% to 2.6% as the PNEW increases from 1.2 to

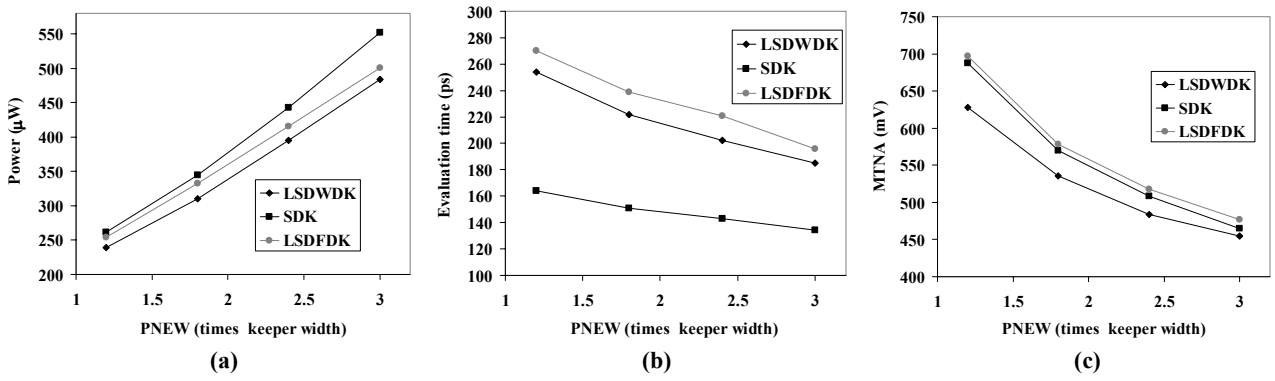

Fig. 4. Simulation results for different pull-down network transistor sizes for a constant keeper size (W_{keeper}= W_{min}). (a) Power versus pull-down network equivalent width (PNEW). (b) Evaluation time versus PNEW. (c) Maximum tolerable noise amplitude (MTNA) versus PNEW.

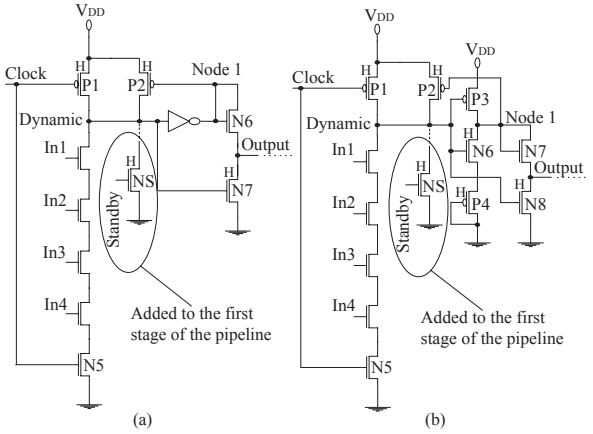

Fig. 5. Dual threshold voltage implementation of the proposed low swing domino circuits. (a) Dual-V_t LSDFDK. (b) Dual-V_t LSDWDK.

3. As shown in Fig. 4, with increasing PNEW, the power advantages of both LSDWDK and LSDFDK increase as compared to SDK while the evaluation times of all three circuits become more similar. Therefore, low swing domino logic circuits are expected to become more attractive as the pull-down network is scaled for higher performance.

4. DUAL THRESHOLD VOLTAGE DOMINO LOGIC

The proposed low swing domino circuits have been shown to be effective in reducing the power consumed during the active mode of operation. The standby mode power characteristics of the proposed circuits, however, are comparable to SDK. In this section, a circuit technique to reduce standby leakage current is proposed. The effects of the proposed technique on the active mode delay and power are also examined.

As described in [10] and [11], domino logic circuits offer an opportunity to apply dual-V_t techniques in order to reduce standby leakage currents without sacrificing active mode circuit performance. The critical signal transitions that determine the delay of a domino logic circuit occur along the evaluation path. Therefore, in dual-V_t domino circuits, all of the transistors that can switch during the evaluation phase, other than the keeper, have a low-V_t. Alternatively, the precharge phase transitions do not affect the performance of the domino logic circuits. Therefore, those transistors that are active during the precharge phase have a high-V_t. The proposed low swing dual-V_t domino circuits are shown in Fig. 5, with the high-V_t transistors labeled by "H" (the NMOS transistor inside the inverter shown in Fig. 5a also has a high-V_t).

The dual-V_t circuit technique described in [10] requires input signal gating of the first stage in each domino pipeline. This structure increases the circuit area and dynamic power while degrading the circuit performance due to the additional gates. An alternative dual-V_t technique has been proposed in [11] to reduce the power, delay, and area. Although the delay and area are reduced by the technique proposed in [11], the leakage power is higher as compared to the circuit proposed in [10]. This increased leakage current is primarily because the NMOS transistor inside the output inverter is not fully turned off and because the keeper has a low-V_t in the technique described in [11].

In this paper, a simple technique is proposed to implement the dual threshold voltage circuit (see Fig. 5). An NMOS switch, labeled as NS in Fig. 5, is added to the first stage of each proposed pipeline circuit. The operation of this transistor is controlled by a separate standby signal. During the active mode of operation, the standby signal is set low, NS is cut-off, and the proposed low swing circuits operate as explained in Section 3. During the standby mode of operation, the standby signal transitions high, turning on NS. The dynamic node of the first domino gate is discharged through NS. As a result, the output of the first stage gate transitions high, cutting off the keeper and causing the following gates to evaluate in a domino fashion. During the standby mode of operation, the clock signal is maintained high, turning off the pull-up transistor (P1) of each domino gate. After the node voltages settle to a steady state, all of the high-V_t transistors in the proposed circuits are strongly cut-off, reducing the leakage current. Note that this technique, requiring no additional gating on the input signals while strongly turning off all of the high-V_t transistors in the standby mode, is more power, delay, and area efficient than the techniques proposed in [10] and [11].

The circuits shown in Fig. 5 have been evaluated for both active and standby modes of operation. The effects of modifying the threshold voltage distribution of the transistors on the power and performance characteristics of the circuits are examined. LSDFDK and LSDWDK are evaluated for high threshold voltages

Table 2. Standby mode leakage power, active mode total power, evaluation delay, and MTNA for different threshold voltage distributions.

	Leakage Power (nW)		Active Power (μW)		Evaluation Delay (ps)		MTNA (mV)	
V_t Distribution	***LSDWDK***	***LSDFDK***	***LSDWDK***	***LSDFDK***	***LSDWDK***	***LSDFDK***	***LSDWDK***	***LSDFDK***
Low-V_t	180.80	264.70	402.3	413.0	216	231	488	520
Dual-V_t	0.76	1.12	395.7	404.4	212	229	467	513
High-V_t	0.73	1.10	341.3	348.4	355	400	685	732

only, low threshold voltages only, and dual threshold voltages. Same size transistors and circuit configurations are used for all three threshold voltage distributions. The low-V_t is assumed to be 200 mV and the high-V_t is assumed to be 400 mV. The PNEW is 2.4. The standby mode leakage power, the active mode total power, and the evaluation delay of the proposed low swing circuits are listed in Table 2.

These results demonstrate that the dual threshold voltage technique is a powerful method to simultaneously reduce the standby power, active mode total power, and the evaluation delay of the proposed low swing domino logic circuits as compared to standard low-V_t circuits. As listed in Table 2, the standby power of the dual-V_t LSDWDK is 237 times smaller than in low-V_t LSDWDK. Similarly, dual-V_t LSDFDK consumes 235 times less leakage power as compared to low-V_t LSDFDK operating in the standby mode. Another advantage of the proposed dual-V_t circuits is the reduced active mode total power. This behavior is primarily caused by the weaker high-V_t pull-up transistors, P1 and P2 (reduced contention current). As listed in Table 2, low-V_t LSDWDK consumes 1.7% more active power than dual-V_t LSDWDK. Similarly, the active power consumption of the low-V_t LSDFDK is 2.1% higher than the power consumption of the dual-V_t LSDFDK.

Another advantage of the dual-V_t implementation is reduced evaluation delay. The dual-V_t technique improves slightly the evaluation time of both LSDWDK and LSDFDK as compared to the low-V_t circuits. This behavior is again due to the reduced contention current due to the weaker high-V_t pull-up transistors.

The primary drawback of the dual-V_t circuits as compared to the low-V_t circuits is reduced noise immunity. As listed in Table 2, MTNA is reduced by 4.3% (2.3%) for dual-V_t LSDWDK (LSDFDK) as compared to low-V_t LSDWDK (LSDFDK). This behavior is primarily caused by the reduced current drive of the high-V_t keeper.

The high-V_t circuits improve both the active and standby power characteristics as compared to the low-V_t and dual-V_t circuits. High-V_t LSDWDK (LSDFDK) offers an approximately 13.7% (13.8%) savings in active power as compared to the dual-V_t LSDWDK (LSDFDK). The difference between the leakage power of the dual-V_t implementation and the high-V_t implementation of LSDWDK (LSDFDK) is 3.8% (2.5%). Another significant advantage of the high-V_t circuits is increased noise immunity. As listed in Table 2, high-V_t LSDWDK (LSDFDK) increases the MTNA by 46.7% (42.7%) as compared to dual-V_t LSDWDK (LSDFDK). This significant power savings and high noise immunity, however, comes with an increased evaluation delay due to the reduced current drive of the evaluation path transistors. The high-V_t LSDWDK (LSDFDK) increases the evaluation delay by 67.5% (74.7%) as compared to the dual-V_t LSDWDK (LSDFDK).

5. CONCLUSIONS

Low swing domino logic circuits with weakly driven keepers and fully driven keepers have been proposed for increased power savings and reliable operation in an increasingly noisy on-chip environment. The proposed low swing domino logic circuits can significantly reduce active power consumption without degrading noise immunity. LSDFDK is shown to consume up to 9.4% less active power and tolerate up to 2.6% more noise as compared to SDK. The active power is further reduced by weakening the keeper which also improves the evaluation delay due to reduced contention current. LSDWDK is shown to reduce the active power consumption by up to 12.4% as compared to SDK while improving the evaluation delay by up to 8.6% as compared to LSDFDK.

A circuit technique has been proposed for controlled standby mode circuit operation in order to reduce subthreshold leakage current. The dual-V_t circuit technique has been applied to the proposed low swing circuits. The standby leakage power of LSDWDK (LSDFDK) is reduced 237 (235) times for a dual-V_t circuit as compared to a low-V_t circuit. Moreover, the proposed dual-V_t technique reduces the active power consumption of LSDWDK (LSDFDK) by 1.6% (2.1%) as compared to a low-V_t circuit without incurring a delay penalty.

Dual-V_t LSDWDK is the proper choice for those applications in which power and speed are both important because of the low active and standby power consumption and relatively low evaluation delay. High-V_t LSDWDK is proposed for those applications in which power and noise immunity are the primary concerns and speed is a secondary issue. High-V_t LSDWDK further reduces the leakage power by another 3.8% and the active power by another 13.7% while improving the noise immunity by 46.7% as compared to dual-V_t LSDWDK.

LSDFDK offers superior MTNA as compared to both LSDWDK and SDK, and is therefore preferable if high noise immunity is the primary design criterion.

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