A Test Design Method for Floating Gate Defects (FGD) in Analog Integrated Circuits

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Abstract

A unified approach to fault simulation for FGDs is introduced. Instead of a direct fault simulation, the proposed approach calculates indirectly from the simulator output the sets of undetectable values of the trapped charge on the floating gate transistor. It covers all potential gate charges of an FGD at one or more transistors and allows the application of conventional circuit simulators for simulating DC, AC and transient test.

Based on this fault simulation, a test design methodology is presented that can determine all test sets that detect all FGDs for all possible values of gate charge.

1 Introduction

The trend towards integration of digital and analog components on the same chip has spawned growing attention to the test needs of mixed-signal ICs. For an increasing number of devices, their price is presently dominated by the cost of production testing. A major part of these testing costs are due to performance test of analog components. Defect-oriented test can supplement functional test in order to increase reliability, and it may even substitute functional test where functional test is impracticable or too expensive.

In this work, we propose a defect-oriented test design methodology for integrated CMOS analog circuits, that can handle *floating gate defects* (FGDs), which are sometimes also called "open-gate faults". In comparison to common fault models for direct path opens and shorts, state-of-the-art fault models for FGDs are very complex [1–3], which poses a challenge for efficient fault simulation, test selection, and validation of test quality.

FGDs make fault simulation and test design much more difficult than direct-path opens and shorts. This is due to two reasons:

1. *The intrinsic charge q trapped on the floating gate* has a dominant influence on test measurements. The value of this charge is however unknown, and various bounds and distributions of gate potential v_g have been assumed in the literature [2, 4–6]. Making these assumptions may be more influential to the outcome of the test than the fault itself.
2. Conventional circuit simulator programs do not allow simulation of an FGD for a given value of the trapped charge, because the standard evaluation programs for transistor models calculate the gate charge as a result of simulation, and will not accept it as input.

In this work, we present a new approach to test design with regard to floating gate faults in analog circuits. Key features introduced by our approach are:

1. No estimations of distributions of fault parameter q is necessary.
2. Application of conventional circuit simulator programs
3. Full use of standard transistor models like BSIM3 without extra modeling effort
4. Simulation of multiple floating gate (MFG) defects
5. DC, AC and transient test are possible.
6. Measurement error and process fluctuation are considered.
7. All alternative test sets of 100% fault coverage are provided for an interactive decision.

In Section 2, we give an overview of the state of the art in open-gate fault modeling and simulation. Section 3 presents the test design method for FGDs. In Section 4, we propose a new method for fault simulation of FGDs. Results for an example operational amplifier and a biquad filter are given in Section 5.

2 Fault model for FGDs

A floating gate defect occurs in a circuit, if the gates of one or more MOS transistors become disconnected from their controlling input and lose their ohmic electrical connection to the rest of the circuit. Today, the main defect cause of FGDs are missing vias [6]. Other causes like photolithographic defects are considered to be less probable [7], but

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will be included in our model, too. An FGD usually affects two or more transistors as a group, because transistors often share a common gate like in current mirrors or in logic gates. This is called a *multiple floating gate defect* (MFGD).

Figure 1 shows a schematic fragment of a circuit with a typical FGD. The common gate node of an n-channel and a p-channel type transistor is connected to the rest of the circuit only via capacitances. Some capacitors were included to represent capacitive influences to the floating node. These include primarily C_{gs}, C_{gd}, and C_{gb}, as well as overlap and fringing capacitances C_{gso} and C_{gdo}. Apart from the transistor itself, parasitic capacitances C_m and C_{pb} model capacitive influences on the gate wire coming from other parts of the circuit.

The charge q captured at the floating node is distributed over these capacitances and cannot flow off the node. The sum of the charges on these capacitances is therefore equal to q and constant [1]:

$$q = \sum_i q_i = \text{const.} \tag{1}$$

This charge has a large influence on the operating point of the affected transistors, including the gate potential v_g. The operating point in turn comprises the potentials on the terminals of the affected transistors and therefore determines the distribution of q over the capacitances. Moreover, most of these capacitances are very bias-dependent, i.e. their values change with the operating point.

It is impossible to calculate the operating point of such a circuit for a given value of q by means of a single conventional circuit simulation, because Eq. (1) is not part of Kirchhoff's laws that modified nodal analysis is based on. In other words, these simulators do not provide a way to specify the node charge sum q, but instead calculate it as a result.

This problem seemed to inhibit test design for FGDs and so it was approached directly in most previous work by taking transistor model equations and solving them for the gate-source voltage in order to make q an input and v_g

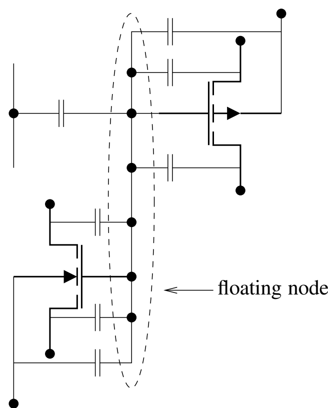

Figure 1: Floating gate fault model on the example of a pair of n-/p-channel transistors that is likely in digital circuits.

a result of their evaluation [1, 3, 8, 9]. The parasitic capacitances C_m and C_{pb} were included into the transistor models. A common drawback of approaches based on model reformulation is that they are restricted to the case of an FGD at a single transistor, because Eq. (1) must hold at circuit level for MFGDs. Moreover, to keep the effort of implementing a new transistor model manageable, the MOSFET capacitance modeling had to be simplified significantly, neglecting for instance bias-dependent capacitances, short-channel effects and channel charge partitioning. Another limitation of many approaches is the general assumption of zero bulk-source voltage, which doesn't hold for many circuits [1, 3, 9].

In [10] and [6], an FGD fault model is integrated with a circuit specific analysis in order to quickly estimate fault coverage of I_{DDQ} and logic tests in combinational circuits.

Other approaches tried to circumvent the simulation problem by using the gate potential v_g as a fault parameter instead of q for fault coverage analysis [11]. The faulty circuit can be simulated for a given value of v_g. To restrict the range of v_g, some authors introduced an interval I_v, containing the values of the gate potential that are most probable to occur at the floating gate. If the test detects the fault for $v_g \in I_v$, it is said to detect the fault [4,6]. A drawback of using v_g as a fault parameter is that due to its inconsistence with the constant charge fault model, such a fault coverage can be reasonably defined only for one test, but not for a set of tests. This is a strong limitation, because a combination of tests may significantly increase fault coverage. Moreover, using a single interval I_v is problematic, because the gate potential range is different for each transistor in a circuit and for each operating point of the circuit. In [2], the size of I_v varied by more than a factor of 10 between identical devices being processed by two different manufacturers. Even for a single process, I_v may change over time. As we will show, the choice of I_v has a strong influence on a fault coverage estimation based on it. Therefore it is extremely difficult or even impossible to determine an interval I_v for a given process and *device under test* (DUT) that yields a reasonable estimation of fault coverage.

In some previous approaches, the physical origin of the open-gate fault was assumed to be a break at an unknown position at the poly line. Under this assumption, the poly-bulk capacitance C_{pb} depends on the position of the break and is treated as an unknown fault parameter in the model. We can consider this by repeating the fault analysis for a discrete set of values for C_{pb} like in [8, 9, 11]. On the other hand, the most likely cause of floating gate defects are open vias in higher layers of metal. Therefore we propose to produce the fault list with respect to the vias like Konuk in [6] and to extract the value of C_{pb} from the layout then. It is hence straightforward to focus on q as the only unknown fault parameter in the following and to treat C_{pb} as a known constant.

In the following we will show that, although simulation of an FGD *for a given value of* q still remains to be enabled,

it is not a prerequisite for test design. We will introduce a fault coverage analysis and test design methodology for FGDs that can be performed by means of a conventional circuit simulator using the full BSIM3 transistor model [12].

3 Test design

There is a fault list F of possibly faulty transistors in the DUT, including all MFGDs. Each fault is assigned a fault index that we will denote ϕ in the following. Test measurements can be any scalar values, which includes DC measurements, AC measurements like phase margin, or transient measurements, e.g. slew rate. A list T of possible tests is built, and each test is assigned a test index τ. For example, $\tau = 4$ may denote the test "Measure DC gain in normal operation."

Each test τ results in a measurement value $m_{\phi,\tau}$ of fault ϕ (see Fig. 2). For FGDs, such a measurement depends on the unknown charge sum q, and will therefore be denoted $m_{\phi,\tau}(q)$ in the following.

If the FGD will make the test measurements deviate sufficiently far from their fault-free values during the test of a faulty device, then the fault will be detected. But for some values of q, the test measurement will be inside the acceptance region A_τ around the fault free measurement. In this case, the faulty circuit would pass the test (see Fig. 3).

The acceptance region is given by the test tolerance limits and can be set arbitrarily. Usually, $\pm 3\sigma$ bounds with regard to measurement error and process fluctuation will be sufficient for A_τ and can be determined automatically. The set of charge values q that make fault ϕ escape test τ is then the *set of undetectable charge values*

$$\mathrm{Sndq}_{\phi,\tau} = \{q \mid m_{\phi,\tau}(q) \in A_\tau\} \ . \tag{2}$$

The goal of test design is to find an optimum set of tests $G \subseteq T$ that detects all faults. Figure 4 shows an example of three tests. The Sndq determine, which test will detect the fault for which values of q. For example, if a FGD occurs with a charge $q = q^*$, this fault will be detected by tests 2 and 3, but not by test 1 because $q^* \in \mathrm{Sndq}_{\phi,1}$. Although there is no single test that detects the fault for all values of q, we know that either test 1 or test 2 will detect it, because their sets of undetectable charge values are disjoint: $\mathrm{Sndq}_{\phi,1} \cap \mathrm{Sndq}_{\phi,2} = \varnothing$. Therefore we could reduce the test set by removing test 3. Alternatively, we could remove test 1, but not test 2, because $\mathrm{Sndq}_{\phi,1} \cap \mathrm{Sndq}_{\phi,3} \neq \varnothing$.

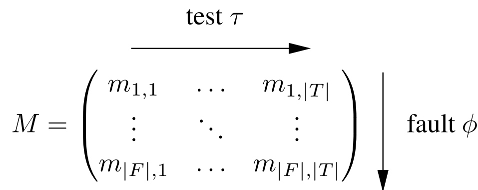

Figure 2: The test measurement matrix M.

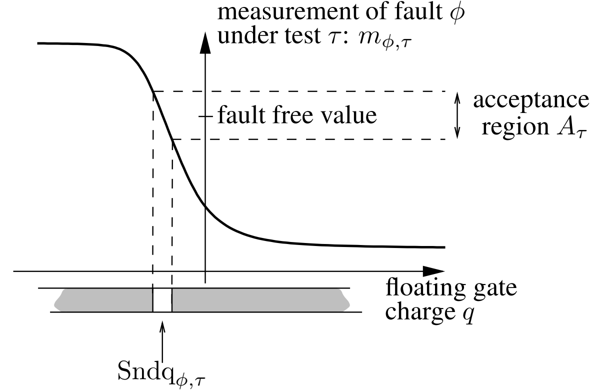

Figure 3: The set of undetectable charge values Sndq for a fault ϕ under test τ.

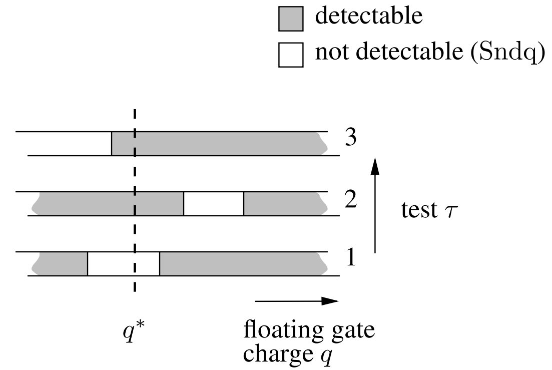

Figure 4: Sets of undetectable charge values for one fault and three tests $\tau \in \{1, 2, 3\}$.

A set G of tests will hence detect a fault ϕ for all values of charge $q \in \mathbb{R}$, if

$$\bigcap_{\tau \in G} \mathrm{Sndq}_{\phi,\tau} \stackrel{!}{=} \varnothing \ , \tag{3}$$

and will detect all faults, if

$$\forall_{\phi \in F} \bigcap_{\tau \in G} \mathrm{Sndq}_{\phi,\tau} \stackrel{!}{=} \varnothing \ . \tag{4}$$

In the following, we will use the binary test selection vector g to denote, which tests are selected. The first bit g_1 of g for example corresponds to the first test $\tau = 1$ and is true if this test is in the set G of selected tests. For example, $g = (0, 1, 1) \Leftrightarrow G = \{2, 3\}$. The boolean detection function $d_\phi(g)$ denotes if fault ϕ is detected by test set G according to Eq. (3). For instance, the detection function is

$$d_\phi(g) = g_1 \cdot g_2 + g_2 \cdot g_3 \tag{5}$$

in the example of Fig. 4. The set of undetectable charge values is usually an interval like in Fig. 3 and construction of the detection function d_ϕ based on interval limits is straightforward then. For other cases, a sub-range coverage matrix like in [11] is used.

Please note this important difference between FGDs and direct-path opens and shorts. Those faults are usually modeled with a resistor of a certain value, e.g. 1Ω for shorts and $10\text{M}\Omega$ for opens. Then it is possible to build a 1:1-relation between a fault and a test that detects this fault in a fault/test detection matrix. The detection function for a direct-path fault could be for example $d_\phi(g) = g_2 + g_5 + g_9$. This is different for an FGD, because there often is no single test that can detect it, but only a combination of tests (Eq.(5)).

According to Eq. (4), a test selection vector g will detect all faults, if the detection functions $d_\phi(g)$ are true for all faults ϕ. In the following, we will use the total detection function

$$d(g) :\Leftrightarrow \bigwedge_{\phi \in F} d_\phi(g) \tag{6}$$

to denote this. Test selection for full fault coverage is then performed by finding vectors g that make the total detection function $d(g)$ true. This is known as a satisfiability problem and can be solved e.g. by SIS [13]. Among these solutions we may choose with regard to e.g. shortest testing time.

4 Fault simulation

As already explained in Section 2, it is usually impossible to simulate the faulty DUT for a given value of q by conventional circuit simulation. Enabling this simulation was the goal of some previous work (see Section 2). In contrast to that, the methodology presented here is based on the idea, that we do not need to know the measurement result of the faulty circuit as a function of the charge, $m_{\phi,\tau}(q)$, if we can find another way to determine $\mathrm{Sndq}_{\phi,\tau}$.

For each fault ϕ and each test τ, we determine the measurement value $m_{\phi,\tau}(v_g)$ and the floating gate charge $q_{\phi,\tau}(v_g)$ by simulating each faulty circuit for a reasonable large range of the floating gate voltage v_g (see Fig. 5). The function $m_{\phi,\tau}(v_g)$ is extracted directly from the simulation results. The charge $q_{\phi,\tau}(v_g)$ comprises the charge sums of all capacitances of the transistor model, including intrinsic gate charge, charge on overlap and fringing capacitances, and the charge on capacitors optionally included to model poly-bulk capacitance $\mathrm{C_{pb}}$ and crossing metal wires $\mathrm{C_m}$. In the case of a MFGD, q is the sum of these charges at all affected transistors. All these charges can be read easily from the simulator output and are summed up to yield $q_{\phi,\tau}(v_g)$.

In the case of DC measurements, a voltage source at the floating node is used to sweep v_g. For AC and transient measurements, most simulators provide commands to set node voltages of the initial operating point, similar to SPICE's .nodeset command. Using a DC voltage source to set v_g for AC measurements is wrong, because the floating gate was connected to small-signal ground then. In the examples of Section 5 and in Figure 5, we used $v_g \in [-3\mathrm{V_{DD}}, 3\mathrm{V_{DD}}]$.

Figure 5 shows an example of a measurement of i_{DD} for one FGD in an example circuit. For fault-free circuits, i_{DD}

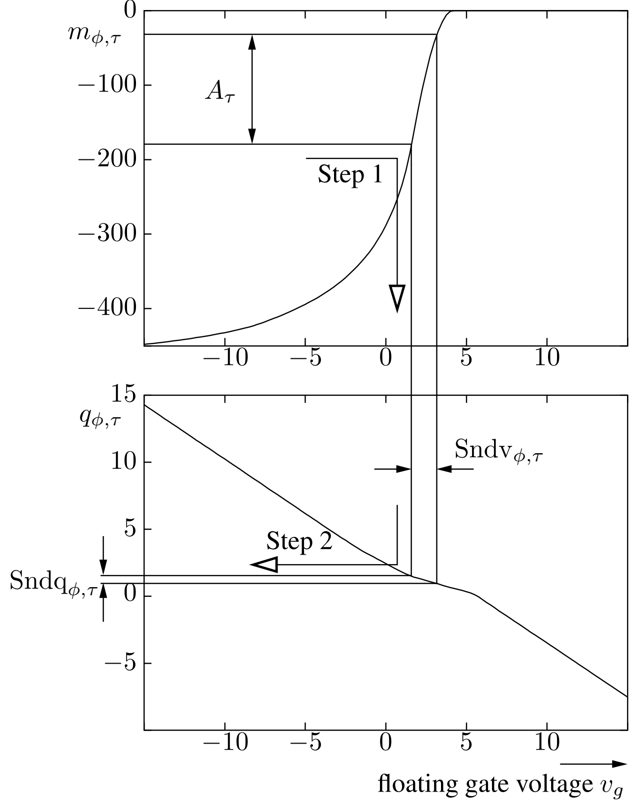

Figure 5: Calculation of $\mathrm{Sndq}_{\phi,\tau}$. Measurement $m_{\phi,\tau}$ is i_{DD} [μA], q is gate charge [pC] at a floating gate in an operational amplifier.

is varying in a $\pm 3\sigma$-range $A_\tau = [-180\mu\text{A}, -30\mu\text{A}]$ due to usual process fluctuations, measurement error, or imprecise test stimulus generation.

In a first step, the set of undetectable gate voltages of fault ϕ under test τ

$$\mathrm{Sndv}_{\phi,\tau} = \left\{ v_g \;\middle|\; m_{\phi,\tau}(v_g) \in A_\tau \right\} \tag{7}$$

is calculated (see Fig. 5) by mapping the acceptance region of fault-free measurements A_τ onto the range of v_g. $\mathrm{Sndv}_{\phi,\tau}$ is the interval of values of the gate node voltage v_g, that lead to measurement values that will make fault ϕ pass test τ. In a second step, the set of undetectable charge values of fault ϕ under test τ

$$\mathrm{Sndq}_{\phi,\tau} = \left\{ q_{\phi,\tau}(v_g) \;\middle|\; v_g \in \mathrm{Sndv}_{\phi,\tau} \right\} \tag{8}$$

is derived by mapping the set of undetectable gate voltages Sndv onto the range of gate charges q (see Fig. 5).

It is important to note that varying the voltage at the floating node for fault simulation does in no way imply, that the fault model used here equated an FGD with a constant gate voltage. One specific FGD may show very different gate voltages under different operating conditions, i.e. for different DC tests or during a transient measurement. The simulation method proposed here is useful to calculate the set of undetectable charge values Sndq by means of a standard circuit simulator that doesn't provide a way to simulate

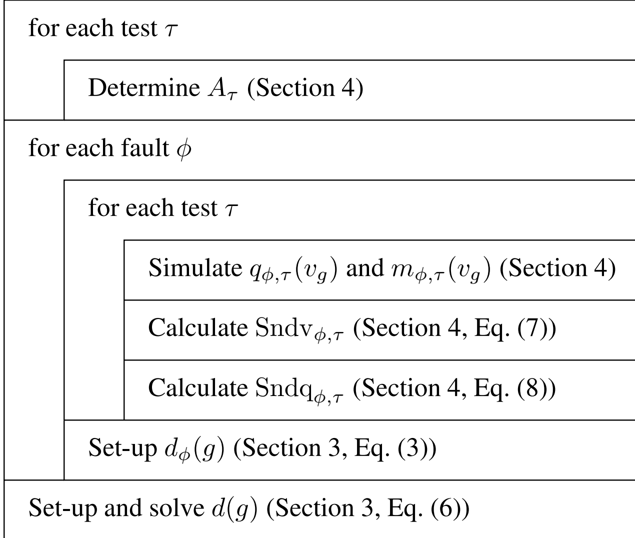

Figure 6: The test design method

the faulty DUT for a given q and therefore impedes a direct calculation of Sndq according to Fig. 3.

The advantages of our simulation method are: State-of-the-art transistor models can be applied and need not be reversed and approximated, existing simulator programs can be used even for MFG faults, and all capacitive influences are included at no extra cost.

Figure 6 shows, how the concepts presented in this section and of test selection presented in Section 3 are combined in a test design method.

5 Simulation Results

5.1 DC Test of an operational amplifier

The operational amplifier shown in Figure 7 is used as a first example circuit. For testing, we consider the power-down control of this operational amplifier, v_{pd}, as a possible test input. In normal operation of the circuit, $v_{\text{pd}} = 0\,\text{V}$ and the bias current source is connected to the operational amplifier. In power-down mode, $v_{\text{pd}} = \text{V}_{\text{DD}}$, and the bias current is disconnected, switching the operational amplifier off.

We apply a set of voltage levels between 0 V and V_{DD} at v_{pd} for testing, in order to modify the bias current of the operational amplifier. This is advantageous for some reasons:

1. Reduced bias current will drive the DUT into modes of operation that cannot be set up otherwise. These operating conditions are useless for normal operation of the circuit, but during test they may reveal important information about circuit faults.
2. Modifying the driving circuit of the v_{pd} signal in order to generate other signal levels than 0 V and V_{DD} will not degrade the performance of the operational amplifier in normal operation. This is important for built-in self test (BIST) application.

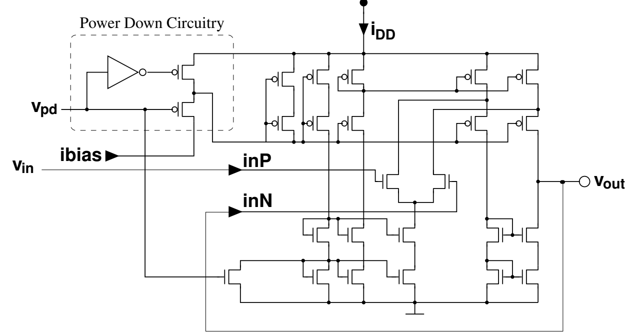

Figure 7: Folded-cascode operational amplifier in voltage follower configuration

Test τ	v_{in}	v_{pd}	*measurement*
4	2 V	0 V	v_{out}
20	2 V	2 V	v_{out}
5	2 V	0 V	i_{DD}
14	5 V	1 V	v_{out}
20	2 V	2 V	v_{out}

Table 1: Two possible test sets $G_1 = \{4, 20\}$ and $G_2 = \{5, 14, 20\}$ out of 560 that would detect all FGDs at the operational amplifier.

The test configuration of the operational amplifier example is a voltage follower. Test input is the input voltage v_{in} of this circuit. Measurements can be performed on v_{out} and i_{DD}. There are 6 MFGDs (the current mirrors of the circuit), and two single transistor FGDs (the input differential pair), together 8 FGDs (6 n-channel, 2 p-channel). Please note that there are more MFGDs than single transistor FGDs here, and that 12 out of 22 transistors have non-zero bulk-source voltage.

The computational cost for the complete fault simulation of all faults and tests was less than 5 minutes on a network of 15 PCs. Setting up the total detection function $d(g)$ and solving the satisfiability problem in SIS took less than a second. The solution consisted of 560 test sets that would detect all considered FGDs when applied. The size of the test sets ranged from 2 to 5. Two of them are shown in Table 1.

For comparison, we performed a test design on the same circuit with the modification that we now use intervals I_v of gate potential v_g to estimate fault coverage. The same simulation results as above were used to evaluate for each single test τ, if it detects an open-gate fault for all values of $v_g \in \mathrm{I}_v$. A test set was validated for five different I_v used in the literature [2, 5, 6]. The fault coverages that were calculated are collected in Table 2. This comparison shows, that the estimated fault coverage depends heavily on the chosen I_v and may vary between 0 and 100%. Since the fault coverage is influenced by assumptions on the unknown I_v in

I_v	$[-1, 1]$	$[0.38, 2.3]$	$[0.77, 0.89]$	$[-4, 2.3]$	$[0, 5]$
f.c.	100%	50%	100%	0%	25%

Table 2: Influence of gate potential ranges I_v [V] on fault coverage estimation based on v_g. The fault coverage in the charge-based fault model is 100%.

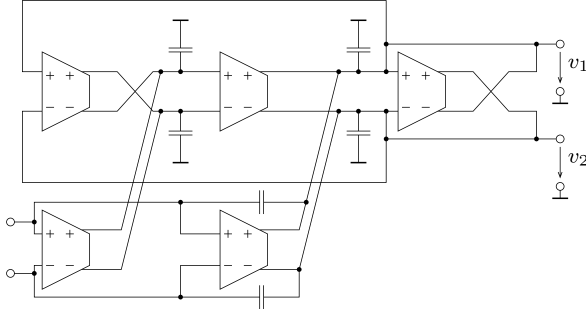

Figure 8: Second order biquad filter

such a strong way, an estimation based on v_g is difficult or impossible.

In contrast to that, our approach does not rely on estimated distributions of gate charge or gate potential, but tries to detect all faults for gate charge $q \in \mathbb{R}$, where q is constant for a fault during all tests.

5.2 AC test of a biquad filter

To show the feasibility of our approach for AC measurements, a CMOS biquad filter circuit (similar to the one in Fig. 8) consisting of 39 transistors was analyzed for its testability with regard to open-gate faults as a second example. Available measurements are the magnitude of two output voltages at the differential output at 20MHz (AC analysis), and quiescent supply current i_{DD} (DC analysis). For testing, two bias currents of the filter (ibias_1 and ibias_2) can be set to 0mA, 0.1mA or 0.2mA. Ten possible open-gate faults were located at two current mirror banks, four current mirrors, and four inverters. Six faults were MFGDs, and two of these affected as many as seven transistors in a group.

The test design resulted in a set of 111 possible test combinations, that would detect all FGDs of this circuit. All test sets had a size of two, i.e. there is no single test that can detect all faults, but two tests are sufficient. Two examples of these test sets are shown in Table 3.

Test τ	ibias_1	ibias_2	*measurement*
17	0.1mA	0.2mA	i_{DD}(DC)
26	0.2mA	0.2mA	i_{DD}(DC)
1	0mA	0mA	v_1 (20MHz)
19	0.2mA	0mA	v_1 (20MHz)

Table 3: Two possible test sets out of 111 that would detect all FGDs at the biquad filter.

6 Conclusion

We presented a new method for fault simulation of floating gate defects. Our approach allows to use conventional circuit simulators with standard transistor models for fault simulation of the full FGD fault model. A fault coverage analysis method determines all test configurations that provide 100% fault coverage.

References

[1] Michel Renovell and Gaston Cambon, "Electrical analysis and modeling of floating-gate fault," *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, vol. 11, no. 11, pp. 1450–1458, Nov. 1992.

[2] S. Johnson, "Residual charge on the faulty floating gate MOS transistor," in *IEEE International Test Conference (ITC)*, 1994, pp. 555–561.

[3] Anna M. Brosa and Joan Figueras, "Characterization of floating gate defects in analog cells," *Journal of Electronic Testing*, vol. 14, pp. 23–31, 1999.

[4] A. K. B. A'ain, A. H. Bratt, and A. P. Dorey, "Exposing floating gate defects in analogue CMOS circuits by power supply voltage control testing technique," in *IEEE Int. Conf. on VLSI Design*, Jan. 1995, pp. 239–242.

[5] M. Renovell, A. Ivanov, Y. Bertrand, F. Azaïs, and S. Rafiq, "Optimal conditions for boolean and current detection of floating gate faults," in *IEEE International Test Conference (ITC)*, 1999, pp. 477–486.

[6] Haluk Konuk, "Voltage- and current-based fault simulation for interconnect open defects," *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, vol. 18, no. 12, pp. 1768–1779, Dec. 1999.

[7] J. A. Prieto, A. Rueda, I. Grout, E. Peralías, J. L. Huertas, and A. M. D. Richardson, "An approach to realistic fault prediction and layout design for testability in analog circuits," in *Design, Automation and Test in Europe (DATE)*, 1998.

[8] V. H. Champac, A. Rubio, and J. Figueras, "Electrical model of the floating gate defect in CMOS ICs: Implications on I_{DDQ} testing," *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, vol. 13, no. 3, Mar. 1994.

[9] A. Ivanov, S. Rafiq, M. Renovell, F. Azaïs, and Y. Bertrand, "On the detectability of CMOS floating gate transistor faults," *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, vol. 20, no. 1, pp. 116–128, Jan. 2001.

[10] Haluk Konuk, F. Joel Ferguson, and Tracy Larrabee, "Charge-based fault simulation for CMOS network breaks," *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, vol. 15, no. 12, pp. 1555–1567, Dec. 1996.

[11] A. M. Brosa and J. Figueras, "On maximizing the coverage of catastrophic and parametric faults," *Journal of Electronic Testing*, vol. 16, no. 3, pp. 251–258, June 2000.

[12] Department of Electrical Engineering, University of California at Berkeley, http://www-device.EECS.Berkeley.EDU/~bsim3/, *BSIM3v3.2.2 MOSFET Model: Users' Manual*, 1999.

[13] Ellen M. Sentovich, Kanwar Jit Singh, Luciano Lavagno, Cho Moon, Rajeev Murgai, Alexander Saldanha, Hamid Savoj, Paul R. Stephan, Robert K. Brayton, and Alberto Sangiovanni-Vincentelli, "SIS: A system for sequential circuit synthesis," Memorandum UCB/ERL M92/41, Electronics Research Laboratory, University of California, Berkeley, CA 94720, May 1992.