Analog Design for Reuse - Case Study: Very Low-voltage $\Delta\Sigma$ Modulator

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Abstract

This paper presents the complete design methodology of a very low-voltage $\Delta\Sigma$ third-order modulator from high-level specifications down to layout. Behavioral models taking into account cell non-idealities are developed and used to map performance specifications to lower levels. Emphasis has been made on eventual design reuse through design plans and layout templates in a layout-oriented circuit design approach. The modulator has been designed for two different technologies demonstrating the suitability of the methodology for very high performance mixed-signal circuits. Moreover, the same design knowledge has been successfully reused in another fourth-order modulator.

1. Introduction

The complexity of IC's being designed nowadays is continuously increasing as advances in process technology make it possible to create mixed-signal integrated SoC designs. As SoC's are becoming larger, the only way to efficiently design such dense SoC's is by embedding IP blocks. Ideally, these cores should be reusable, pre-characterized and pre-verified. IC foundries and IP providers offer layouts for commonly-used blocks. The problem is that the analog space cannot be fully covered by any finite library of blocks. An alternative approach consists of developing specific block synthesis tools [1] [2] which couple optimization with a knowledge database continuously updated and reused by the IP provider. Block generator development, however, takes a considerable effort and time. It must be justified by an extensive use of the generator. Design reuse based on an original *working* design has been investigated both through qualitative reasoning [3] and analog synthesis [4]. The above approaches treat only the sizing phase of the design, the layout is considered as a separate phase handled with dedicated tools.

Yet the most efficient way to generate reusable IP's is by incorporating appropriate information, concerning both circuit design and layout, in the original design methodology. This ensures a first-pass silicon since the original design considerations of the original *working* circuit are all respected. This is made possible through the use of design plans which include a close interaction between sizing and layout templates [5].

In this work, this approach is introduced through a demanding application in order to show its generality and suitability even to state of the art designs. The complete design experience of a very low-voltage (1V) third-order $\Delta\Sigma$ modulator [6] is presented. Switched-capacitor (SC) operation in standard CMOS has been achieved using a special low-voltage *bootstrapped* switch that allows rail-to-rail signal switching. A modified low-voltage fully-differential opamp has been employed [7]. The circuit shows the feasibility of very low-voltage high performance circuits using common SC techniques.

While the tools supporting the methodology have been presented by the authors [5], [8] , [9], as well as circuit results [6], [7], so far no paper has been published to present an overall view of the design methodology. The use of hierarchical sizing and procedural layout have enabled to explore a large design space in the presence of layout parasitics. The developed behavioral models, sizing procedures and layout templates have also allowed to resynthesize the same design in another technology. Moreover, they have allowed to redesign a fourth-order modulator with a different topology based on the same building blocks.

2. Methodology and Tools

The modulator design process contains four major steps:

1. **High-Level Synthesis**: Starting from the performance goal, the most suitable modulator architecture and oversampling ratio (OSR) are chosen followed by modulator coefficient determination. During this phase usually a large number of simulations are done

on the functional level where ideal models are used for the building blocks.

2. **Performance Parameter Mapping**: Now that the architecture has been fixed, models that describe the non-ideal behavior of the modulator building blocks are built and used to investigate the feasibility of the chosen architecture on the circuit level. This also leads to performance parameter mapping from the system level to the building blocks transistor level.

3. **Low-Level Synthesis**: In this step each block is designed according to the performance specifications determined in the previous step. Synthesis of the building blocks is done using the CAD tools and methodology described in [5]. For each block:

   - The complete design procedure is incorporated in the knowledge-based sizing tool COMDIAC [9]. Hierarchical sizing facilitates this step by re-using existing circuit building blocks such as differential pairs and OTA's.
   - The layout template is described using the layout language CAIRO [8]. The code is independent of transistor sizes and technology. A parasitics calculation mode allows layout parasitics to be taken into account during sizing.

4. **Physical Design**: The complete layout is generated using the layout templates in a layout generation mode.
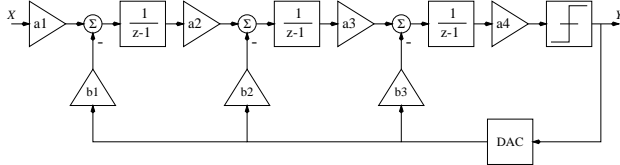
3. High-Level Synthesis

Figure 1. Modulator topology

The goal of this circuit is to achieve very low-voltage operation ($V_{DD} = 1V$) of a high resolution $\Delta\Sigma$ modulator (around 14 bits) for a digital-audio signal.

Fig. 1 shows the block diagram of the modulator. It is based on a one-bit chain of integrators with distributed feedback topology. Modulator coefficients have been determined with the help of the *Delta-Sigma Toolbox* [10] for MATLAB, according to the design procedure given in [11].

4. Performance Parameter Mapping

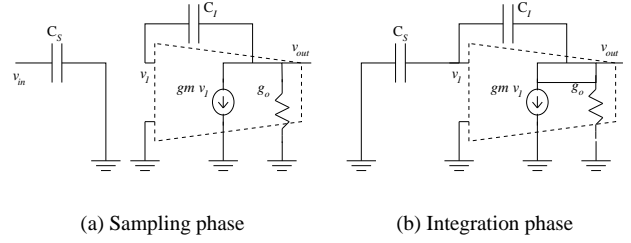Cell non-idealities lead to quantization noise leakage and degrade the overall signal-to-noise ratio (SNR). Study-

(a) Sampling phase   (b) Integration phase

Figure 2. SC integrator

ing their effect also provides mapping of high-level performance specifications to individual block ones.

4.1. Opamp Finite Gain and Frequency

An approach similar to [12] is used. The model is based on the simple one-pole amplifier shown in Fig. 2, whose transfer function is given by :

$$H(z) = \frac{gz^{-1}}{1 - pz^{-1}} \qquad (1)$$

where

$$g = \frac{C_S}{C_I}\rho_i(1-\delta_i), \qquad p = \frac{\rho_i}{\rho_s}\left(1 - \delta_i\left(1 - \frac{\rho_s}{\rho_i}\right)\right) \quad (2)$$

$$\rho_s = \frac{A_{d0}\beta_s}{1 + A_{d0}\beta_s}, \qquad \rho_i = \frac{A_{d0}\beta_i}{1 + A_{d0}\beta_i} \qquad (3)$$

where $A_{d0} = g_m/g_o$, β_s and β_i are the sampling and integration phases feedback factors. The parameter δ_i represents the settling error in the integration phase. It is expressed by

$$\delta_i = exp\left(-\frac{g_m}{C_S}\cdot\frac{T_i}{\rho_i}\right) \qquad (4)$$

where T_i is the time available for integration. The factor g_m/C_S represents the closed loop dominant pole p_{CL} of the amplifier during the integration phase. The above model does not include neither the input parasitic capacitance of the amplifier (C_{ip}) nor the parasitic output capacitance. Furthermore, the used amplifier is actually a two-stage one [7] having its closed-loop pole determined by an internal compensation capacitance. However, if one tries to model these effects, the analysis becomes very complicated. One can preserve the previous simple model and change only the most inaccurately modeled factors [12], such that

$$\beta_s = \frac{C_I}{C_I + C_{ip}}, \qquad \beta_i = \frac{C_I}{C_I + C_{ip} + C_S} \qquad (5)$$

In addition, the exponential factor in equation (4) is strongly affected by the parasitic capacitances. Equation (4) can still be used with $p_{CL} = \beta_i\omega_t$, where ω_t is the GBW of the two
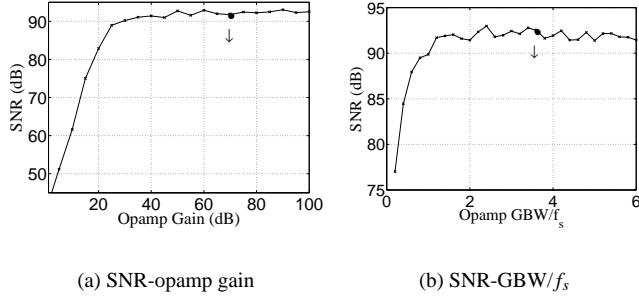
(a) SNR-opamp gain   (b) SNR-GBW/f_s

Figure 3. Simulation results

stage amplifier. Obviously, these approximations neglect the effect of high frequency poles and zeros on the settling performance of the amplifier. This is true for a sufficiently high phase-margin.

The above model is then employed in discrete time simulations. Same non-idealities are considered in all amplifiers. A sinusoidal input of relative amplitude 0.5 and frequency 3.2 kHz is used. First assuming an infinite opamp GBW frequency (f_t), i.e. $\delta_i = 0$, the effect of the amplifier gain on the overall SNR is studied. Fig. 3(a) shows the results of such simulations. A gain of 40dB is then sufficient for preserving the SNR. In our design a gain of 70dB has been chosen for the first opamp and 60dB for the second and third ones. This high gain is chosen to avoid any performance degradation and to reduce the effect of non-linearities. Using the above amplifier gains, Fig. 3(b) shows the variation of the SNR with f_t. Simulations show that an $f_t > 2f_s$ where f_s is the sampling frequency is sufficient. To have some margin, a ratio of 3.5 is chosen.

4.2. Opamp Slew Rate

According to the integrator first-order model presented in the previous section, the time domain response of the integrator output during the integration phase is given by

$$V_{osf}(t) = V_{o1} + V_{step}\left[1 - exp\left(-\frac{1}{\rho_i}\frac{t}{\tau}\right)\right] \qquad (6)$$

where V_{o1} represents the leakage of the integrator stored value due to the amplifier finite gain and GBW and assumed constant for this analysis,

$$V_{step} = V_{in}(0)\frac{C_S}{C_I}\rho_i, \qquad \tau = \frac{1}{p_{CL}} = \frac{1}{\beta_i\omega_t} \qquad (7)$$

From Fig. 4, the slewing output can be described by

$$V_{os}(t) = \begin{cases} SR.t & 0 < t < t_d \\ V1 + V2\left(1 - exp\left(-\frac{1}{\rho_i}\frac{t-t_d}{\tau}\right)\right) & t_d < t < T_i \end{cases}$$
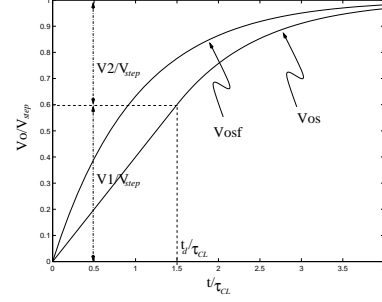$$\qquad (8)$$

Figure 4. Slew-free & and slewing outputs

where $V1$ and $V2$ are defined as shown in Fig. 4. Equating the slope of both sections at $t = t_d$, we have

$$V2 = SR.\tau.\rho_i \qquad (9)$$

and using $V_{step} = V1 + V2 = SR.t_d + V2$, we obtain

$$t_d = \frac{V_{step}}{SR} - \tau.\rho_i \qquad (10)$$

Fig. 5 shows an integrator model based on the above analysis. V_{step} represents the integrator output considering no frequency limitations. The parameters g_{inf} and p_{inf} are given by equation (2) with $\delta_i = 0$. V_{sf} represents the slewing-free integrator output taking into account frequency limitations. The parameters g_{sf} and p_{sf} are given by equation (2). The *SLEW* block models the slewing behavior of the integrator: By calculating t_d from equation (10), the output can be determined according to the slewing state:

- if $t_d < 0$, then the output is slew free,
- if $0 < t_d < T_i$, then slewing occurs but the integrator re-enters eventually in the linear region.
- if $t_d > T_i$, the integrator remains slewing during the entire integration period and the output is given by $SR.T_i$.

A hard limiter is used to model the integrator output saturation levels.

Using the amplifier gain and GBW frequency calculated in the previous section and the above integrator model, Fig. 6 shows the variation of the SNR with the amplifier SR. A SR of $1.3V_{ref}/T_s$ has been chosen, where $T_s = 1/f_s$.
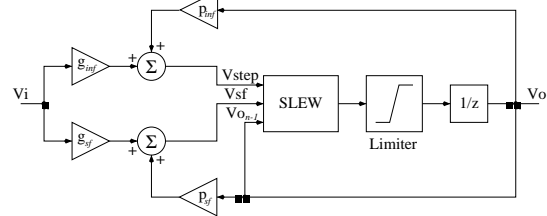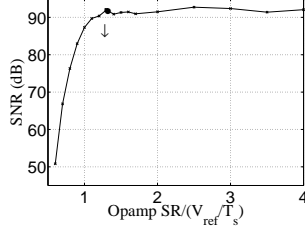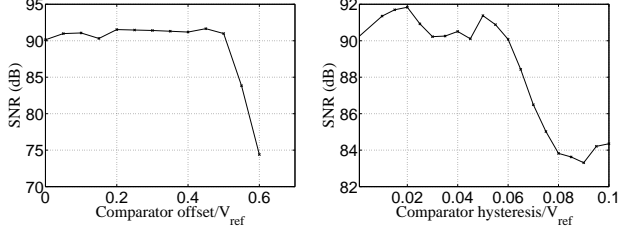

Figure 5. Integrator model

Figure 6. Simulation results, SNR vs. SR

(a) SNR-offset　　　　　(b) SNR-hysteresis

Figure 7. Simulation results

4.3. Comparator Offset and Hysteresis

Fig. 7(a) shows the effect of the comparator offset voltage. The effect of the offset is greatly reduced by the feedback loop of the modulator such that an offset of half of the reference voltage can still be tolerated. However, hysteresis is more critical. Fig. 7(b) shows that the ratio between V_{hys} and the reference voltage must be kept below 0.05.

5. Low-Level Synthesis and Design

In this phase, the analytical equations used to size the building blocks starting from the performance specifications determined in section 4, are derived. In order to be used in COMDIAC, these equations need to be as accurate as possible. All transistor currents, transconductances and capacitances are calculated using the same model equations as that used in the circuit simulator and implemented in COMDIAC.

Fig. 8 shows the modulator design flow with emphasis on the low-level synthesis step. Starting from the required SNR performance, both the quantization noise and circuit noise are determined. The in-band noise power must be dominated by the circuit noise rather than the quantization noise in order to minimize the total power consumption. Quantization noise is determined during high-level synthesis by the chosen architecture and OSR (section 3). The circuit noise is further decomposed to KT/C noise and amplifier noise. Due to the very low coefficient of the first integrator (a_1) the amplifier noise becomes dominant. The amplifier
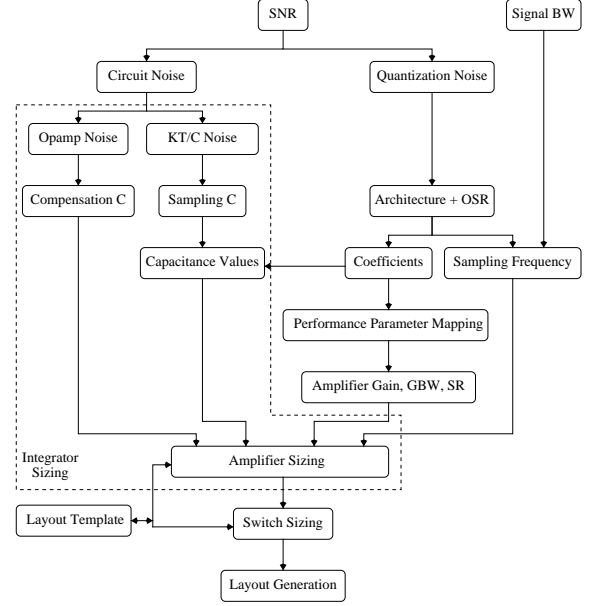

Figure 8. Modulator design flow

thermal noise power depends directly on the compensation capacitor C_C, but since it also depends on the amplifier noise excess factor γ_{th}, which is not known before the complete amplifier design, fine tuning of the compensation capacitor value is thus needed during the amplifier sizing process. In fact, the calculated C_C sets the minimal value for the compensation capacitor which also controls the opamp phase margin. On the other hand, the switch thermal noise power is mainly determined by the value of the input sampling capacitor. Starting from the modulator coefficients and taking into account integrator scaling, all capacitor values are then determined.

Performance parameter mapping is then performed as described in section 4 leading to values for the opamp DC gain, GBW and SR, as well as the comparator offset and hysteresis that avoid noise leakage. Integrator sizing then follows as described in the following section.

5.1. Integrator Sizing in COMDIAC

Fig. 9 shows the integrator sizing plan. In our design procedure, there are two sets of input parameters; those determined directly by the previous high-level analysis and those used for design optimization. The first set, shown horizontally in Fig. 9, includes:

- The maximum input signal amplitude (U_{max}).
- The sampling frequency (f_s) and the integration phase duty cycle.
- The opamp gain, GBW, and SR.
- Minimum opamp compensation capacitance (C_C).
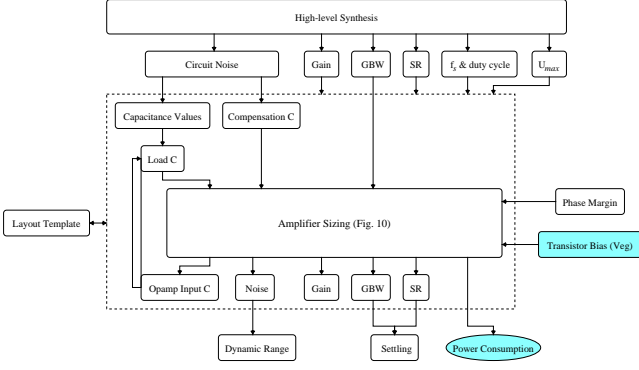- The integration and sampling capacitances (C_I and C_S).

Figure 9. Integrator sizing

While the second set, shown vertically on the right of Fig. 9, includes:

- The phase margin (PM).
- Transistor bias voltages V_{EG} and V_{DS}.

The integrator sizing module uses the opamp module as a building block. The opamp load C_L is calculated taken into account the loading of the integrator feedback network as given by

$$C_L = \frac{(C_S + C_{ip})C_I}{C_S + C_{ip} + C_I} + C_{Ibp} \qquad (11)$$

where C_{Ibp} is the integration capacitor bottom-plate capacitance. Since C_L depends on C_{ip} which is only calculated after sizing, two or more iterations are needed to find C_L. The opamp calculated performance parameters are then used to calculate those of the integrator namely the settling performance, the dynamic range and the total power consumption. Shaded input parameters on the right of the figure, namely transistor bias voltages, are used for performance optimization as explained in the next section. The optimization goal was to minimize the power consumption under a given settling and dynamic range performance.

A layout template is used to calculate the associated layout parasitics. During sizing, layout parasitics are also taken into account. This includes exact transistor diffusion after the calculation of parallel elements (M), routing and capacitor bottom-plate capacitances.

5.2. Opamp Sizing in COMDIAC

The complexity of the sizing problem resides in its multi-dimensional design specification and variable spaces. Four types of independent variables can be defined for a given opamp:

1. the bias current I,
2. transistor biasing voltages $V_{EG} = V_{GS} - V_{TH}$ and V_{DS},
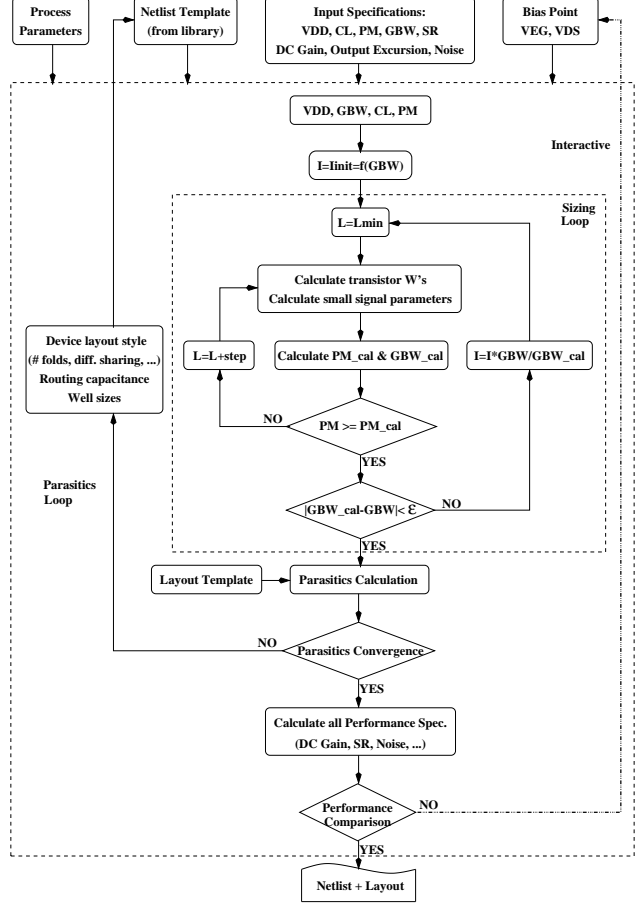3. technology parameters, and

Figure 10. Opamp sizing

4. transistor lengths L.

By fixing the current and biasing voltages, only transistor lengths should be varied in order to satisfy a given performance specifications. The phase-margin (PM) and the gain-bandwidth product (GBW) have been chosen as the main characteristics to be satisfied. Other specifications can be realized interactively by modifying transistor biasing points. Fig. 10 describes the sizing procedure. A minimal set of specifications are defined, this includes:

- the supply voltage V_{DD},
- the gain-bandwidth product,
- the phase margin,
- the load and compensation capacitances,

in addition to the biasing voltage V_{DS} and V_{EG} of each independent transistor which are also held constant during the sizing loop (since V_{TH} changes with transistor lengths during sizing, the effective gate-source voltage $V_{EG} = V_{GS} - V_{TH}$ is held constant rather than V_{GS}). First, an initial bias current is *estimated* from the given GBW. All transistor lengths are set to their corresponding minimal value

as a starting point. The sizing loop starts by incrementing transistor lengths, calculating the corresponding widths and small signal parameters using the chosen transistor model equations, and finally calculating the PM. The GBW is then calculated and compared with the required one. A new value for the bias current is calculated by linear interpolation and the whole process is repeated till the required GBW is satisfied. A call to the layout tool allows to calculate the corresponding layout parasitics. If parasitics convergence is achieved, i.e. the layout parasitics do not change any more, the procedure calculates the rest of the obtained performance characteristics. These characteristics can be controlled by choosing appropriate transistor biasing voltages. Fixing the operating point of each transistor taking into account considerations like matching and temperature dependence increases the reliability of the produced circuits. The fact that the sizing process is very fast and highly accurate allows interactive exploration of wide variety of design space points.

5.3. Switch Sizing in COMDIAC

In this section, we discuss the method used for switch sizing implemented in COMDIAC. Due to the low supply voltage, switch slewing [13] must be taken into account. Switch sizing is performed given:

- Transistor length.
- The load capacitance C_S.
- V_{GS}, V_{BS} and initial V_{DSinit}.
- Available time for charging the load capacitance t_{av}.
- Settling error ε.

Worst-case settling is assumed by considering that the given t_{av} will be divided into a slewing time t_{slew} during which the switch slews throughout the whole given $V_{DS} = V_{DSinit}$ down to $V_{DS} = 0$ in addition to a linear time t_{lin} during which slewing is neglected and a linear settling to the required settling error is assumed. The sizing procedure is summarized in Fig. 11. It starts from the minimum transistor width W_{min}. If the transistor starts in the saturation region, it calculates the switch $SR_{switch} = I_{Dsat}/C_S$. The slewing time is then calculated by:

$$t_{slew} = \frac{V_{DSinit}}{SR_{switch}} \tag{12}$$

and the linear time is calculated using:

$$t_{lin} = \tau_{switch} ln\left(\frac{1}{\varepsilon}\right) = \frac{C_S}{g_{ds}} ln\left(\frac{1}{\varepsilon}\right) \tag{13}$$

Then if the total time $t_{slew} + t_{lin}$ is less then the given available time t_{av}, then sizing is accomplished, if not the process is repeated by incrementing the transistor width which in
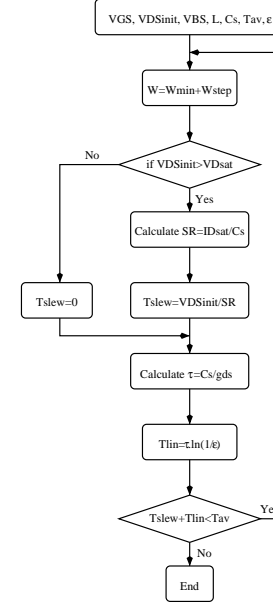
Figure 11 flowchart:
VGS, VDSinit, VBS, L, Cs, Tav, ε → W=Wmin+Wstep → if VDSinit>VDsat (No → Tslew=0; Yes → Calculate SR=IDsat/Cs → Tslew=VDSinit/SR) → Calculate τ=Cs/gds → Tlin=τln(1/ε) → Tslew+Tlin<Tav (Yes → back to W=Wmin+Wstep; No → End)

Figure 11. Switch sizing

turn increases the saturation current (and consequently the switch SR) and the drain-source conductance g_{ds} both leading to decrease t_{slew} and t_{lin} respectively.

The same procedure has been used to size the switch bootstrapping circuit. Switch sizing procedures allow to size *separately* each switch in the modulator circuit based on its charge and the required settling error. This optimizes switch sizes for low-voltage operation which happens to be large compared to normal SC circuits due to the small switch overdrive, this allows to minimize as much as possible clock feedthrough effects due to large switch gate capacitances. In order to avoid performance degradation due to switch settling, all switches are required to settle to the modulator accuracy.

6. Implementation and Design Reuse

The quality of the previous design flow has been verified through circuit fabrication and measurements. The layout language CAIRO [8] has been used to construct layout templates. Based on these templates, CAIRO can both estimate layout parasitics used during the design phase and eventually generates hierarchically the final layout. The tool internal complex device generators (transistors, differential pairs, capacitor arrays, ...) integrate analog-specific and reliability layout constraints. For example, by controlling the number of folds of a given transistor, one can minimize diffusion parasitic capacitance on the source/drain terminals [8]. A parasitics model that is used during the parasitics estimation mode accompanies each device. In addition, routing capacitance is easily determined based on the
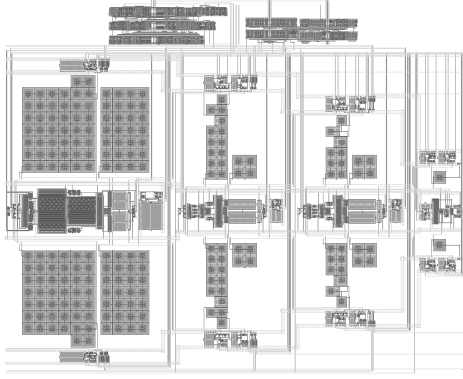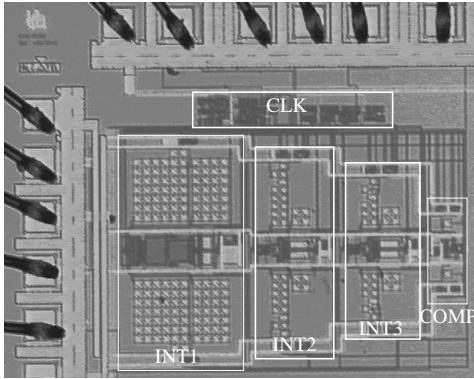
Figure 12. Modulator in technology 1

Figure 13. Chip die photo in technology 1

Figure 14. Modulator in technology 2

	Technology 1	Technology 2
Technology	twin-tub 2P5M	p-sub 2P3M
Min. gate length	0.35μ	0.3μ
n/p threshold	580/600mV	500/650mV
Poly capacitor	1.1 ± 0.15fF/μm^2	0.86 ± 0.1fF/μm^2
1st integ. P_c	570μW	610μW
Total P_c	950μW	820μW
Modulator Area	0.9×0.7mm^2	1.0×0.9mm^2

Table 2. Modulator in two technologies

rameter mapping (section 4).

The *same* input specifications has been resynthesized in another technology from a different foundry, as follows:

1. The same high-level synthesis (section 3) and performance parameter mapping (section 4) results are directly applied.

2. The same integrator sizing procedure is used to size the integrators. Since this sizing is done interactively as shown in sections 5.1 and 5.2, this is the most time-consuming step. However, COMDIAC allows rapid design-space exploration in the presence of parasitics.

3. The same switch sizing procedure (section 5.3) is used to size separately all switches in the circuit.

4. The same layout templates have been reused both for parasitics estimation and layout generation.

Since the modulator was targeted for reliable operation of future very low-voltage technologies [6], real low-voltage technologies, available at the time of implementation, have been chosen. Table 2 shows a comparison of the two implementations. While for the first design the same opamp has been used for the second and third integrators, in the second design two different amplifiers, optimized for each stage, have been used which enabled a further reduction of the total power consumption. However, lower specific capacitance of the second technology has resulted in a larger area. Figures 12 and 14 show the resulting layouts in both

corresponding layout template which also includes information on relative routing, such that the exact position of each routing wire is easily found after the area optimization step. The code corresponding to each block has been developed separately and then instantiated in higher blocks. The code corresponding to repeatedly used blocks is thus reused several times each with a different set of transistor sizes.

The modulator has been designed for the following input specifications: An OSR of 100, a signal BW of 16kHz, a DR of 85dB under a supply voltage of 1V. Fig. 13 shows the chip photograph [6]. Measured performance is summarized in table 1. Obtained results are better than simulated ones due to extra design margins chosen during performance pa-

Supply Voltage	1V
Reference Voltage	1V
Dynamic Range	88dB
Peak SNR / SNDR	87dB / 85dB
Oversampling Ratio	100
Sampling Rate	5MHz
Signal Bandwidth	25kHz
Power Consumption	950μW

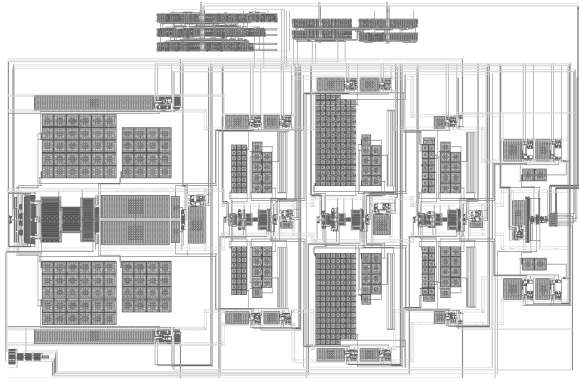**Table 1. Measured performance summary**

Figure 15. 4th-order modulator

cases. It should be noted that after the complete design of the first modulator, the second design has taken only one week from specifications down to layout.

In order to further investigate another dimension of design reuse, a completely different modulator topology has been used to design another modulator using the same low-voltage building blocks as the previous ones thus the same *design knowledge*. A single-loop fourth-order modulator employing a mixed loop topology with both feedforward and feedback paths [14] has been chosen. The same design flow, described above, has been employed during the design. Technology 2 has been chosen for the implementation. Simulations show that for a supply voltage of 1V, an OSR of only 70 and a signal BW of 20kHz, the modulator achieves a DR of 90dB with a power consumption of 1.15mW. Fig. 15 shows the complete layout of the modulator. The overall area is 1.3×0.85mm^2. Due to the reuse of the same layout templates, the modulator floorplan is very close to the previous ones except for the additional integrator stage. The complete design and layout generation was completed in two weeks.

7. Conclusions

The complete design methodology of a very low-voltage $\Delta\Sigma$ modulator has been presented. It is based on a hierarchical top-down approach with performance parameter mapping from high-level to lower level blocks. A layout-oriented sizing approach has been employed to accurately account for layout parasitics during the design. This avoids laborious sizing-layout iterations and facilitates design reuse. Two modulator designs have been resynthesized using the knowledge stored in the sizing and layout plans. Besides being fast, this method also allows first-pass silicon of future circuits with guaranteed performance.

This work shows that design experience acquired during analog design can be efficiently stored for eventual similar designs. This allows rapid IP design reuse.

References

[1] R. R. Neff, P. R. Gray, and A. Sangiovanni-Vincentelli. A Module Generator for High-Speed CMOS Current Output Digital/Analog Converters. *IEEE J. of Solid-State Circuits*, 31(3):448–451, Mar. 1996.

[2] F. Medeiro, B. Pérez-Verdú, A. Rodríguez-Vázquez, and J. L. Huertas. A Vertically Integrated Tool for Automated Design of $\Sigma\Delta$ Modulators. *IEEE J. of Solid-State Circuits*, 30(7):762–772, July 1995.

[3] K. Francken and G. Gielen. Methodology for Analog Technology Porting Including Performance Tuning. In *Proc. IEEE Int. Symposium on Circuits and Systems*, volume 1, pages 415–418, May 1999.

[4] R. Phelps, M. J. Krasnicki, R. A. Rutenbar, L. R. Carley, and J. R. Hellums. A Case Study of Synthesis for Industrial-Scale Analog IP: Redesign of the Equalizer/Filter Frontend for an ADSL CODEC. In *Proc. Design Automation Conf.*, http://www.dac.com/profrTOC.html, June 2000.

[5] M. Dessouky, M.-M. Louërat, and J. Porte. Layout-Oriented Synthesis of High Performance Analog Circuits. In *Proc. Design Automation and Test in Europe Conf.*, pages 53–57, Mar. 2000.

[6] M. Dessouky and A. Kaiser. Very Low-voltage $\Delta\Sigma$ Modulator with 88dB Dynamic Range using Local Switch Bootstrapping. *IEEE J. of Solid-State Circuits*, 36, Mar. 2001.

[7] M. Dessouky and A. Kaiser. Very Low-Voltage Fully Differential Amplifier for Switched-Capacitor Applications. In *Proc. IEEE Int. Symposium on Circuits and Systems*, volume 5, pages 441–444, May 2000.

[8] M. Dessouky and M.-M. Louërat. A Layout Approach for Electrical and Physical Design Integration of High-Performance Analog Circuits. In *International Symposium on Quality Electronic Design*, Mar. 2000.

[9] J. Porte. *COMDIAC: Compilateur de Dispositifs Actifs, reference manual*. Ecole Nationale Supérieure des Télécommunications, Paris, Sept. 1997.

[10] R. Schreier. *The Delta-Sigma toolbox for MATLAB*. Oregon State University, ftp://next242.ece.orst.edu/pub/delsig.tar.Z.

[11] R. W. Adams and R. Schreier. Stability theory for $\Delta\Sigma$ modulators. In S. R. Norsworthy, R. Schreier, and G. C. Temes, editors, *Delta-Sigma Data Converters. Theory, Design, and Simulation*, chapter 4. IEEE Press, 1996.

[12] Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen. A 3.3-V, 15-bit, Delta-Sigma ADC with a Signal Bandwidth of 1.1 MHz for ADSL Applications. *IEEE J. of Solid-State Circuits*, 34(7):927–936, July 1999.

[13] V. Peluso, M. S. J. Steyaert, and W. Sansen. A 1.5V-100μW $\Sigma\Delta$ Modulator with 12-b Dynamic Range Using the Switched-Opamp Technique. *IEEE J. of Solid-State Circuits*, 32(7):943–952, July 1997.

[14] A. L. Coban and P. E. Allen. A 1.5V 1.0mW Audio $\Delta\Sigma$ Modulator with 98dB Dynamic Range. In *Proc. IEEE Int. Solid State Circuit Conf.*, pages 50–51, 1999.