Exploring SOI Device Structures and Interconnect Architectures for 3-Dimensional Integration *

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ABSTRACT

3-Dimensional (3-D) integration offers numerous advantages over conventional structures. Double-gate (DG) transistors can be fabricated for better device characteristics, and multiple device layers can be vertically stacked for better interconnect performance. In this paper, we explore the suitable device structures and interconnect architectures for multi-device-layer integrated circuits and study how 3-D SOI circuits can better meet the performance and power dissipation requirements projected by ITRS for future technology generations. Results demonstrate that DGSOI circuits can achieve as much as 20% performance gain and 8% power delay product reduction than SGSOI (single-gate SOI). More important, for an interconnect-dominated circuits, multi-device-layer integration offers significant performance improvement. Compared to 2-D integration, most 3-D circuits can be clocked at much higher frequencies (double or even triple). Multi-device-layer circuits, with suitable SOI device structures, can be a viable solution for future low power high performance applications.

1. INTRODUCTION

Scaling has been the primary approach employed in the past few decades in meeting circuit performance and power consumption requirements in VLSI circuits. However, as device dimensions shrink to submicron and below, short channel effects and quantum effects become prominent. Simply scaling down device dimensions without altering device structures is no longer sufficient to maintain good device characteristics, circuit performance, or power consumption [1]. Moreover, transistor count and chip size continually increase; more and more transistors are closely packed and connected [2]. To deal with such a challenge, state-of-the-art process technologies heavily rely on adding more metal layers. It is believed that up to ten metal layers are needed in the next decade when the circuit speed reaches several gigahertz [3]. Adding more metal layers increases the complexity and cost of the process technology and degrades the circuit reliability. More seriously, interconnect delay increases significantly due to the reduced wire width and increased interconnect length. In fact, interconnect delay has become a dominant factor in determining circuit performance [4]. It is, therefore, necessary to look for new device structures and circuit integration concepts to continually fuel the growth of the VLSI industry in the nanometer generations when conventional device structures are likely to reach the projected physical limits, and when the interconnect becomes the limiting factor to the integration capacity as well as circuit speed.

Silicon-on-Insulator (SOI) technology has demonstrated many advantages over bulk silicon technology [5]. Moreover, the unique features of SOI technology make it easy to realize vertical structures for fully or partially depleted transistors with single or double gates. Double gate SOI (DGSOI) transistors have better on/off current ratio and may result in better circuits [6, 7]. In addition, vertical integration enables a process technology to stack the device layers [8]. Stacking device layers significantly reduces the interconnect complexity and delay [9, 10]. Hence, 3-D integration is able to simultaneously meet the device, circuit, and interconnect requirements, which makes it a serious contender for future low power and high performance applications.

In this paper, we present the first study (to the best of our knowledge) of the applications that combine two highly promising technologies – DGSOI transistors for superior device characteristics, and multi-device-layer integration for enhancing interconnect performance. Different 3-D SOI device structures and interconnect architectures for low power and high performance applications are explored. We present a system-level performance and power dissipation evaluation for multi-device-layer integration with double-gate or single-gate transistors. By comparing the clock speed, power dissipation, and power-delay product of SGSOI and DGSOI circuits with various number of device layers, we provide a vision on how 3-D SOI circuits can better meet the requirements of future technology generations.

2. 3-D SOI DEVICE AND CIRCUIT STRUCTURES

Fig. 1 (a) shows the cross section of a single-gate SOI (SGSOI) structure. When the silicon film is thicker than the maximum gate depletion width, SOI transistors exhibit floating body effects and are regarded as partially-depleted (PD) SOI MOSFETs. If the silicon film is thin enough that the entire film is depleted, the SOI devices are considered as fully-depleted (FD) SOI MOSFETs. Another structure is double gate SOI (DGSOI) (see Fig. 1 (b)), where t_{of}, t_{si}, and t_{ob} represent front gate oxide thickness, silicon film thickness, and back gate oxide thickness, respectively. Double gate fully depleted SOI MOSFETs have ideal subthreshold slope, high drive current and superb short channel effect immunity. This

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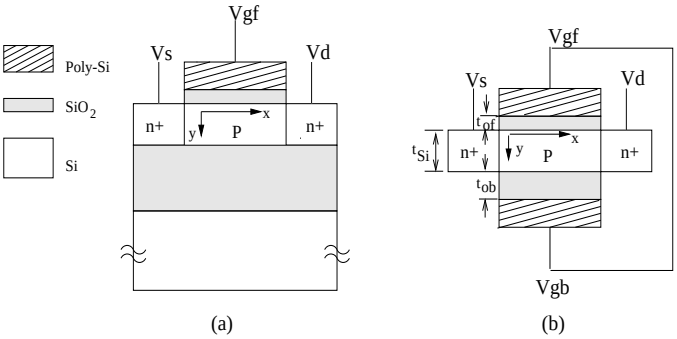

Figure 1: SOI MOSFETs (a) SGSOI (b) DGSOI.

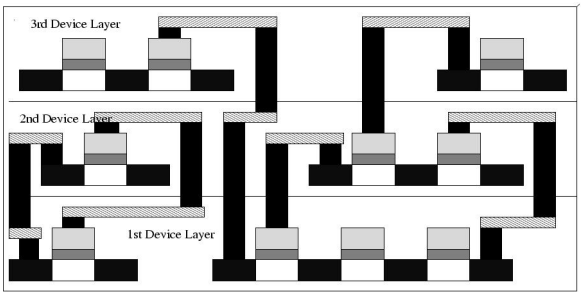

Figure 2: Cross-section of a multi-device-layer integrated circuit.

makes them very attractive in low-voltage low-power and high performance CMOS circuit designs [5].

The vertically integrated process technology provides possibilities for double gated fully depleted devices and eliminates the concerns in making a small, well-aligned back gate. Moreover, instead of simply spanning devices in a single 2-D layer, vertically integrated technology (3-D technology) enables us to have multiple device layers stacked over each other. Stacked structures achieve an increase of packing density and a decrease of interconnection length, saving chip area and improving circuit performance. A 3-device-layer SOI structure is illustrated in Fig. 2.

Recent published work suggests that performance improvement can be achieved by reduced wire length with 3-D integration [9, 10]. Fig. 3 illustrates how the wire-length can be reduced in a 4-device-layer integration. Original wire AB is replaced by $A'B'$ and length is reduced by half.

3. 3-D DELAY DISTRIBUTION

An accurate model is needed for system-level performance and power dissipation evaluation for 3-D circuits. This model should encompass device, interconnect, as well as circuit and logic. 3-D SOI circuit delay distribution provides the information necessary to understand the overall system performance.

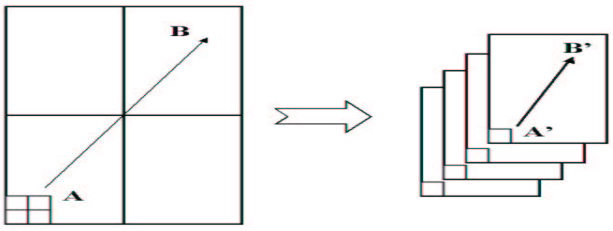

Figure 3: Reduction of wire-length with 3-D integration.

3.1 Modeling of Fully Depleted SOI MOSFETs

A well established, general analytical model, which can be applied to both symmetric and asymmetric DGSOI transistors, is derived in [6].

Consider the DGSOI NMOSFET shown in Fig. 1(b). V_{gf} and V_{gb} denote the front gate and back gate voltages while t_{si}, t_{of}, and t_{ob} represent the silicon film thickness, front gate oxide thickness, and back gate oxide thickness, respectively (Usually, $t_{of} \leq t_{ob}$. If $t_{of} = t_{ob}$, the transistor is regarded as a symmetric DGSOI MOSFET). Thus, the front gate threshold voltage with depleted back surface ($V_{tf,depb}$) and the front gate threshold voltage with inverted back surface ($V_{tf,invb}$) can be expressed by the following equations,

$$V_{tf,depb}(V_{gb}) = V_{fbf} + \frac{(1+\alpha)(2\Phi_F) - (V_{gb} - V_{fbb}) + \frac{\beta}{2}\frac{qN_A}{\epsilon_{si}}}{\alpha}; \quad (1)$$

$$V_{tf,invb} = V_{fbf} + 2\Phi_F + \frac{q N_A t_{si}}{2C_{of}}; \quad (2)$$

where $\alpha = \frac{\epsilon_{ox}}{\epsilon_{si}}\frac{t_{si}}{t_{of}} + \frac{t_{ob}}{t_{of}}$ and $\beta = 2\frac{\epsilon_{si}}{\epsilon_{ox}}t_{ob}t_{si} + t_{si}^2$. V_{fbf} and V_{fbb} represent the front channel and back channel flat band voltages, respectively. Φ_F denotes Fermi Potential. N_A is channel doping and C_{of} and C_{ob} are the front gate and back gate capacitance per unit area, respectively.

Back gate threshold voltage with front surface depleted ($V_{tb,depf}(V_{gf})$) and back gate threshold voltage with front surface inverted ($V_{tb,invf}$) can be obtained with similar equations.

For a DGSOI MOSFET, the saturation current I_{on} can be expressed as

$$I_{on} = \begin{cases} \frac{W\mu_{eff}C_{of}}{2L}\frac{(V_{dd}-V_{tf,vdd})^2}{1+(V_{dd}-V_{tf,vdd})/\frac{2v_{sat}}{\mu_{eff}}L} & (V_{dd} < V_{tb,invf}); \\ \frac{W\mu_{eff}C_{of}}{2L}\frac{(V_{dd}-V_{tf,invb})^2}{1+(V_{dd}-V_{tf,invb})/\frac{2v_{sat}}{\mu_{eff}}L} + & \\ \frac{W\mu_{eff}C_{ob}}{2L}\frac{(V_{dd}-V_{tb,invf})^2}{1+(V_{dd}-V_{tb,invf})/\frac{2v_{sat}}{\mu_{eff}}L} & (V_{dd} \geq V_{tb,invf}); \end{cases} \quad (3)$$

where μ_{eff} is the effective mobility and v_{sat} is carrier saturated drift velocity. $V_{tf,vdd} = V_{tf,depd}(V_{dd})$.

I_{off} can be expressed by the following equations,

$$I_{off} = I_{f0}\, e^{-\frac{V_{tf,0}}{V_T}}(1 - e^{-\frac{V_{dd}}{V_T}}) + I_{b0}\, e^{-\frac{V_{tb,0}}{V_T}}(1 - e^{-\frac{V_{dd}}{V_T}}); \quad (4)$$

$$I_{f0} = \mu_0 C_{of}\frac{W}{L}\, {V_T}^2 e^{1.8}; \quad (5)$$

$$I_{b0} = \mu_0 C_{ob}\frac{W}{L}\, {V_T}^2 e^{1.8}; \quad (6)$$

where $V_{tf,0} = V_{tf,depb}(0)$ and $V_{tb,0} = V_{tb,depb}(0)$ represent the front gate threshold voltage at zero bias V_{gb} and the back gate threshold voltage at zero bias V_{gf}, respectively. V_T is the thermal voltage $\frac{KT}{q}$, and μ_0 is zero bias mobility.

For SGSOI transistor, $t_{ob} \approx \infty$. Thus I_{on} and I_{off} can be expressed as

$$I_{on} = \frac{W\mu_{eff}C_{of}}{2L}\frac{(V_{dd} - V_{tf,vdd})^2}{1 + (V_{dd} - V_{tf,vdd})/\frac{2v_{sat}}{\mu_{eff}}L}; \quad (7)$$

$$I_{off} = I_{f0}\, e^{-\frac{V_{tf,0}}{V_T}}(1 - e^{-\frac{V_{dd}}{V_T}}). \quad (8)$$

3.2 3-D Interconnect Modeling

A 3-D interconnect model was developed for investigating the impact of multi-device-layer structures on circuit performance and

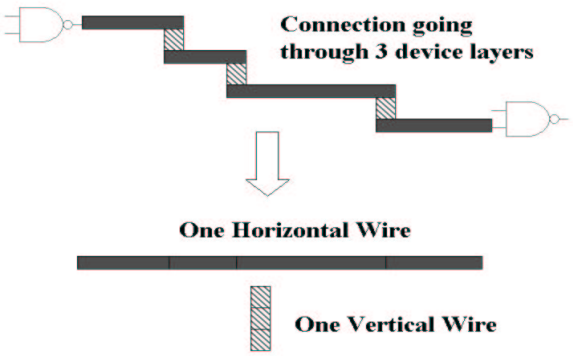

Figure 4: Definition of horizontal and vertical wire.

power consumption [10]. In order to best understand the wiring requirements, the overall wires are divided into two parts: horizontal wires and vertical wires. For a wire connecting one gate to another, the portions that are parallel to the device layers are defined as a *horizontal wire* and the portions that are perpendicular to the device layers are defined as a *vertical wire* (Fig. 4). Horizontal wires determine the overall routing resources on top of each device layer, and are generally realized by metal layers. Vertical wires are realized by vertical channels and have impact on the area of device layer. Both horizontal and vertical wires contribute to the overall interconnection delay.

For a system with N gates distributed in m device layers, The closed form expressions of the horizontal and vertical wire-length distributions are obtained by extending Rent's Rule [4] and are listed as follows:

Horizontal Wire-Length Distribution:

$$h(\ell) = \begin{cases} \Theta(\frac{\ell^3}{3} - 2\ell^2\sqrt{\frac{N}{m}} + 2\ell\frac{N}{m})l^{2p-4}, & 1 \le \ell < \sqrt{\frac{N}{m}}; \\ \frac{\Theta}{3}(2\sqrt{\frac{N}{m}} - \ell)^3\ell^{2p-4}, & \sqrt{\frac{N}{m}} \le \ell \le 2\sqrt{\frac{N}{m}}; \end{cases} \quad (9)$$

where $h(\ell)$ is the number of connections with horizontal distance of ℓ gate pitches; and

$$\Theta = \frac{\alpha A m^p \frac{N}{m}(1-(\frac{N}{m})^{p-1})}{-(\frac{N}{m})^p \frac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{\frac{N}{m}}}{2p-1} - \frac{\frac{N}{m}}{p-1}}.$$

Vertical Wire-Length Distribution:

$$V(k) = \frac{\alpha AN(1 - N^{p-1} - m^{p-2} + m^{-1}N^{p-1})}{m(m-1)}(2m - 2k); \quad (10)$$

where $V(k)$ is the number of connections with vertical distance of k device layers. $k = 1, 2, ..., m-1$. A, α, p are Rent's parameters for interconnect complexity [4].

When $m = 1$, the expressions give the wire-length distributions of 2-D circuits (no vertical wires).

3.3 3-D Delay Distribution

With the device and interconnect models presented in the previous subsection, delay distribution can be readily obtained for 3-D integrated SOI circuits. This subsection studies the delay distribution of single-gate and double-gate circuits with multi-device-layer integrations. The delay distribution is calculated for $180nm$ technology generation as projected by ITRS [3]. To simplify the calculation, we assume that each gate is a two-input NAND gate. Based on transistor density predicted by ITRS, the sizes of the transistors are estimated to be $W_n/L_n = 10$ and $W_p/L_p = 10$. Also, for a net with both horizontal wire and vertical wire, we assume that the vertical wire is in the middle of the net regardless of the length of the net (Fig. 5). We denote the resistance and capacitance of a horizontal wire with one gate pitch as R and C, respectively; and denote the resistance and capacitance as $Rv * R$ and $Cv * C$ respectively for a vertical wire with one device layer depth (distance between the neighboring device layers). The coefficients R_v and C_v equalize the vertical wire-length to horizontal wire-length for resistance and capacitance calculation. Under the assumption that tungsten plugs are used as vertical channels, Rv and Cv are estimated to be 10 and 0.85, respectively. Fan-out of a gate is assumed to be 3, which gives us $A = 3.8$ and $\alpha = 0.74$ [11]. For discussion purpose, Rent's constant p is arbitrarily set to 0.45 based on the facts that $p = 0.45$ roughly reflects the interconnect complexity of high performance MPUs.Our conclusions, however, are independent of the value of p.

Table 1: Device and Interconnect Parameters at 180nm Technology Node.

Parameter	Value
Assumed	
Transistor count	22M
Average gate fanout	3
Minimum gate length, L_n , $L_p(nm)$	140
Front gate oxide thickness, t_{of}, (nm)	2.5
DGSOI Back gate oxide thickness, t_{ob}, (nm)	25
Body film thickness, t_b, (nm)	12.5
Supply voltage, $Vdd(V)$	1.8
Channel doping, $N_a(cm^{-3})$	1.5E18
Horizontal interconnect resistance, $\rho(\Omega - cm)$	3.3
Horizontal interconnect capacitance, $C_w^h(fF/\mu m)$	0.2
Length of one gate pitch, (μm)	9
Width of the wires, $2L_n(nm)$	280
Wire aspect ratio	2.2
Derived	
DGSOI Gate switching resistance, $R_{sw}(\Omega)$	2154.5
DGSOI Gate capacitance, $C_g(fF)$	4.763
SGSOI Gate switching resistance, $R_{sw}(\Omega)$	2489
SGSOI Gate capacitance, $C_g(fF)$	4.33
Horizontal wire resistance per gate pitch, $R(\Omega)$	1.719
Horizontal wire capacitance per gate pitch, $C(fF)$	1.8
Vertical wire resistance per device layer depth Ω	17.19
Vertical wire capacitance per device layer depth fF	1.53

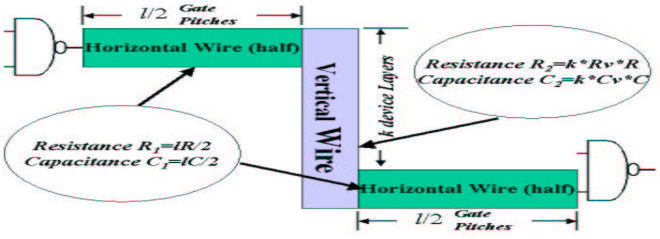

Figure 5: 3-D wire and its parasitic resistance and capacitance.

Table 1 lists the device and interconnect parameters for $180nm$ technology node identified by ITRS [3]. The delay of each net is calculated using Elmore delay model [12].

Figs. 6 illustrate the delay distributions of single-gate SOI circuits with respect to the number of device layers $m = 1,\ 4,\ 8,\ 16$

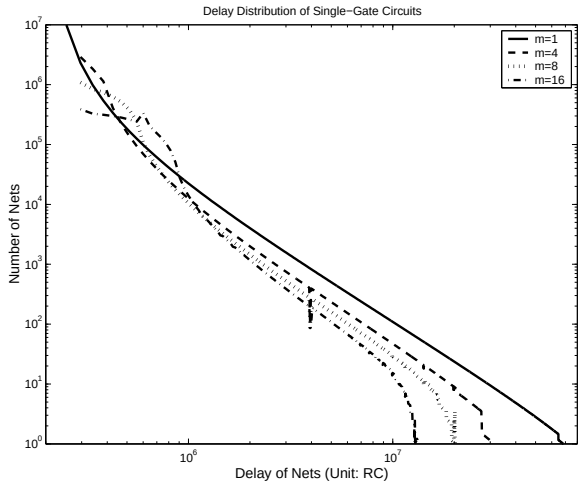

Figure 6: Delay distribution of SGSOI circuits with multi-device-layer integration.

(Double-gate SOI circuits have similar plot). Clearly we see that every 3-D delay distribution shows two distinct regions compared to 2-D distribution (solid line). We refer to the region that contains the short-delay nets as local region; and refer the region that contains the long-delay nets as the global region.

We observe that as the number of device layers increases, the range of the local region increases and the range of the global region decreases. Two factors contribute to this scenario. First, with more device layers, more long-delay nets in 2-D are reduced and converted into short-delay nets in 3-D. Thus, the local region is enlarged. The increase of nets in the local region compensates for the decrease of nets in the global region so that the conservation of total nets is maintained. We can therefore conclude that 3-D structures effectively reduce the long-delay nets to achieve high performance. Second, the influence of vertical wires is more pronounced with the increasing number of device layers and may even turn the short delay nets in 2-D to moderate delay nets in 3-D. When the contribution of vertical wires is significant enough, the local region may even be further extended and may completely cancel the benefit brought by 3-D structures. This implies that vertical wires may limit the number of the device layers that can be integrated.

To compare the SGSOI and DGSOI circuits, we combine their delay distribution plots into Fig. 7. We observe that DGSOI distribution looks like a left-shift of SGSOI's. This implies that the delay for all nets is consistently reduced by DGSOI circuits. Therefore, performance improvement can be expected for DGSOI circuits.

4. PERFORMANCE AND POWER DISSIPATION EVALUATION

The evaluation is based on 1999 *International Technology Roadmap for Semiconductors* [3]. ITRS identifies the trends and challenges of the VLSI technology from 1999 up to 2014. The period is divided into 6 technology generations. Clear targets and technology requirements for each generation are projected.

Table 2 lists the parameters of high performance MPUs for the six technology generations. We again assume that the gates are 2-input NAND gates. The wire width are two times the minimum gate length. The normalization coefficient Rv and Cv remain the same across the six technology generations ($Rv = 10.0$ and $Cv = 0.85$). Rent's constant p is taken as 0.45. The back gate

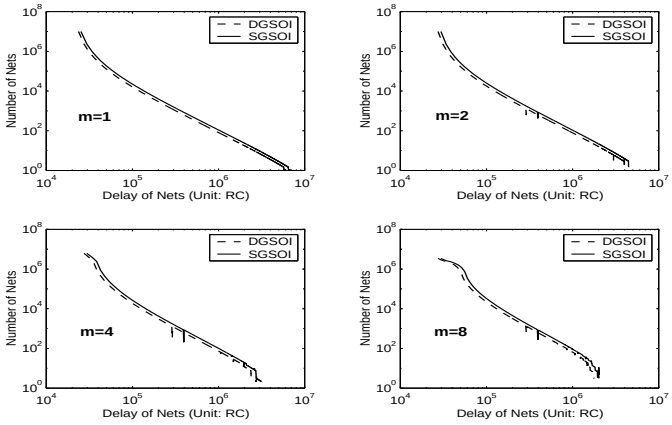

Figure 7: Comparison of Delay distribution of DGSOI and SGSOI circuits with multi-device-layer integration.

oxide thickness and body film thickness are set as $5t_{of}$ and $10t_{of}$, respectively, where t_{of} represents the front gate oxide thickness.

4.1 Performance Evaluation

The widely accepted critical path delay model with f_d stages [4] assumes that delay of $f_d - 1$ stages to be average net delay and the remain one to be determined by the longest global interconnect. Therefore, the minimum clock period T_c is given by

$$T_c = (f_d - 1)\tau_{avg} + T_{LD}, \tag{11}$$

where f_d is the logic depth and is estimated around 20 [4], τ_{avg} is the average gate delay, and T_{LD} is the delay of the longest global interconnect in the system. For giga-scale integration, the performance is dominated by the interconnect. T_c is mostly determined by the longest global interconnect delay.

In most of the critical path models, the average gate delay is calculated by taking average interconnection length as the wire load [4]. Such an approach does not capture the fact that the relation of delay and wire-length is not linear, hence can not be linearly superimposed. A more accurate approach is to calculate the average delay directly. With delay distribution calculated in Section 3, The average net delay τ_{avg} can be easily obtained by

$$\tau_{avg} = \frac{\sum_{all\ t} N(t)t}{\sum_{all\ t} N(t)}; \tag{12}$$

where function $N(t)$ gives the number of nets N with delay t.

Fig. 8 plots the clock speed with respect to various numbers of device layers for SGSOI and DGSOI circuits, respectively. For comparison, we assume that 2-D SGSOI circuit at each technology generation meets the ITRS clock speed requirement (i.e. 2-D SGSOI runs at $1.2GHz$ for 180nm generation) and use the critical path delay as the relative speed measurement among circuits.

From Fig. 8 we observe that DGSOI circuits consistently show better performance than SGSOI circuits. DGSOI can be clocked at $13\% - 20\%$ higher speed than the corresponding SGSOI circuits due to its higher drive current.

Moreover, substantial performance improvement is obtained with multi-device-layer integration. Most of the circuits can be clocked at rates double or even triple those of 2-D. For interconnect-dominated circuits, the delay reduction by multi-device-layer integration is significant.

Fig. 9 further plots the clock speed for all technology generations. DGSOI and multi-device-layer circuits demonstrate significantly better performance across all technology nodes. multi-device-layer integration shows 2 or 3 technology generation ad-

Table 2: Parameters for High Performance MPUs over Technology Generations.

Year Technology Nodes	1999 180nm	2002 130nm	2005 100nm	2008 70nm	2011 50nm	2014 35nm
Gate Length (L_n, L_p) (nm)	140	85	65	45	32	22
Gate Oxide Thickness (t_{of}) (nm)	2.5	1.9	1.5	1.2	0.8	0.6
Channel Doping (N_a) $(10^{18}\,cm^{-3})$	1.5	2.5	6.0	9.0	15	25
Supply Voltage (V_{dd}) (V)	1.8	1.5	1.2	0.9	0.6	0.6
Performance (f_{clk}) (MHz)	1200	1600	2000	2500	3000	3600
Chip Size (mm^2)	450	509	622	713	817	937
Transistor Count	22M	67M	180M	546M	1560M	4320M
Gate Pitch (μm)	9.0	5.5	3.7	2.3	1.4	0.9
Wiring Aspect Ratio	2.2					
Wiring Resistivity $(\mu\Omega - cm)$	3.3					
Wiring Capacitivity (pF/cm)	2					

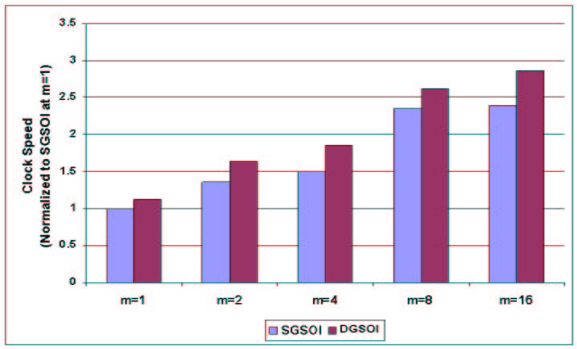

Figure 8: Clock speed with respect to various number of device layers for SGSOI and DGSOI circuits.

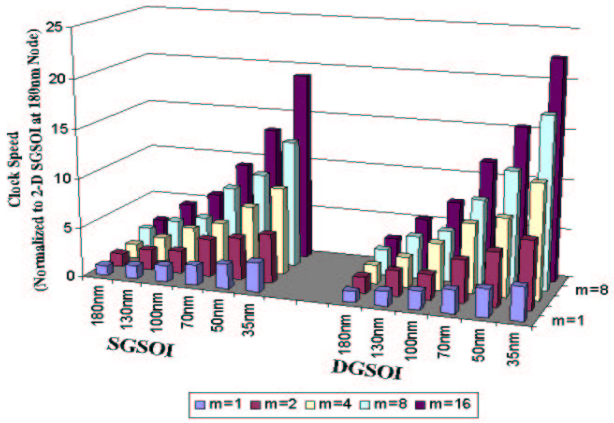

Figure 9: Clock speed over technology generations for various numbers of device layers.

vantage over conventional 2-D integration. We therefore conclude that multi-device-layer integration, together with DGSOI transistors, can be a serious contender for future high performance applications.

It should be noticed that although repeaters are not considered in our performance evaluation, including repeaters for delay estimation can be easily done using the approach shown in [4, 10].

4.2 Power Dissipation

In CMOS digital circuits, power dissipation consists of dynamic and static components. Ignoring power dissipation due to direct-path short circuit current, the total average power dissipation of a CMOS inverter is given by

$$P_T = P_{dynamic} + P_{static} = \frac{1}{2}(activity \times C_L)V_{dd}^2 f_{clk} + I_{off}V_{dd} \quad (13)$$

where *activity* is defined as the average number of switching events per clock cycle. I_{off} denotes the subthreshold leakage current, which is given by Equations (4) or (8). C_L is the sum of the gate and interconnect capacitance.

While DGSOI circuits show better performance than SGSOI circuits, DGSOI circuits dissipate more energy due to the added back gate capacitance. It is estimated that DGSOI circuits consume about 5% more power than corresponding SGSOI circuits, as can be seen from Figs. 10 and 11, where the power consumptions for an individual gate and for the whole chip are plotted. In estimating the power consumption, we assume that the supply voltage remains the same within the technology generation regardless of the number of device layers. Therefore, the power due to gate capacitance is the same for any number of device layers in the same technology generation. Based on our estimation, power consumption is still dominated by the gate capacitance. However, power consumed by interconnects is becoming substantial, consuming about 15% to 25% of the total power. This is not an insignificant portion and should call for our attention.

Despite the continuing reduction of power consumption in each gate, the total power for the whole system increases over technology generations due to the continual increase in the transistor count. Nevertheless, 3-D integration can provide a relief, as shown in Figs. 10 and 11. This mainly comes from the reduction of the interconnect capacitance, since we do not alter the device or circuit structures.

However, we observe that there is a limit on how much reduction can be achieved by multi-device-layer integration. In fact, integrating more device layers may increase the power consumption. While the horizontal wire capacitance is reduced by multi-device-layer integration, the vertical wire capacitance increases. For a small number of device layers, the decrease of horizontal wire capacitance overrides the increase of the vertical wire capacitance. Therefore, the total interconnect capacitance decreases, so does the power consumption. However, with a large number of device layers, the decrease of horizontal wire capacitance slows down while the rate at which the vertical wire capacitance increases almost remains the same. Thus, the total wire capacitance increases. This in turn increases the power consumption.

4.3 Power-Delay Product

Power-delay product ($PDP = T_c \times P_T$) is a common measure of circuit performance. Despite the higher power consumption of DGSOI circuits, the power-delay product of DGSOI is lower than

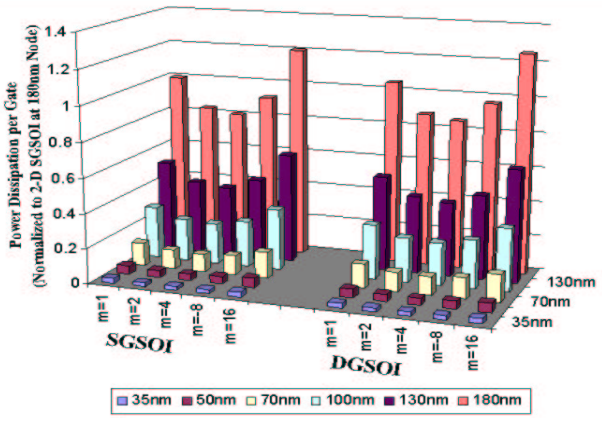

Figure 10: Average power consumption for an individual gate over technology generations for various numbers of device layers.

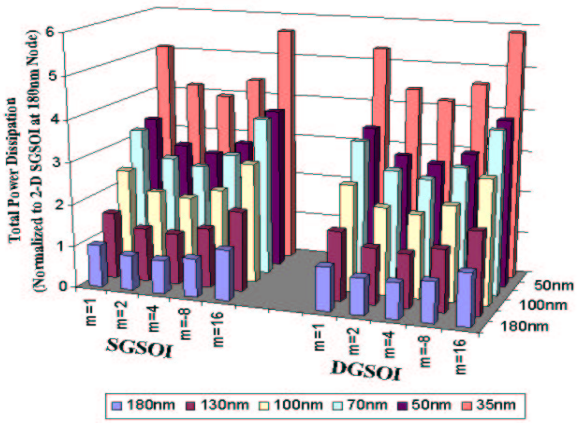

Figure 11: Total power consumption for the whole chip over technology generations for various numbers of device layers.

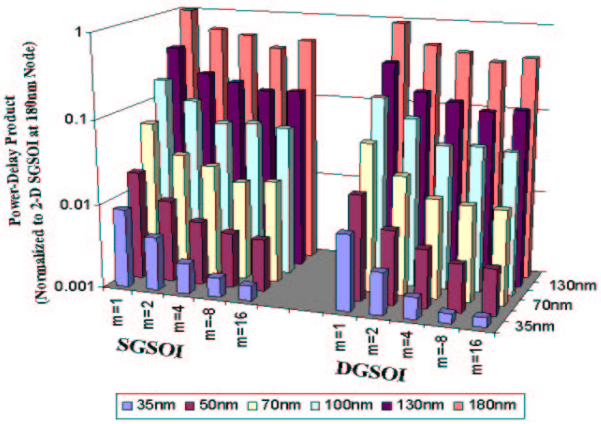

Figure 12: Power-delay product over technology generations for various numbers of device layers.

the corresponding SGSOI circuits. Fig. 12 plots the power-delay product over technology generations for various number of device layers. We observe that the power-delay product of DGSOI circuits is as much as 8% lower than SGSOI circuits. This makes DGSOI circuits very attractive for lower power and higher performance applications.

Multi-device-layer integration also achieves better power delay product. As we showed in the previous sections, multi-device-layer integration can have higher circuit performance and low power dissipation, thus achieving better power-delay product. From Fig. 12, we again observe that there exists an optimum number of device layers that gives the best power-delay product. This implies that there is a limit on vertical integration of device layers in terms of power dissipation and power-delay product.

5. CONCLUSIONS

In this paper, we explore device structures and interconnect architectures for 3-D integrated SOI circuits. Based on the projections of ITRS, SGSOI and DGSOI circuits with various number of device layers are compared in terms of circuit speed, power dissipation, and power-delay product. Their applications for future technology generations are investigated. Results shows that, compared to SGSOI circuits, DGSOI can have up to 20% performance and 8% power-delay product gain. Moreover, for interconnect-dominated circuits, multi-device-layer integrated circuit offers significant performance improvement. Multi-device-layer integration can have 2 or 3 technology generation advantage over 2-D. We also show that multi-device-layer integration offers power and power-delay product reduction. Therefore, we conclude that 3-D integration can be a viable solution for future low power and high performance applications.

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