Modeling and Analysis of Differential Signaling for Minimizing Inductive Cross-Talk

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Abstract

Many physical synthesis tools interdigitate signal and power lines to reduce cross-talk, and thus, improve signal integrity and timing predictability. Such approaches are extremely effective at reducing cross-talk at circuit speeds where inductive effects are inconsequential. In this paper, we use a detailed distributed RLC model to show that inductive cross-talk effects are substantial in long busses associated with 0.18 micron technology. Simulation experiments are then used to demonstrate that cross-talk in such high speed technologies is much better controlled by re-deploying interdigitated power lines to perform differential signaling.

1 Introduction

In deep sub-micron (DSM) technologies, critical feature size continues to shrink and now nearly 100 million transistors can be packed into a single die. The availability of many layers of low resistance metal (Cu) interconnects makes routing of such complex chips possible, but demand for higher system performance reduces timing slacks and puts added constraints on timing accuracy and predictability. This makes the optimization of interconnects extremely difficult. Typically, performance is achieved by routing global interconnects using upper metal layers and wide metal lines to reduce resistance. To keep resistance low, top metal layer thickness have not scaled with newer technologies, which has led to an increase in coupling capacitance, and therefore, has created cross-talk problems. To reduce coupling between adjacent lines the commonly used techniques are widening metal lines, shielding, buffer insertion, and increasing the wire to wire spacing. These techniques, especially shielding, handle capacitive coupling noise problems very successfully.

In the next section, we evaluate the noise characteristics of standard cross-talk avoidance strategies including: shielding, widening metal lines, increasing wire separation, and buffer insertion. RC models of the interconnect are analyzed first then inductive effects are included to show that in 0.18 micron technology, and beyond, inductance has a first order effect on cross-talk noise. Assuming the same set of timing constraints applies for all strategies, we show that standard cross-talk avoidance strategies are of limited effectiveness. In section 3, we present results on using differential signaling, and show that such an approach is much more effective at reducing cross-talk when inductive effects are included.

In section 4, we compare the performance of differential signaling to shielding as a means of reducing cross-talk noise, and show that differential signaling has much superior noise characteristics even for much tighter timing budgets than other standard cross-talk avoidance strategies. In section 5, we show that differential signaling superiority in noise reduction is due to its insignificant noise radiation, and also, due to its superior noise immunity.

2 Standard Cross-Talk Noise Reduction Techniques

For our simulation and analysis, we used a major foundry's 0.18μ process. The metal lines were implemented in metal 6 with all lines having a metal width of 3μ and a metal to metal spacing of 1.5μ consistent with typical high level metal implementations of high performance global busses. The only exception to that are the test cases where the metal width or the metal spacing was intentionally varied as part of the experiment. In all experiments, we sandwiched the data bus between a VDD line and a VSS line each 15μ wide to provide a return path for the current flowing in the buses.

In all test cases, we used simple buffers (scaled inverters) for drivers and receivers implementation in the standard cases, and a differential driver-receiver pair for the implementation of differential examples. In order to be consistent in our comparison between the various cases considered, we maintained the same timing constraint of a propagation delay of 0.35ns from input to output. We always used the weakest drivers sufficient for meeting that timing constraint in all the test cases to make sure that the drivers are not themselves a source of noise. Also, we maintained an input capacitance of approximately 10ff. All receivers were loaded with a moderate load of 0.1pf.

We used a distributed RLC [1] model to model the interconnects where FastCap [2] was used to model the interconnect capacitance and FastHenry [3] was used to model both the resistance and the inductance of the interconnects.

In order to test for the worst case noise generated on the 8-bit data bus, 3000μ long, standard single ended bus shown in Figure 1, we applied a 50 psec rise time step to all the inputs except the one in the middle. In Figure 3, simulation results using Hspice[9] shows a totaly unacceptable

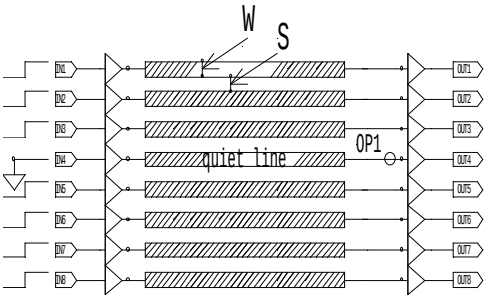

Figure 1: A 8-bit global bus 3000μ long. Metal line width $W = 3\mu$, metal line to metal line spacing $S = 1.5\mu$. The bus is sandwiched between a VDD line and a VSS line each 15μ wide. The driver and receiver of each line is a standard CMOS buffer.

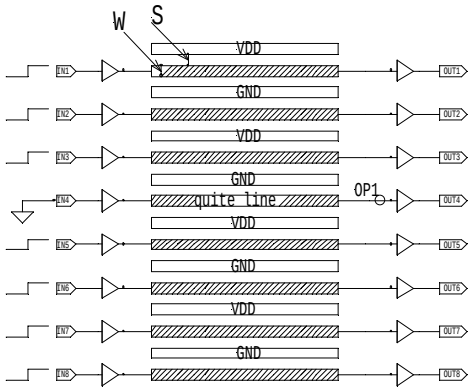

Figure 2: A 8-bit global bus 3000μ long. Metal line width $W = 3\mu$, metal line to metal line spacing $S = 1.5\mu$. A shield line of alternating VSS/VDD connectivity is inserted between alternating signal lines.

voltage glitch of 1.17V. Such a glitch could cause erroneous switching and logic failures. In order to solve this cross-talk noise problem, we tested the most popular cross-talk noise reduction techniques against this example.

2.1 Shielding Technique

Shielding is one of the most successful existing noise reduction techniques [4,5]. The technique, as shown in Figure 2, interdigitates signal lines with Vdd or Vss alternatively. Figure 3 shows that even when we use the shielding technique, a voltage glitch of 0.54V will still appear. Figure 4 shows that when the inductance is not modeled, the shielding technique appears to solve the cross-talk problem perfectly as only a 0.03V voltage glitch is generated. This is because the shielding technique is capable of screening signal lines and thus eliminating capacitive coupling. However, due to the long range of current return paths, shielding is capable of screening only part of these signals current return paths, and thus shielding might eliminate only part of the inductive coupling.

2.2 Widening Metal Lines

Widening signal metal width is one the techniques that is mainly used to reduce capacitive cross-talk noise by increasing the signal capacitance to the ground. Figure 5 shows that the generated noise was reduced by not more than 20% after the wire width was increased from 3μ to 7.5μ. In this example we have widened the interconnects and kept the separation distance, S, at 1.5μ so that the total area taken by the data bus is the same as the one used in the shielding technique. Other than this modest noise improvement, this technique tends to increase the delay as the area capacitance increases.

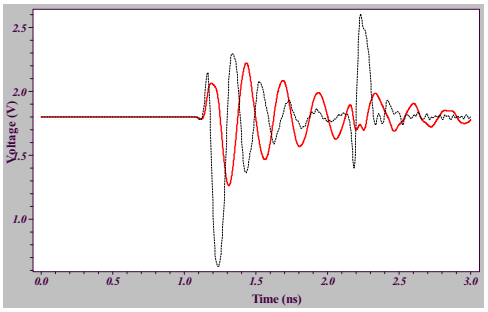

Figure 3: Solid graph represents the noise signal in the shielded example measures at OP1 in Figure 2 (peak noise=0.54V). Dotted graph represents the noise signal in the standard single ended example measured at OP1 in Figure 1 (peak noise=1.17V). Note that the inductance of the interconnect is modeled.

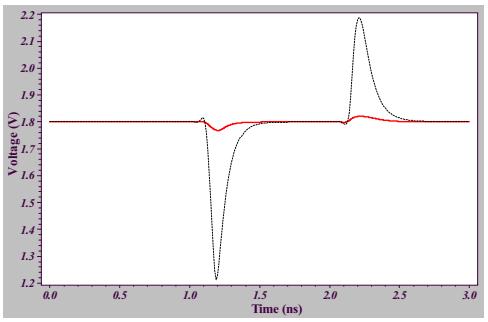

Figure 4: Solid graph represents the noise signal in the shielded example measures at OP1 in Figure 2 (peak noise=0.03V) when the inductance of the interconnect is **not** modeled. Dotted graph represents the noise signal in the standard single ended example measured at OP1 in Figure 1 (peak noise=0.59V) when the inductance of the interconnect is **not** modeled.

2.3 Increasing Metal to Metal Separation

Increasing the separation distance between signal lines is a very well known technique to reduce cross-talk noise. In order to test this method, we simulated the configuration shown in Figure 1 where we kept the signal width at 3μ and increased the separation distance, S, such that the total area consumed by the structure will be the same as the one consumed by shielding. Figure 6 shows that the generated noise was reduced to 0.82V. This is not as good as the shielding technique. Note that when neglecting the inductance, this technique reduced the cross-talk noise to 0.21V which shows that this technique can be successful if no inductive coupling is involved. This is due to the fact that although when increasing line separation, capacitive coupling decreases with

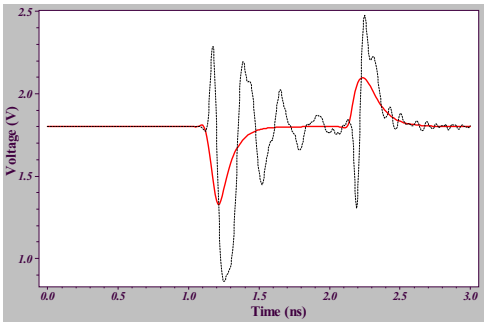

Figure 5: Noise signal measured at OP1 in Figure 1 for a bigger width $W = 7.5\mu$ and $S = 1.5\mu$. Solid graph represents noise when inductance is NOT modeled(peak noise=0.47V). Dotted graph represents noise when inductance is modeled (peak noise=0.94V).

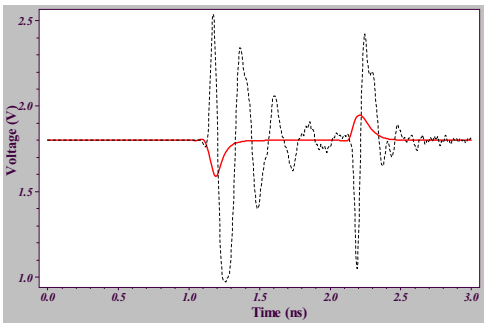

Figure 6: Noise signal measured at OP1 in Figure 1 for a bigger spacing $W = 3.0\mu$ and $S = 5.5\mu$. Solid graph represents noise when inductance is NOT modeled (peak noise=0.21V). Dotted graph represents noise when inductance is modeled (peak noise=0.82V).

distance, loop inductance increases, and thus the technique fails.

2.4 Buffer Insertion Technique

Buffers are often inserted in long interconnect routes to reduce cross-talk noise[6]. Buffer insertion typically reduces cross-talk noise but often degardes the performance due to the additional delays of the inserted buffers. In order to test the buffer insertion method with the standard single-ended bus configuration in Figure 1, we divided each interconnect line in the bus into two 1500μ segments with a buffer instered in between the two segemnets. We used the weakest buffers and drivers to meet our delay target of 0.35ns. Figure 7 shows that the generated cross-talk noise was reduced to 0.87V which is worse than that of the shielding technique. When inserting two buffers instead of one buffer in each interconnect line of the bus in figure 1, the delay has deteriorated significantly and the delay constraint could not be met. Even when doubling the delay constraint to 0.7ns, the cross-talk noise was 0.62V which is still worse than shielding.

3 Differential Signaling

As we discussed in section 2, all of the standard noise reduction techniques failed to give satisfactory noise reduction

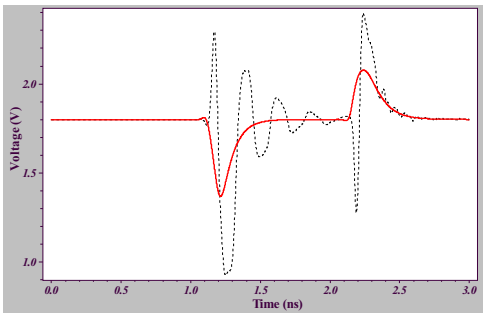

Figure 7: Noise signal measured at OP1 in Figure 1 with each interconnect line in the bus is divided into two 1500μ segments with a buffer instered in between the two segemnets. Solid graph represents noise when inductance is NOT modeled (peak noise= 0.43V). Dotted graph represents noise when inductance is modeled (peak noise=0.87V).

results for a high performance global bus. This was mainly due to the presence of inductance in this problem and these techniques are more suited for capacitance dominated problems. Recently [7], there has been increased interest in low swing signaling, but inductive effects have not been included in previous studies. In this section we will discuss the use of limited swing differential signaling and how it can significantly reduce cross-talk noise.

3.1 Circuit Implementation for the differential transmitter and reciever

The differential driver used is shown in Figure 8, The driver consists of a very low input capacitance inverter and of a transmission gate generating a balanced delay signal and signal-bar that drive two matched buffers generating the differential signal. The buffers are simple inverters with active current feedback in the form of an always -on transmission gate. The buffer with the feedback is essentially a simple op-amp with a virtual grounded input and a low voltage gain. The active feedback provides maximum flexibility in controlling the delay, swing, and centering of the differential signal with respect to vdd and gnd. Also the very low input capacitance of the pre-driver makes this driver very useful in tight timing budgets and shallow pipeline architectures. Similar drivers have been used for very high frequency RF applications [8]. The driver we implemented had a swing of 300mV with a low level of 0.7V and a high level of 1.0V. The input capacitance of the driver was 10ff. The receiver, shown in Figure 9, was a standard static differential receiver with a low impedance current source for stability against injected noise and it drove a load of 100ff (ten standard loads equivalent).

3.2 Differential Bus

We next investigated the use of differential signaling for the whole bus, as shown in Figure 10, and we observed the outputs OP1 and OP2 of the "quiet" differential signal and signal-bar in the middle of the bus at the end of the 3000μ differential line. Figure 11 shows that the two points OP1 and OP2 are almost always in phase. This makes the difference OP1-OP2 very small. This difference is the effective noise seen by the differential receiver. Figure 12 shows that by using this differential bus the effective noise seen at the

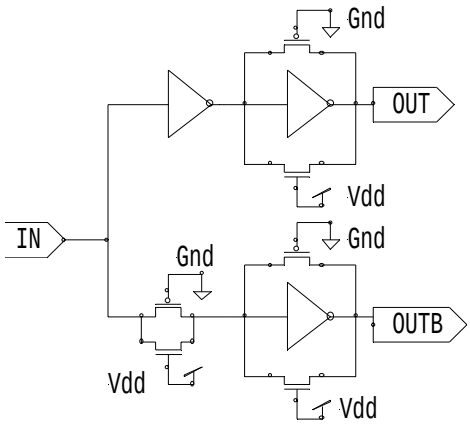

Figure 8: Limited Swing Differential Transmitter

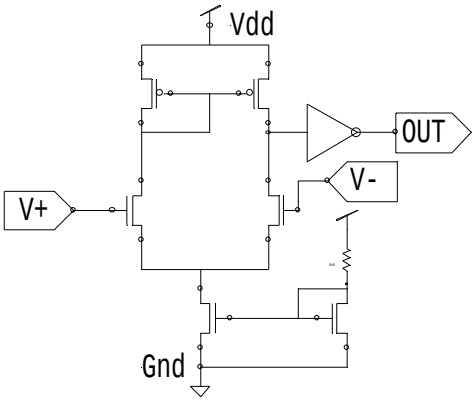

Figure 9: Differential Receiver

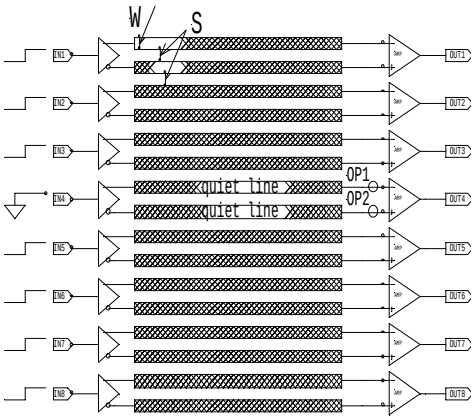

Figure 10: A 3000μ long global bus with 8-bits differential. The driver of the differential signals is a limited swing differential driver and the receiver is a differential receiver. Metal line width $W = 3\mu$, metal line to metal line spacing $S = 1.5\mu$. The 16 line bus is sandwiched between a VDD line and a VSS line each 15μ wide.

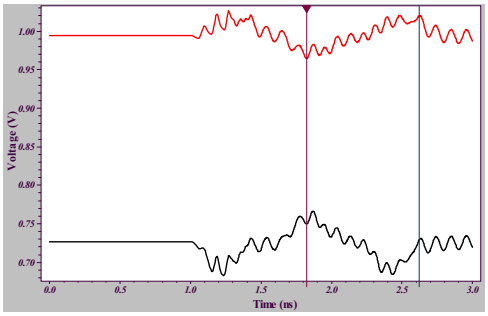

Figure 11: The signal on points OP1 and OP2 of the differential receiver in Figure 10.

input of the differential receiver is only 53mv peak, thus, reducing the cross-talk noise by more than one order of magnitude compared with any of the cross-talk noise reduction techniques discussed in section 2.

4 Timing and Noise Comparison between differential signaling and shielding

In this section, we compare the performance of differential signaling to shielding, having shown in section 2 that shielding is the most effective among the standard noise reduction techniques. In the previous two sections, we showed that when maintaining the same timing constraint of a propagation delay of 0.35ns on the global data bus, the differential bus exerted a worst case cross-talk noise of only 53mv. Thus, by using this differential bus, the cross talk noise was reduced by more than 10 times compared to the shielding technique. In order for the shielding technique to produce a better noise performance, the delay constraint on the data bus has to be further relaxed. For example: the delay constraint has to be tripled to 1.05 nsec in order for the noise shown on the shielded bus to be 60mv which is still more than that of the differential bus. Thus, by using this differential bus, which takes no more area than that used by the shielding technique, the cross-talk noise was reduced by

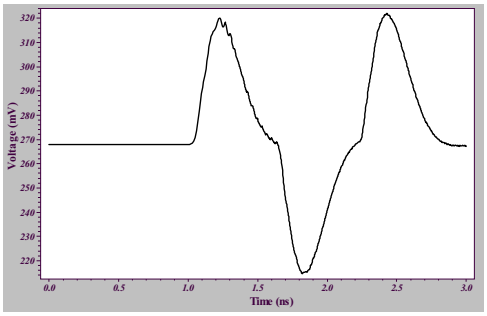

Figure 12: The difference between the signals on points OP1 and OP2 of the differential in Figure 10. This represents the input noise signal to the differential receiver (maximum cross-talk noise is only 53mv).

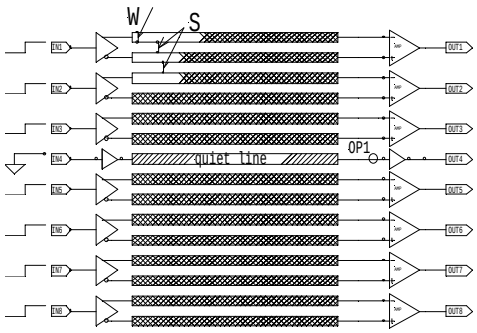

Figure 13: A 8-bit global bus with 7-bits differential (14 signal lines) 3000μ long. $W = 3\mu$, $S = 1.5\mu$. The non-differential (standard) bit signal is placed in the middle of the differential signals.

more than an order of magnitude for the same timing constraint. Also, the differential bus still produced a better noise performance over the standard shielded bus even when the timing budget for the standard shielded bus was tripled.

5 Why Differential Signaling is superior

We devised two experiments to sort out if differential signaling is good because it is inherently immune to noise or because it does not radiate significant electromagnetic interference that can disturb neighbors.

5.1 Low Noise Generation

Figure 13 shows a setup where the bus is driven differentially. However, the "quiet" line in the center is standard single ended. We observed the output (OP1) of the quiet line with the remaining 7 differential pairs switching. Figure 14 shows the quiet line to have a cross-talk noise peak of 38mV, which asserts that differential signaling does not radiate significant electromagnetic interference. This is mainly because a differential transmitter needs to drive a load to a voltage swing of less than 300mv, compared to 1.8V for a standard driver. Therefore for the same latency, differential drivers tend to be much smaller than standard drivers, which results in a significantly lower di/dt, and therfore lower inductive noise generated. This has special positive implications. It makes routing differential signals over sensitive areas such

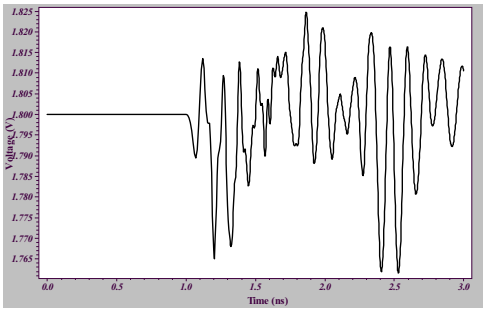

Figure 14: The noise signal on point OP1 in Figure 13. (peak noise is only=38mv).

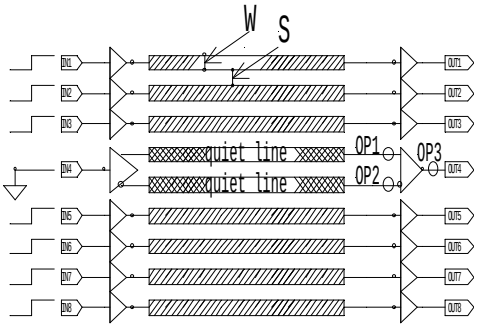

Figure 15: An 8-bit, 3000μ long, global bus of 7 standard signals and a differential signal located in the center of the bus. $W = 3\mu$, $S = 1.5\mu$. The bus is sandwiched between a VDD line and a VSS line. The driver of the differential signal is a limited swing differential driver and the receiver is a differential receiver. The drivers and receivers of all the standard bits are standard CMOS buffers.

as RAMS possible. Generally, routing over a RAM block is prohibited for the fear of destructive coupling effects.

5.2 Noise Immunity

The second experiment, shown in Figure 15, had all the switching signals standard non-shielded lines with the differential signal in the middle as the quiet line. Although the single ended lines caused a high level of coupling on each of the differential lines, OP1 and OP2, as shown in Figure 16, the two differential lines moved together keeping the difference between them not exceeding 83mV. This reflected an insignificant 4mV on the differential reciever output, OP3, as shown in Figure 17.

In order to compare the noise immunity of the differential with that corresponding to the shielding, we replaced the differential bus in the middle of the single ended bus in Figure 15 with a regular standard single ended line along with a shielded line, as shown in Figure 18. Figure 19 shows a voltage cross-talk glitch on the input of the standard single ended receiver, OP1, of 1.12V, which reflected a final output noise of 360mV on OP2 in Figure 18. This experiment proves that differential signaling is much more immune to injected noise as the noise glitches on both the input and the output of the differential receiver were more than an order of magnitude less than the repective glitches on the shielded single ended reciever. This makes differential signaling a very good solution for critical nets, as it provides superior noise immunity along with speed.

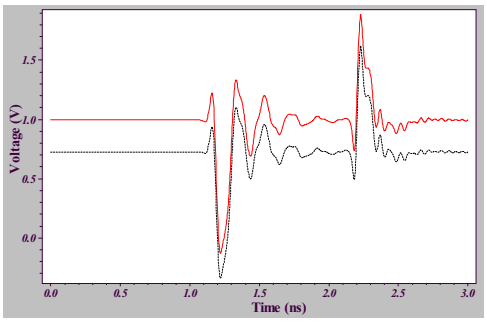

Figure 16: The input signals to the differential receiver, OP1 and OP2 in Figure 15.

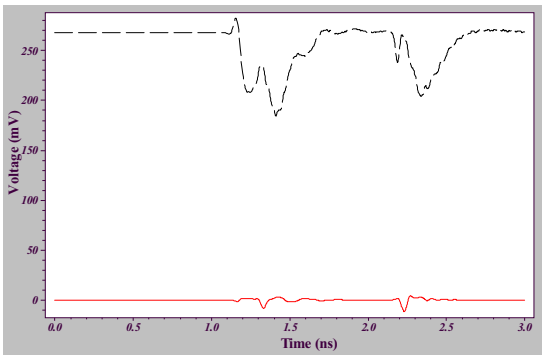

Figure 17: Dotted graph represents the difference between the signals on points OP1 and OP2 of the differential receiver in Figure 15. This represents the input noise signal to the differential receiver (peak input noise is 83mv). The solid graph represents the output of the differential receiver, OP3, in Figure 15. (peak output noise is only 4mv).

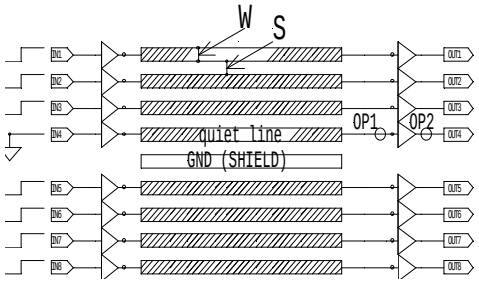

Figure 18: An 8-bit global bus 3000μ long. $W = 3\mu$, $S = 1.5\mu$. A grounded shield wire of width $W = 3\mu$ is inserted in the middle of the bus. The bus is sandwiched between a VDD line and a VSS line. The driver and receiver of each line is a standard CMOS buffer.

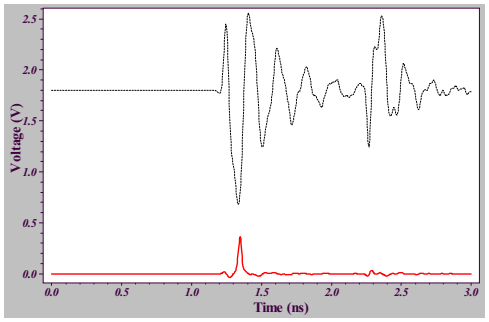

Figure 19: Input and output noise signal to the middle standard receiver buffer in Figure 18. Peak noise on buffer input OP1=1.12V. Peak noise on buffer output OP2=360mV.

6 Conclusions

We have shown that noise reduction techniques such as increased line separation, widening metal lines, buffer insertion, and shielding perform well when only capacitive coupling is considered. However, when inductive effects are modeled, simulations show there is still substantial cross-talk. We then demonstrated that low swing differential signaling is both noise immune and generates less electomagnetic noise.

In this paper, we have focused on the noise immunity and noise generation issues in DSM interconnect using limited swing differential signaling. We showed that differential signaling has superior noise characteristics with no area penalty. Also, the fact that differential signaling generates much less noise than standard cross-talk avoidance techniques makes it possible to route over noise sensitive areas.

References

[1] A. Deutsch et. al., " When are Transmission-Line Effects Important for On Chip Interconnections ?," IEEE Transaction on MTT, vol. 45, No 10, pp. 1836-1846, October 1997.

[2] K. Nabors and J. White, " FastCap: A Multipole - Accelerated 3-D Capacitance Extraction Program," IEEE Transaction on Computer-Aided Design , pp. 1447-1459, November 1991.

[3] M. Kamon, M. Tsuk, and J. White, " FastHenry: A Multipole-Accelerated 3-D Inductance Extraction Program," IEEE Transaction on MTT, vol. 42, No 9, pp. 1750-1758, September 1999.

[4] Y. Massoud, S. Majors, T. Bustami, and J. White," Layout Techniques for Minimizing On-Chip Interconnect Self Inductance," ACM/IEEE DAC 1998.

[5] S. Khatri, A. Mehrotra, R. Brayton, A. Sangiovanni-Vincentelli, and R. Otten," A Novel VLSI Layout Fabric for Deep Sub-Micron Applications," ACM/IEEE DAC 1999.

[6] C. Alpert, A. Devgan, and S. Quay, " Buffer Insertion for Noise and Delay Optimization," ACM/IEEE DAC 1998.

[7] H. Zhang, V. George, and J. Rabaey, " Low-Swing On-Chip Signaling Techniques: Effectiveness and Robustness," IEEE Transaction on VLSI Systems, vol. 8, No 3, pp. 264-272, June 2000.

[8] H. Shin, D. Hodges, "A 250-Mbit/s CMOS Crosspoint Switch", IEEE Journal of Solid State Circuits, vol 24, no.2, April 1989.

[9] Hspice, Avanti Corporation, 2000.