Built-In Self-Test for Signal Integrity

Mehrdad Nourani and **Amir Attarha**

Center for Integrated Circuits & Systems
The University of Texas at Dallas
Richardson, TX 75083-0688

{nourani,attarha}@utdallas.edu

Abstract

Unacceptable loss of signal integrity may harm the functionality of SoCs permanently or intermittently. We propose a systematic approach to model and test signal integrity in deep-submicron high-speed interconnects. Various signal integrity problems occurring on such interconnects (e.g. crosstalk, overshoot, noise, skew, etc.) are considered in a unified model. We also present a test methodology that uses a noise detection circuitry to detect low integrity signals and an inexpensive test architecture to measure and read the statistics for final observation and analysis.

1. INTRODUCTION

Signal integrity is the ability of a signal to generate correct responses in a circuit. According to this informal definition, a signal with good integrity has: (*i*) voltage values at required levels and (*ii*) level transitions at required times. For example, an input signal to a flip-flop with good signal integrity arrives early enough to guarantee the setup and hold time requirements and it does not have spikes causing undesired logic transition. The technology size is estimated to shrink to 70 *nm* and the frequency to increase to 4 *GHz* by year 2006 [1]. This growth magnifies the problem of integrity loss, specifically when high-speed communications among cores in system-on-chips (SoC) are required.

By nature, digital systems are tolerant of many signal integrity deficiencies. However, sufficiently large integrity problems (e.g. large delays or large voltage swings) can cause systems to fail permanently or intermittently. Particularly, the intermittent failures, caused by the lack of signal integrity, are very difficult to debug or test due to their unpredictable nature (e.g. depending on data, parasitic values, interaction, environment, etc.). Such intermittent failures often occur in the field rather than during manufacturing testing; thus, testing SoCs for signal integrity is of great importance.

Our main contribution is an on-chip mechanism to detect signal integrity problems in high-speed SoCs. In the driving side of the interconnect, we show that the conventional TPGRs (test pattern generation register) can generate effective patterns with reasonable cost. In the receiving side of the interconnect, special cells monitor signals received from the system interconnect and record the occurrence of signal entering the vulnerable region over a period of operation. The information accumulated by these cells will be eventually sent out for final test analysis, reliability judgment and diagnosis.

2. BACKGROUND

SoC testing has been discussed from different perspectives in the literature [2][3][4]; none has directly addressed the SoC signal integrity issue. While it is impossible, and often unnecessary, to eliminate all noise, the signal integrity must be analyzed and tested to assure correct system functionality. One of the challenges facing test engineers is knowing when they may confront the signal integrity problems. Various signal integrity problems (termed also as "noise", "distortion", "dispersion", "jitter", etc. in the literature) have been previously studied for radio frequency (RF) printed-circuit boards by researchers. Currently, many RF aspects are being revisited for their on-chip effects in high-speed deep-submicron VLSI chips. The most important ones are: 1) *Crosstalk* (signal distortion due to a fast dV/dt in one net and cross coupling effects between signals) [5][6], 2) *Overshoot* (signal rising momentarily above the power supply voltage or below ground) [7][8], 3) *Reflection* (echoing back a portion of a signal when it reaches the end of interconnect), 4) *Electro-magnetic interference* (that happens in high and ultra-high frequencies resulting from the antenna properties) [9], 5) *Power supply noise* (due to inadequate power grid) [10]; and 6) *Signal skew* (the difference in arrival time of one source signal to different receivers) [11][12].

There is a long list of possible design/fabrication solutions to enhance the signal integrity on the interconnect. None, of course, guarantees to resolve the issue perfectly. These solutions include: 3-D layout modeling and parasitic extraction [13], accurate RLC simulation of on-chip power grid [11], using decoupling capacitors to limit the maximum dV/dt [14][10] and to improve IR-drop [11][15], inserting repeaters/buffers on the interconnects [13] and shielding wires (e.g. grounding every other line) [16].

3. SIGNAL INTEGRITY MODEL

3.1 Interconnect Model

Signal integrity problems originate from the circuit interconnects. A wire not only serves as a conductor of electrons but also includes parasitic resistor (at low frequencies), capacitor (at mid-range frequencies), inductor (at high frequencies) and antenna (at very high frequencies), all of which can affect signal integrity. In low and mid-range frequencies, common in the past, the *RC* delays have been the dominating factors in the global interconnect delay and distortion. Inductance (L) effects are becoming increasingly important as frequency of operation increases.

There are many efficient distributed models in the literature [17][18][19]. Figure 1 shows an accurate equivalent RLC circuit for several parallel interconnect lines [17][20]. This model comprises resistance (R), partial self inductance (L) and capacitance (C) for each segment, mutual inductances (M) and coupling capacitance (C_c) between all pairs of parallel components. The values of distributed R, L and C depend on many factors including the operating frequency, length and technology. The number of segments can be selected based on the

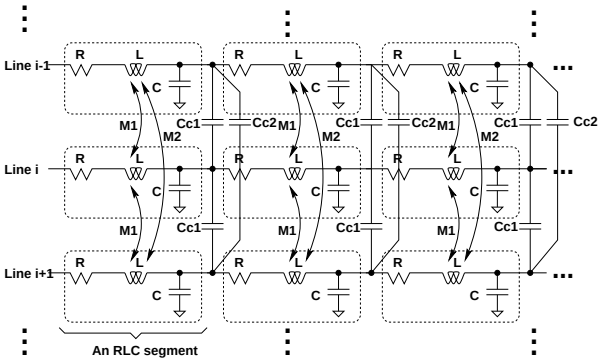

Figure 1: An interconnect model.

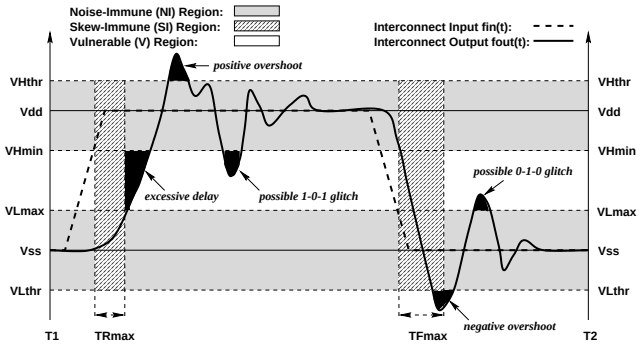

Figure 2: Practical view of integrity loss (IL) metric.

length of the interconnect and the operating frequency. All results reported in this work are based on this distributed RLC model [17][20].

3.2 A Model for Signal Integrity

True characteristics of a signal is reflected in its waveform. Recent interconnect simulation, design and optimization methods not only consider peak voltage and delay, but also take into account the signal waveform [21][25]. In reality, electronic components can tolerate certain level of noise. For example, a CMOS gate interprets any voltage in the $[V_{Hmin}, V_{dd}]$[1] range as logic 1 and any voltage in the $[V_{ss}, V_{Lmax}]$[2] range as logic 0. Moreover, many of these circuits are designed to tolerate certain amount of delay, i.e. T_{Rmax} for rising delay and T_{Fmax} for falling delay.

In real-world circuits there are *noise-immune* (NI) regions that tolerate certain level of voltage swing and *skew-immune* (SI) regions that tolerate certain level of delay. Any portion i of a signal in *vulnerable* (V) region (i.e. located out of NI and SI regions) indicates the integrity loss and its accumulated value forms the *integrity loss* (IL) metric:

$$IL = \sum_{i \in \text{V-region}} \left(\int_{T_{i1}}^{T_{i2}} |K - f_{out}(t)| \cdot dt \right)$$

where $K \in \{V_{Hmin}, V_{Lmax}, V_{Hthr}, V_{Lthr}\}$. This concept has been shown graphically in Figure 2. The shaded and unshaded (white) strips show the immune and vulnerable regions, respectively. The black areas illustrate portions of the output signal in the vulnerable region and indicate the integrity loss. The signal portions in the V-region correspond to unacceptable distortion because the receiving core may misinterpret the signal (in terms of logic level and/or delay) and thus the system functionality will be subject to error.

This paper focuses on a mechanism to detect signals that exit the NI-region. Leaving the NI-region not only causes error in functionality

[1] V_{Hmin} is the minimum input voltage recognized as *High*.
[2] V_{Lmax} is the maximum input voltage recognized as *Low*.

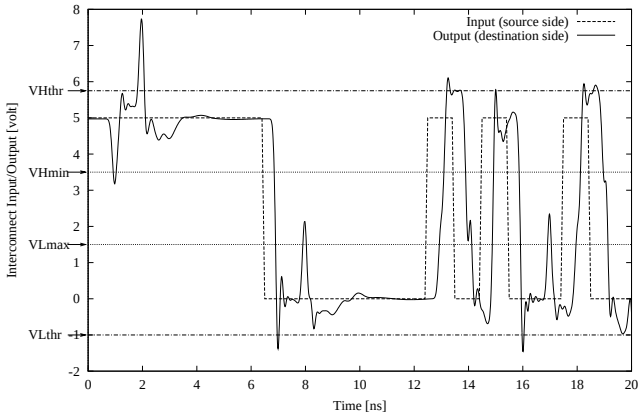

Figure 3: SPICE simulation of an SOC interconnect in 1 *GHz*.

(ringing), but also repeated overshoots are known to inject high-energy electrons and holes (also called *hot-carriers*) into the gate oxide that ultimately cause permanent degradation of MOS transistors' performance and reliability [7][8].

Figure 3 shows the snapshot of one of the bus lines between two cores ($V_{dd} = 5$ *Volt*) for 20 patterns (20 *ns*) near the receiving core. The signals are obtained by using SPICE [23] for a clock frequency of 1 *GHz* with rise and fall time of $T_r = T_f = 0.1$ *ns* and the interconnect length of 10 *mm*. The experiment clearly confirms the concern that the parasitic RLC, crosstalk and other high-speed effects may distort the signal to a functionally-unacceptable level. For example, assuming $\{V_{Hmin}, V_{Lmax}\} = \{3.5, 1.5\}$ we have voltage vulnerability at $t = 1, 8, 17$ due to potential ringing. Similarly, assuming $\{V_{Hthr}, V_{Lthr}\} = \{5.7, -1.0\}$ potential vulnerability at $t = 2, 7, 13, 16, 18$ exists.

4. TEST PATTERNS GENERATION

Depending upon the functionality of the core feeding the interconnect under test and the acceptable overhead and accuracy, we can use normal-operation patterns, pseudorandom patterns (e.g. TPGR) or special test pattern generation circuitry. The cost of a special test pattern generator can be justified if it creates the maximal integrity loss (i.e. the largest IL metric).

4.1 Worst Case of Signal Integrity Loss

Researchers have searched for test patterns causing the worst case of signal integrity to enhance their test quality. In [24] and [5], the worst case test patterns associated with a specific fault model (MAFM) were presented. They used the RC interconnect for test pattern generation. Techniques, such as the one reported in [24], apply identical transitions to all wires except the victim net to create maximal integrity loss in the victim wire. Six scenarios and typical test patterns used in such techniques (e.g. [24]) have been shown in Figure 4. Although this set of test patterns can test interconnects at lower frequencies where inductance is negligible, it is inadequate for higher frequencies. Our empirical evidences show that in high frequency they fail to show the true picture of integrity of a signal.

For accurate analysis, having the coupling capacitances between all wires in a distributed model (e.g. Figure 1) is necessary but not sufficient. The effect of capacitive coupling is considered local, in the sense that the coupling effects of adjacent wires are quite dominant compared to the capacitive coupling effects of far off wires [17][22]. However, the inductance has larger range effect and thus the effect of mutual inductance could be significant. As discussed in [17], the effect of coupling inductances and capacitances on a wire oppose each other. When the signal on a wire switches in one direction, the noise due to capacitive coupling affects other nearby signals in the same direction

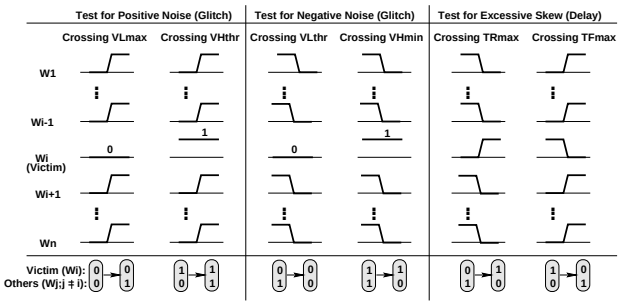

Figure 4: Creating maximal integrity loss using RC model.

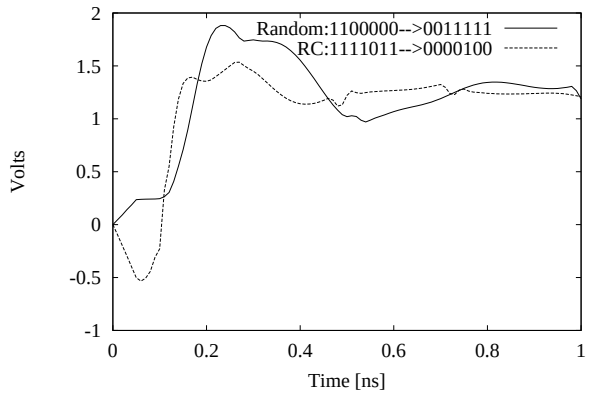

Figure 5: Comparing patterns for the worst case delay.

as that of switching while the noise due to inductive coupling is in the opposite direction. All of these make the patterns generated by RC models inaccurate and inadequate.

In what follows, we present four experiments to show the deficiency of RC model and the corresponding uniform patterns. These examples clearly show that there are scenarios for test patterns that create worse delay and/or noise on the signal and cause more integrity loss compared to those commonly reported earlier [24][17]. Thus, RLC model of interconnect needs to be consolidated for test pattern generation. We have used an RLC model of seven parallel interconnect lines (indexed "7654321") for our experimentation. The R, L and C values are extracted using accurate extraction tools [17] [26]. TISPICE has been used to simulate the complete RLC model. Typical CMOS gates are considered as driver and driven gates in two sides of the interconnect and $V_{dd} = 1.2$ Volt. Note that in the waveforms of these examples *RC* refers to the test pattern (similar to those in Figure 4) suggested by approaches that use RC interconnect modeling. We call them RC-patterns for short. Note that many random patterns stimulate integrity loss (noise) more than limited RC-patterns. We will show some statistics in Section 7.

• Example 1: Maximal Delay
Test pattern pair 1111011 $\rightarrow$ 0000100 is proposed for observing the highest potential delay on line 3 based on RC model. As shown in Figure 5, test pattern pair 1100000 $\rightarrow$ 0011111 can generate 31% more delay than the RC patterns.

• Example 2: Maximal Noise
In Figure 6, the difference between the worst case test pattern for RC model and another test data is demonstrated. In this case, the glitch on quiescent line 3 at 0 is investigated. This example shows that the worst case patterns (in terms of peak and duration of noise) for RC model are not necessarily the worst case for RLC model.

• Example 3: Mutual Effects
We believe categorizing lines as victim and aggressors is misleading

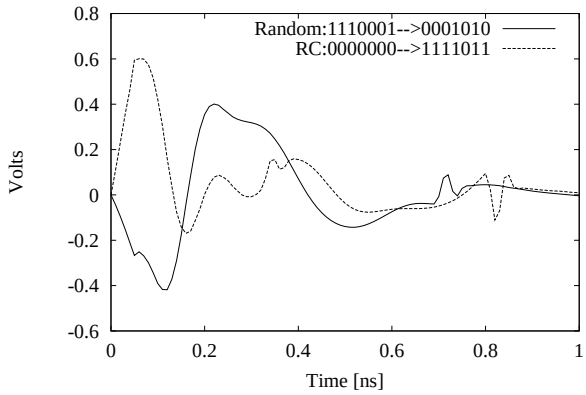

Figure 6: Comparing patterns for the maximal noise.

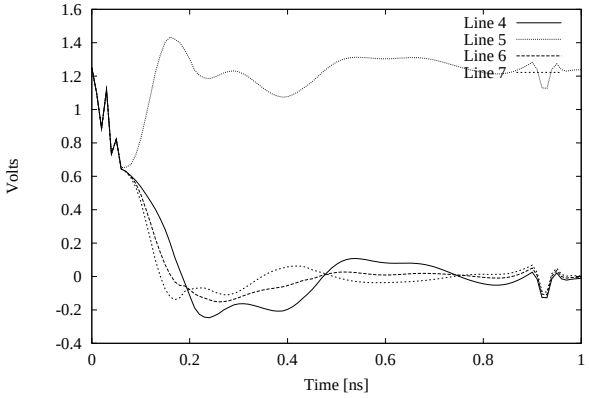

Figure 7: Mutual effects of wires.

and unrealistic. Every line (including so-called aggressors) can be affected by all other lines (including so-called victims). Although the overall effect of aggressors on victims may be larger than effect of victims on aggressors, the change on the other lines cannot be ignored. Such minor effects may cause different switching times for aggressors which eventually results in longer settling delay up to 51% as reported in [17]. Figure 7 shows an example in which line 5 is quiescent at 1 and lines 4, 6 and 7 make $1 \rightarrow 0$ transitions. As shown in the figure, they affect each other due to the inductive and capacitive couplings.

• Example 4: Oscillations
Another important phenomenon that may happen in long interconnects is oscillations. As shown in Figure 8, a particular pattern may cause oscillations on some wires, that is line 3 here. Although the voltage level of oscillation may be somewhat limited or the oscillation frequency may be too high, still such phenomenon contributes to noise and may create problems in high-speed systems.

In conclusion, due to the complexity of accurate RLC interconnect model, parasitic values and too many influential factors, finding patterns guaranteed to create the worst case scenarios for noise (integrity loss) is very much difficult and almost impractical with the current state of knowledge. Our empirical evidences indicate that random patterns are more qualified than those conjectured (e.g. RC patterns in Figure 4) to create the worst case integrity loss. Thus, we propose to use conventional TPGRs to generate pseudorandom test patterns as an efficient way to test the high-speed interconnects. We will elaborate on this issue in Section 7.

5. ON-CHIP NOISE DETECTION

This paper focuses on the NI-region and a mechanism to detect signals that leave the NI-region indicating integrity loss. Leaving the NI-region causes ringing (when voltage crosses V_{Hmin} or V_{Lmax}), or

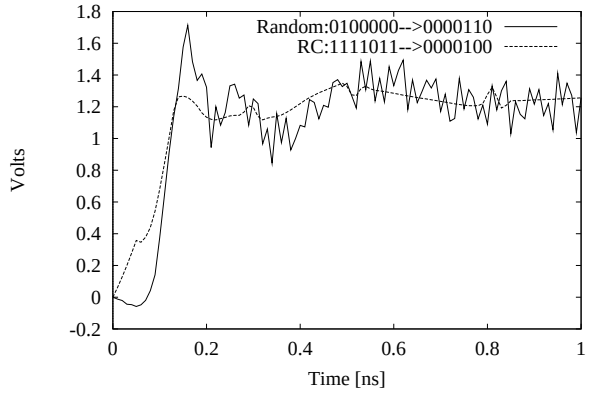

Figure 8: Oscillation phenomenon.

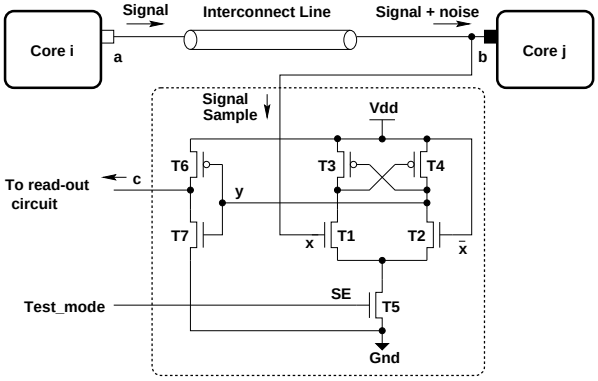

Figure 9: The ND-cell using cross-coupled PMOS amplifier.

more importantly creates overshoots that in long run cause permanent degradation of MOS transistors' performance and reliability.

Sense amplifiers are widely used in memory architectures (both DRAM's and SRAM's) [27][28]. The modified cross-coupled PMOS differential sense amplifier is our choice to detect integrity loss (noise) relative to the V-regions. The cell architecture that detects signals leaving the top V-region (above V_{Hthr} or below V_{Hmin}) is pictured in Figure 9. In this figure for simplicity we showed only one bit of an interconnect (point-to-point or bus) between *Core i* and *Core j*. The noise detector (ND) cell sits physically near the receiving core and samples the actual signal plus noise received by *Core j*. NMOS transistor T_5 is the current source (when $SE = 1$) and PMOS transistors T_3 and T_4 are loads. The positive feedbacks (drain-gate connection between T_3 and T_4) allow amplification in this structure. *SE* is connected to *test_mode* to create a permanent current source in the test mode and input $\overline{x}$ is connected to V_{dd} to define the threshold level for sensing V_b, i.e. the voltage received in *x*. The inverter, formed by T_6 and T_7, stabilizes the voltage levels in the output of ND cell. Various architectures for sense amplifiers and in-depth details can be found in [27][28].

By adjusting the size of the PMOS transistors (i.e. W and L), the current through transistors T_1 and T_2 are set to different values. Combining this with the feedbacks between PMOS transistors creates threshold voltages to turn the transistors on or off. Figure 10 shows signals on the input and output (points *b* and *c*) of the cell to validate the behavior of our noise detector cell.

The waveforms in Figure 10 reflect that the ND cell shows a *hysteresis* (Schmitt-trigger) property which implicitly indicates a (temporary) storage behavior. Each time that such noise occurs (i.e. $V_b > V_+ = V_{Hthr}$), the ND cell generates a 0 signal that remains unchanged until V_b drops below $V_- = V_{Hmin}$. To confirm this we ran a DC analysis on the ND cell to get the hysteresis curve shown in Figure 11. In

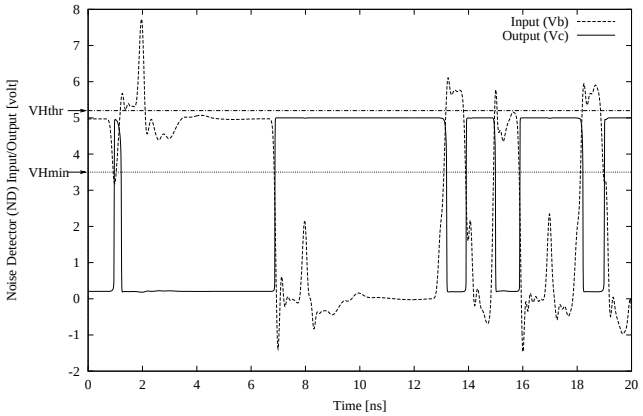

Figure 10: SPICE simulation of the ND cell for top V-region.

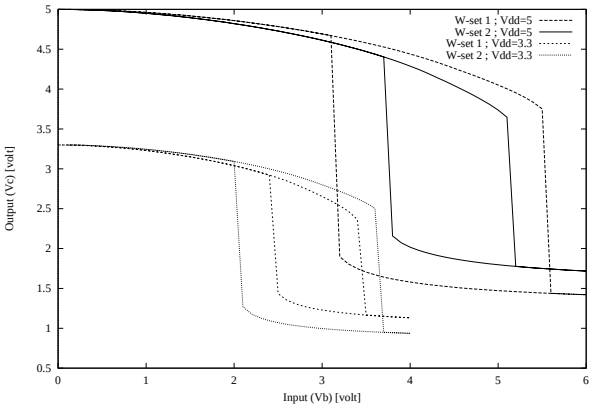

Figure 11: The hysteresis property of our noise detector cell.

this figure, for example, the solid-line curve shows that the switching threshold voltages are $V_+ = V_{Hthr} = 5.2$ and $V_- = V_{Hmin} = 3.5$ when $V_{dd} = 5.0$. The hysteresis property is quite desirable since it means the ND cell not only captures crossing V_{Hthr} (e.g. the overshoots) but also it filters out the signal bounces before settling down.

The unacceptable level of noise (integrity) can be a matter of test and reliability debate. For example, some researchers estimated that $0.1V_{dd}$ or more overshoot values create hot-carriers and thus may lead to a permanent damage [17]. A nice feature of our ND cell is that for any V_{dd} the overshoot threshold (i.e. V_+ of hysteresis) can be tuned by changing the layout size of the PMOS transistors (mainly W's of T_3 and T_4). This is also shown in Figure 11 in which two set of transistor widths ($W - set1$ and $W - set2$ for T_3 and T_4) and two V_{dd} values (3.3 and 5.0 volts) have been used. Analytical analysis (see [27]) or a simulation-based approach is used for such tuning. An identical cell can be used to detect V_{Lthr} and V_{Lmax}. Due to the space limitation, we have not shown the cell and its corresponding behavior.

6. TEST METHODOLOGY

Detecting noise (crossing the threshold voltage) was a crucial step that is performed by the ND cells. The ND cells are not expensive – seven transistors per cell as Figure 9 shows. Overall two cells are needed per interconnect to detect four threshold levels that are the borders of the immune regions (see Figure 2). The test architecture to read out the information stored in the ND cells is a DFT decision which depends on the overall SoC test methodology, testing objective and cost consideration. Some alternatives are shown in Figure 12. Note that due to the importance of overshoots we showed only one ND cell per wire to detect crossing V_{Hthr} and V_{Hmin}. The architecture can be replicated to consider the other two threshold voltages.

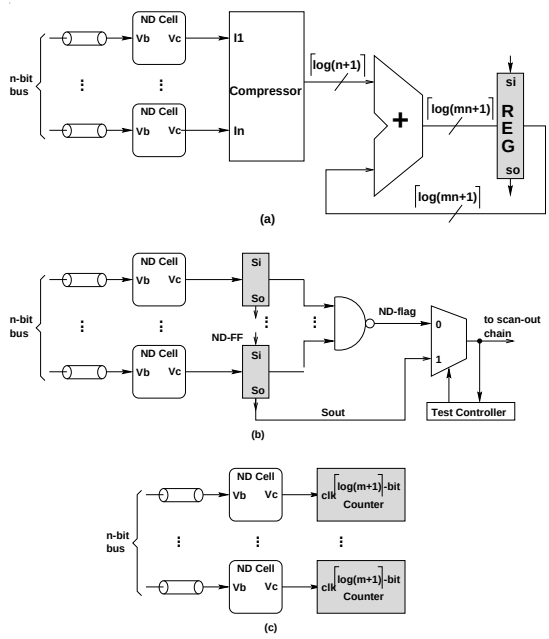

Figure 12: Test architecture alternatives.

•Using Compressors

In Figure 12(a), a compressor unit is used to compact test information (i.e. noise occurrence corresponding to the low signal integrity counts). Similar 4:2 compressor units have been extensively used in multiplier designs [29]. The noise are often required to be measured over a period of m transfer cycles (i.e. m patterns).Thus, a $\lceil log_2(mn+1)\rceil$-bit adder can be used to store numbers between 0 and mn. This is a very pessimistic worst case scenario in which we assume all lines are subject to low integrity (noise) in all m cycles. In reality, a much smaller adder and scannable register can be used to keep the statistics.

•Using Flip-Flops

Figure 12(b) demonstrates a flip-flop based test architecture, which is able to record the occurrence of noise and transfer it to the output. In the test-mode, first the noise flag signal (ND-flag) is transferred, through MUX, to the test controller. If noise (low integrity signal) occurs (ND-flag=1), the content of flip-flops (ND-FF's) are scanned out through S_{out} for further reliability and diagnosis analysis. The very pessimistic worst case scenario in terms of test time is a case in which all lines are subject to noise in all m cycles. This situation requires overall $m \cdot n$ cycles for readout. In practice, a much shorter time (e.g. $k \cdot n$, where $k << m$) is sufficient since the presence of defects causing unacceptable level of noise (signal integrity) is quite limited.

•Using Counters

If the cost is justified, we can get more accurate statistics about noise occurrence on each line of the bus by assigning each line to a dedicated counter as shown in Figure 12(b). This architecture will be costly but it keeps much more information about individual lines that may help in testing, diagnosis and reliability analysis. Ultimately, the content of the counter(s) can be scanned out through dedicated scan chain or through the main scan chain.

7. EXPERIMENTAL RESULTS

The number of cores in the SoC and the number of input ports of cores do not influence the low integrity detection process since the ND cells independently function near core input ports. They do, however, influence the cost of test overhead (e.g. ND cells, counters) and test time (e.g. scan-out time).

The experimental results here are reported using SPICE [23]. We analyzed five main buses (data, address, control and two internal) of the famous 8051 microprocessor [30]. In our implementation the 7 cores communicate through these buses and are potentially subject to noise in high frequency. For experimentation purpose, we used the interconnect architecture of 8051 assuming that it runs in 1 GHz. Typical global interconnect lengths in large SoC systems are chosen as the wire lengths in our experiments. Then, we have applied random patterns to the interconnects assuming that they run under 1 GHz frequency. The statistics are summarized in Table 1. As shown in Table 1, the average occurrence of unacceptable noise (low integrity signals) in a presumed 1 GHz 8051 system will be 32.44% and it will cause sever damages on chip over time.

Table 1: Integrity test results for 8051 bus structure.

Buses	Bitwidth	Length [mm]	Noise [%]
Data	8	20	43.38
Address	16	5	23.28
Control	10	10	28.50
Internal 1	10	10	34.40
Internal 2	8	10	32.62
Average	10.40	11.00	32.44

Table 2: Test overhead for 8051 16-bit address bus.

Architectures	*Cost [NANDs]*	*Time [cycle]*
Compressor+Adder	335	11
ND-FF+MUX	127	1600
Multiple Counters	784	112

Table 3 compares the cost and time of three alternatives for the test architectures corresponding to *Compressor+Adder* (Figure 12(a)), *ND-FF+MUX* (Figure 12(b)) and *Multiple Counters* (Figure 12(c)). We assumed that the total number of m patterns are applied to test each bus. Among these three, the *Multiple Counters* architecture is the most expensive one. In terms of test time for readout, the capture time is the same for all architectures since all use the same number and type of ND-cells. However, *ND-FF+MUX* architecture is the slowest one. To quantify the formulas given in Table 3, we show the statistics for the 16-bit address bus in 8051 reported by SYNOPSYS design compiler toolset [31] when 100 random patterns are applied. All costs are expressed in terms of 2-input NAND gates. The readout overhead results are shown in Table 2.

Table 4 compares the quantity and quality of random test patterns versus the RC patterns for a 7-wire parallel interconnect line. The overall number of patterns used in this experiment are 42 (6 patterns per wire as shown in Figure 4) and 100 for RC and random cases, respectively. The second and third columns show the number of patterns that show significant integrity loss (i.e. overshoot or delay at least 15% larger than their nominal values) from different perspectives. Although in general, the number of the RC patterns is smaller than the random patterns, the latter significantly improves the quality of interconnect testing by stimulating larger integrity loss (the worst case scenarios). For example, when we average the results of applying all patterns (first row), the random patterns cause larger integrity loss (in terms of peak noise and settle time) than the RC patterns. As for maximal delay on the interconnects, 43 (out of 100) and 14 (out of 42) patterns were counted for random and RC cases, respectively, causing significant delay. The average delay caused by these patterns are $122ps$ versus $102ps$. Similar trend exists for patterns that stimulate maximal peak/duration of noise. The RC test patterns do not stimulate any oscillation effect, while 5% of random patterns cause oscillation on the interconnect lines.

Table 3: Cost and time overhead for different test architectures

Test Architecture	*Component Size [bit]*					*Test Time [cycle]*	
	Compressor	Adder	Flip-Flops	Counters	Glue Logic	Capture	Scan-out
Compressor+Adder	n	$\lceil log_2(mn+1) \rceil$	$\lceil log_2(mn+1) \rceil$	–	–	m	$\lceil log_2(mn+1) \rceil$
ND-FF+MUX	–	–	n	–	NAND,MUX	m	$m \cdot n$
Multiple Counters	–	–	–	$n \times \lceil log_2(m+1) \rceil$	–	m	$n \cdot \lceil log_2(m+1) \rceil$

Table 4: Random test patterns versus RC test patterns.

Integrity Factor	*Quantity*		*Quality*		
	RC	*Random*	*Metric*	*RC*	*Random*
Mutual Effects	42	100	*Settle[ps]*	61	117
			Peak[V]	$0.15V_{dd}$	$0.28V_{dd}$
Maximal Delay	14	43	*Delay[ps]*	102	122
Maximal Noise	14	51	*Settle[ps]*	211	328
			Peak[V]	$0.26V_{dd}$	$0.34V_{dd}$
Oscillation	0	5	–	–	–

8. CONCLUSION

Designing industrial SoCs with testability in mind is an economic necessity. The rising level of complexity and frequency of chips makes it increasingly difficult to achieve an adequate interconnect (wiring system) test using the ad-hoc techniques currently practiced in industry. Identifying patterns to stimulate maximal integrity loss on the interconnect is also a big challenge. We propose a systematic methodology to model and test signal integrity in deep-submicron high-speed interconnects. Using inexpensive built-in TPGRs and noise detection cells offers an efficient test mechanism for signal integrity.

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REFERENCES

[1] Semiconductor Industry Association, *The International Technology Roadmap for Semiconductors*, Sematech, Inc., 1999.

[2] E. Marinissen, R. Arendsen, G. Bos, H. Dingemanse, M. Lousberg and C. Wouters, "A Structured and Scalable Mechanism for Test Access to Embedded Reusable Cores," in Proc. *Intern. Test Conf. (ITC'98)*, pp. 284-293, 1998.

[3] Lee Whetsel, "An IEEE 1149.1 Based Test Access Architecture for ICs With Embedded Cores," in Proc. *Intern. Test Conf. (ITC'97)*, pp. 69-78, Oct. 1997.

[4] C. Papachristou, F. Martin and M. Nourani, "Microprocessor Based Testing for Core-Based System-on-Chip," in Proc. *Design Automation Conf. (DAC'99)*, pp. 586-591, June 1999.

[5] M. Cuviello, S. Dey, X. Bai and Y. Zhao, "Fault Modeling and Simulation for Crosstalk in System-on-Chip Interconnects," in Proc. *Intern. Conf. on Computer Aided Design (ICCAD'99)*, pp. 297-303, Nov. 1999.

[6] W. Chen, S. Gupta and M. Breuer,, "Test Generation in VLSI Circuits for Crosstalk Noise," in Proc. *Intern. Test Conf. (ITC'98)*, pp. 641-650, 1998.

[7] P. Fang, J. Tao, J. Chen and C. Hu, "Design in Hot Carrier Reliability For High Performance Logic Applications," in Proc. *IEEE Custom Integrated Circuits Conf.*, pp. 25.1.1-25.1.7, Oct. 1998.

[8] Yusuf Leblebici, "Design Considerations for CMOS Digital Circuits with Improved Hot-Carrier Reliability," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 7, pp. 1014-1024, July 1996.

[9] S. Kimothi and U. Nandwani, "Uncertainty Considerations in Compliance-Testing for Electromagnetic Interference," in Proc. *Annual Reliability and Maintainability Symposium*, pp. 265-268, 1999.

[10] S. Zhao and K. Roy, "Estimation of Switching Noise on Power Supply Lines in Deep Sub-Micron CMOS Circuits," in Proc. *Intern. Conf. on VLSI Design*, pp. 168-173, Jan. 2000.

[11] H. Chen and L. Wang, "Design for Signal Integrity: The New Paradigm for Deep-Submicron VLSI Design," in Proc. *Intern. Symposium on VLSI Technology*, pp. 329-333, June 1997.

[12] D. Cho, Y. Eo, M. Seung, N. Kim, J. Wee, O. Kown and H. Park, "Interconnect Capacitance, Crosstalk and Signal Delay for 0.35 μm CMOS Technology," in Proc. *Intern. Meeting on Electron Devices*, pp. 619-622, 1996.

[13] L. Green, "Simulation, Modeling and Understanding the Importance of Signal Integrity," *IEEE Circuit and Devices Magazine*, pp. 7-10, Nov. 1999.

[14] R. Downing, P. Gebler and G. Katopis, "Decoupling Capacitor Effects on Switching Noise," *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, vol. 16, no. 5, pp. 484-489, Aug. 1993.

[15] R. Saleh, D. Overhauser and S. Taylor, "Full-Chip Verification of UDSM Designs," in Proc. *Intern. Conf. on Computer Aided Design (ICCAD'98)*, pp. 453-460, Nov. 1998.

[16] A. Kahng, S. Muddu and E. Sarto, "Interconnect Optimization Strategies for High-Performance VLSI Designs," in Proc. *Intern. Conf. on VLSI Design*, pp. 464-469, Aug. 1999.

[17] C. Cheng, J. Lillis, S. Lin and N. Chang, *Interconnect Analysis and Synthesis*, John Wiley & Sons, 2000.

[18] H. Veendrick, *Deep-Submicron CMOS ICs: from Basics to Asics*, Kluwer, 1998.

[19] B. Sheehan, "Projective Convolution: RLC Model-Order Reduction Using the Impulse Response," in Proc. *Design Automation Conf. (DAC'99)*, pp. 669-673, 1999.

[20] K. Gala, V. Zolotov, R. Panda, B. Young and D. Blaauw, "On-Chip Inductance Modeling and Analysis," in Proc. *Design Automation Conf. (DAC'00)*, pp. 63-68, 2000.

[21] J. Cong and L. He, "Theory and Algorithm of Local-Refinement-Based Optimization with Application to Device and Interconnect Sizing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 18 no. 4, pp. 406-420, April 1999

[22] L. He, N. Chang, S. Lin and O. Nakagawa, "An Efficient Inductance Modeling for On-chip Interconnects," in Proc. *IEEE Custom Integrated Circuits Conf.*, pp. 457-460, 1999

[23] TI-SPICE3 User's and reference manual, *1994 Texas Instrument Incorporation*, 1994.

[24] X. Bai, S. Dey and J. Rajski, "Self-Test Methodology for At-Speed Test of Crosstalk in Chip Interconnects," in Proc. *Design Automation Conf. (DAC'00)*, pp. 619-624, 2000.

[25] P.Restle, A.Tuehli and S. Walker, "Dealing with Inductance in High-Speed Chip Design," in Proc. *Design Automation Conf. (DAC'99)*, pp. 904-909, 1999.

[26] A. Deutsch, et. al., "The Importance of Inductance and Inductive Coupling for On-Chip Wiring," *IEEE 6th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 53-56, 1997.

[27] J. Rabaey, *Digital Integrated Circuits*, Prentice Hall, 1996.

[28] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, 2000.

[29] M. Elrabaa, I. Abu-Khater and M. Elmasry, *Advanced Low-Power Digital Circuit Techniques*, Kluwer Academic, 1997.

[30] Intel Corporation, "MCS-51 8-bit Microcontroller,", *Databook of Intel MCS-51 Microcontroller*, 1994.

[31] Synopsys Design Analyzer, "User Manuals for SYNOPSYS Toolset Version 2000.05-1," Synopsys, Inc., 2000.