

# Panel:

## Is Nanometer Design Under Control?

**Chair:** Andrew B. Kahng, Professor of CSE and ECE, UC San Diego, La Jolla, CA

**Organizers:** Bing Sheu, Nassda Corp., Santa Clara, CA,  
and Andrew B. Kahng, UC San Diego, La Jolla, CA

### Abstract

As fabrication technology moves to 100 nm and below, profound nanometer effects become critical in developing silicon chips with hundreds of millions of transistors. Both EDA suppliers and system houses have been re-tooling, and new methodologies have been emerging. Will these efforts meet the challenges of nanometer silicon such as performance closure, power, reliability, manufacturability, and cost? Which aspects of nanometer design are, or are not, under control? This session will consist of a debate between two teams of distinguished representatives from EDA suppliers and system design houses. Which side has the right answers and roadmap? You and a panel of judges will decide!

### Nancy Nettleton

#### Sun Microsystems, Palo Alto, CA

The top issues in nanometer design that I believe will place semiconductor designs at the greatest risk are physical chip planning/integration and signal integrity. Both issues cross a broad range of design disciplines, design tools, and design project scope. Neither issue is being effectively addressed today without significant homebrew EDA development. Both issues will ultimately require systemic changes to the way we design chips; not just the way we hook tools together, but the way we plan projects and organize teams.

I expect both issues will most likely be addressed by design methodologists, for two reasons:

1. Design methodologists have the most momentum on these issues today.
2. Design methodologists have a better vantage point of the entire design flow from which to make the kind of systemic changes that will be required.

### John Cohn

#### IBM Microelectronics, Burlington, VT

As we enter the nanometer design space, we find ourselves in an ever-tightening box between design closure issues, schedule pressure and increasing technology complexity. While many problems such as timing closure, power management and signal integrity are getting lots of attention, three problems that may not be getting the attention they deserve are: design predictability, cost, and methodology integration.

Our ability to profitably build big, fast chips is based entirely on our ability to accurately predict their

performance, reliability, and design effort in the face of an ever-growing list of technology challenges. In the nanometer design era these challenges includes such tough to modelling issues as device leakage, short channel effects, increased soft error sensitivity, substrate noise and increased parametric variation. In the interest of productivity, commercial tools are addressing these predictability problems by over-design and abstraction, in effect moving us away from the technology. The result is a widening performance gap between ASIC/SoC designs and more custom approaches.

Chip cost is another parameter that has seen surprisingly little focus from CAD vendors. Just because our methodologies enable us to make complex systems on a single die doesn't mean that it's always economically wise to do so. In fact, many of the things we have done in the interest of productivity actually lead to lower performance, larger dies, and thus higher costs. Current tool approaches tend to obscure the intrinsic trade-off between cost, design effort and other design metrics, again moving us away from the technology. The result is an overall poor ability for the industry to optimize profitability.

A final risk I see in the nanometer design space relates to the direction taken by many of the major CAD providers. In response to the deep sub-micron bogeyman, most CAD providers are attempting to soften the traditional boundaries between logical and physical design. This has given rise to a very powerful set of 'blended' tools offering combined synthesis, physical design and analysis. While the benefit is easier and faster design closure, the result is an overall loss in methodology flexibility due to the difficulty of mixing and matching methodology components from several sources.

Combining the concerns about technology predictability and cost with the complexity of large mixed-content SoC designs absolutely argues against any 'one size fits all' solution. A closed design system, no matter how elegant, will never contain the best of all current approaches. The solutions to these tough problems will not come from a single CAD company, silicon house or university, but rather from a synthesis of the best evolving knowledge from all of the sources. This then begs the question: "Who will best solve the nanometer design problem?" The answer is "Those who best understand the rules: the people that build the silicon.!"

**Shekhar Borkar**  
**Intel Corporation, Hillsboro, CA**

There are several issues when it comes to nanometer scale technologies. Transistors in this regime could have severe short channel effects, reducing their effectiveness in high speed circuits and logic. Parameter variations could affect circuit functionality and yield. And the high speed circuits that we depend on today to provide performance boost (e.g., domino) will cease to function. Technologists and circuit designers are aware of these problems and are working hard to solve them; therefore, these issues pose moderate risk from the technology standpoint. However, the EDA community is completely oblivious to this, and is solving today's mundane problems, extrapolating into the nanometer regime. As a result, we might have process and circuit technology for nanometer scale, but no design technology to take advantage of the nanometer technology. This is the major risk moving forward.

**Louis Scheffer**  
**Cadence Design Systems, Inc., San Jose, CA**

The biggest risk to nanometer design is any effect that:

1. affects many nets and/or cells, so it can't be fixed by hand;
2. cannot be addressed without major changes to tools or libraries, both of which have very long lead times; or
3. can't be fixed by methodology without unacceptable overhead.

Three effects come to mind that meet these criteria - leakage currents, soft errors, and manufacturability requirements such as antenna rules. Leakage currents are most easily addressed by architectures that allow power switching and/or new libraries and tools that can take advantage of them. Both of these are long lead time items, so we need to thinking about leakage now or we risk a crisis later. Soft errors are a similar problem, with a complete library re-design required if the effect is worse than anticipated. Manufacturing rules can have a similar effect - indeed this almost happened with antenna rules during the 0.18 micron to 0.13 micron transition. These rules became much more restrictive and the EDA vendors were barely able to respond in time. A similar unanticipated manufacturing requirement could precipitate a crisis, with no chips produced until a solution is invented.

Who is responsible for anticipating these problems? Library creators and vendors will need to step up their efforts; in-house library creation and/or tight cooperation will be needed to anticipate any process quirks in time for early production. Next, the fabs need to be upfront about any new manufacturability requirements, and the

CAD vendors must take them seriously. Finally designers need to understand those effects (such as leakage power) that can't be fixed by libraries and/or tools alone. These must be addressed by architectural tradeoffs. With due diligence on the part of all concerned, we can keep nanometer effects (barely) under control.

**Ed Cheng**  
**Synopsys, Inc., Mountain View, CA**

**Sang Wang**  
**Nassda Corp., Santa Clara, CA**

The top three issues putting the semiconductor industry at risk:

1. Prevalent nanometer effects inducing more serious circuit timing, power and signal integrity problems will cause frequent silicon failures. These nanometer effects stemming from interconnect parasitics and nonlinear device behavior are very difficult to control without accurate accounting for their details.
2. Very large circuit size or high circuit complexity (such as mixed analog, digital and memory components) exceeding most simulation and verification tools' capacity or substantially slowing down tools' performance. This significantly reduces designers' effectiveness in understanding and solving difficult circuit problems at the whole-chip level.
3. A lack of efficient and reliable layout extractors hinders effective post-layout circuit verification and circuit optimization. Without full-chip detailed simulations with reasonably accurate extracted layout parameters and parasitics, users have little control in assuring working silicon and good yield.

Which constituency will solve these issues, and how?

1. Highly accurate and efficient simulation and analysis tools are needed to thoroughly understand and resolve nanometer effects so that silicon success can be achieved for nanometer circuits.
2. Tools must support very large circuit capacity with very high computational performance to control the ever-increasing design size and turnaround time requirements. Mature mixed-level and hierarchical tools are two possible solutions.
3. Mature extractors are key. Hierarchical extractors will be most effective but are very difficult to develop. Hierarchical parasitic backannotation is an alternative and the solution is around the corner for users to have a control of post-layout full-chip verification.