An Interconnect Energy Model Considering Coupling Effects

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ABSTRACT

This paper first presents an analytical interconnect energy model with consideration of event coupling, which is not considered by the conventional $\frac{1}{2}CV^2$ model. Our energy calculation algorithm has the same time complexity as the $\frac{1}{2}CV^2$ model, and is several orders of magnitude faster than HSPICE with less than 5% error. In comparison, the error of the $\frac{1}{2}CV^2$ model can be as high as 100%.

1. INTRODUCTION

The $\frac{1}{2}CV^2$ model has been commonly used as an interconnect energy model. In this model, each event is supposed to consume energy $\frac{1}{2}CV^2$, where C is the load capacitance of the interconnect, and V is the change of the voltage. However, this model is not accurate because it does not consider crosstalk noise and incomplete voltage swing. These effects are due to spatio-temporal event coupling, and significant for long interconnects in deep sub-micron design.

This paper proposes an interconnect energy model with consideration of event coupling, and provides algorithms to calculate the interconnect energy. The paper is organized as follows: Section 2 defines an interconnect model. Section 3 presents an analytical expression for the interconnect energy. Section 4 proposes an algorithm to calculate the model parameters. Section 5 presents an event-driven energy calculation algorithm. Section 6 discusses the relation between energy and signal correlation. Section 7 describes the overall procedure of our approach. Section 8 provides experimental results, and Section 9 concludes the paper.

2. PRELIMINARIES

A *net* is a set of pins, one of which is a *driver*, and the others are *sinks*. The driver is modeled by a voltage source and an output resistance as shown in Appendix A.

The *interconnect* of a net is a directed tree, in which each node represents either the voltage source, a sink, or a joint of wire segments, and each edge represents either the output resistance or a wire segment. The voltage source node is called *root*, and is connected to the output resistance edge. The direction of an edge is consistent with the path from the root to a sink.

38^{th} *DAC,* June 18-22, 2001, Las Vegas, Nevada, USA.

Let M and N denote the number of the interconnects and that of the edges. The node and edge labels are defined in such a way that (1) the output resistance of interconnect m is labeled edge m, and (2) the root of interconnect m is labeled node $N+m$, called root m, where $m = 1, \cdots, M$.

The *incidence matrix* A is an $(M+N) \times N$ matrix, where $A_{vi} = 1$ ($A_{vi} = -1$) if node v is the head (tail)[1] of edge i, and $A_{vi} = 0$ otherwise. The *reduced incidence matrix* A_r is an $N \times N$ matrix defined by $(A_r)_{vi} = A_{vi}$ $(v, i = 1, \cdots, N)$. A_r is invertible, and satisfies the property that $(A_r^{-1})_{iv} = 1$ if $v \in T_i$ and $(A_r^{-1})_{iv} = 0$ otherwise, where T_i is the set of the nodes in the subtree rooted at the head of edge i.

Let $V_m(t)$ denote the voltage of root m at time t. According to our driver model (*c.f.* Appendix A), the time derivative of $V_m(t)$ can be expressed as

$$\dot{V}_m(t) = \sum_{a=1}^{w_m} \delta(t - t_m^a) \Delta V_m^a, \tag{1}$$

where $\delta(t)$ is the δ-function, $0 < t_m^1 < t_m^2 < \cdots < t_m^{w_m}$ are the event times, w_m is the number of the events at root m, and ΔV_m^a is the change of $V_m(t)$ at t_m^a. In digital circuits, $V_m(t)$ is either 0 or V_{DD} (the supply voltage). Hence, $\Delta V_m^a = \pm V_{DD}$. Event a at root m is denoted by (m, a).

The *resistance matrix* R is an $N \times N$ diagonal matrix, where R_{ii} (> 0) is the resistance of edge i.

The *inductance matrix* L is an $N \times N$ symmetric matrix, where $L_{ij} (i \neq j)$ is the mutual inductance between edges i and j, and L_{ii} is the self inductance of edge i.

The *capacitance matrix* C is an $N \times N$ symmetric matrix defined by $C_{vw}(v \neq w) = -\Gamma_{vw}$ and $C_{vv} = \sum_{w=1}^{N} \Gamma_{vw}$, where $\Gamma_{vw}(v \neq w)$ is the coupling capacitance between nodes v and w, and Γ_{vv} is the ground capacitance of node v. The charge of node v is expressed as $\sum_{w=1}^{N} C_{vw} u_w$, where u_w is the voltage of node w. For later use, we introduce $\tilde{C} \equiv A_r^{-1} C A_r^{-1^T}$, which can be also expressed as

$$\tilde{C}_{ij} = \sum_{v \in T_i} \sum_{w \in T_j} C_{vw} = \sum_{w \in T_j} C_{h(i),w} + \sum_{k \in Child(i)} \tilde{C}_{kj}, \tag{2}$$

where $h(i)$ is the head of edge i, and $Child(i)$ is the set of the edges outgoing from $h(i)$. Note that $\tilde{C}_{mm}$ $(m = 1, \cdots, M)$ is the load capacitance of interconnect m, and $-\tilde{C}_{mn}$ $(m \neq n; m, n = 1, \cdots, M)$ is the total coupling capacitance between interconnects m and n.

3. INTERCONNECT ENERGY

The nodal equations for the set of interconnects are $A_r \vec{i} = C\dot{\vec{u}}$, and $R\vec{i} + L\dot{\vec{i}} = \sum_{m=1}^{M} \vec{e}_m V_m - A_r^T \vec{u}$, where i_j (the j-th element of vec-

[1]The *head (tail)* of an edge is the node to (from) which the edge is incoming (outgoing).

tor $\vec{i}$) is the current of edge j, and $(e_m)_j = \delta_{m,j}$[2]. The solution of the nodal equations is expressed as $\vec{x}(t) = \vec{b}(t) - \int_0^t d\xi\, e^{Q(t-\xi)}\dot{\vec{b}}(\xi)$ with initial condition $\vec{x}(0) = \vec{b}(0)$, where $\vec{x} \equiv \begin{bmatrix} A_r^T\vec{u} \\ \vec{i} \end{bmatrix}$, $\vec{b} \equiv \sum_{m=1}^{M} \begin{bmatrix} \vec{e}_m \\ 0 \end{bmatrix} V_m$, and $Q \equiv \begin{bmatrix} 0 & \tilde{C}^{-1} \\ -L^{-1} & -L^{-1}R \end{bmatrix}$. Inserting this solution into the interconnect energy dissipation $E \equiv \int_0^\infty dt\, \vec{i}^T R \vec{i}$, we obtain

$$E = \int_0^\infty dt \int_0^t d\xi \int_0^t d\xi'\, \dot{\vec{b}}^T(\xi)\, e^{Q^T(t-\xi)} \begin{bmatrix} 0 & 0 \\ 0 & R \end{bmatrix} e^{Q(t-\xi')}\dot{\vec{b}}(\xi').$$

Since the integrand is a total derivative:

$$-\frac{1}{2}\frac{d}{dt}\left(\dot{\vec{b}}^T(\xi)\, e^{Q^T(t-\xi)} \begin{bmatrix} \tilde{C} & 0 \\ 0 & L \end{bmatrix} e^{Q(t-\xi')}\dot{\vec{b}}(\xi')\right),$$

we change the order of the integration to carry out the integration over t, and obtain $E = \sum_{m=1}^{M}\sum_{n=1}^{M} E_{mn}$, where

$$E_{mn} \equiv \frac{1}{2}\int_0^\infty d\xi \int_0^\infty d\xi'\, H_{mn}(|\xi - \xi'|)\dot{V}_m(\xi)\dot{V}_n(\xi'), \qquad (3)$$

and $H_{mn}(t) \equiv \begin{bmatrix} \vec{e}_m^T\tilde{C} & 0 \end{bmatrix} e^{Qt} \begin{bmatrix} \vec{e}_n \\ 0 \end{bmatrix}$. To derive the above equations, we used the stability condition: $\lim_{t\to\infty} e^{Qt} = 0$.

Inserting Eq. 1 into Eq. 3, we also obtain

$$E = \sum_{m=1}^{M}\sum_{n=1}^{M}\sum_{a=1}^{w_m}\sum_{b=1}^{w_n} \frac{1}{2} H_{mn}^{ab}\Delta V_m^a \Delta V_n^b, \qquad (4)$$

where $H_{mn}^{ab} \equiv H_{mn}(|t_m^a - t_n^b|)$ represents spatio-temporal coupling effects. By assuming $H_{mn}^{ab} = 0$ for $(m,a) \neq (n,b)$, the conventional $\frac{1}{2}CV^2$ model is obtained as follows:

$$E_C = \sum_{m=1}^{M}\sum_{a=1}^{w_m} \frac{1}{2}\tilde{C}_{mm}\Delta V_m^a \Delta V_m^a. \qquad (5)$$

To show the importance of the coupling effects, we apply Eq. 4 to simple circuits. In the following, we call the simultaneous switching of any event pair in the same (opposite) direction as an *aligned (anti-aligned) pair*.

In the first example, we assume $M = 2$, $w_1 = w_2 = 1$, and $t_1^1 = t_2^1$. In this case, $E = \frac{1}{2}(\tilde{C}_{11} + \tilde{C}_{22} + 2\tilde{C}_{12})V_{DD}^2$ when the events are aligned, and $E = \frac{1}{2}(\tilde{C}_{11} + \tilde{C}_{22} - 2\tilde{C}_{12})V_{DD}^2$ when the events are anti-aligned. On the other hand, Eq. 5 does not show any difference for these two cases.

In the second example, we assume $M = 1$ and $w_1 = 2$. In this case, $E = (\tilde{C}_{11} - H_{11}^{12})V_{DD}^2$. The term $-H_{11}^{12}$ represents the incomplete voltage swing, which means the voltage does not always reach 0 or V_{DD} everywhere in the interconnect within time interval $[t_1^1, t_1^2]$ due to wire resistance.

4. ONE-POLE APPROXIMATION

Under the one-pole model [2], $H_{mn}(t) \approx \tilde{C}_{mn}e^{-t/d_{mn}}$, where $d_{mn} \equiv D_{mn}/\tilde{C}_{mn}$, and $D_{mn} \equiv \sum_{i=1}^{N} R_{ii}\tilde{C}_{im}\tilde{C}_{in}$. d_{mn} is called *charge time* in this paper since it represents the time to charge/discharge interconnects. Note that inductance does not appear in the one-pole model.

To show an algorithm to calculate $\tilde{C}_{mn}$ and D_{mn}, we consider a circuit after layout, in which each interconnect is implemented by horizontal and vertical wires. We assume only adjacent parallel wires have coupling capacitance.

[2] $\delta_{i,j} = 1$ for $i = j$ and $\delta_{i,j} = 0$ for $i \neq j$.

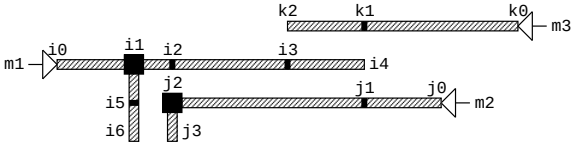

Figure 1: Interconnects after Layout

Each wire is divided into a minimum number of *uniform segments*, such that unit-length resistance, ground and coupling capacitance are constant within each uniform segment. In Fig. 1, (j_0, j_2) is divided into uniform segments (j_0, j_1) and (j_1, j_2) due to the difference of coupling capacitance.

In the distributed circuit composed of uniform segments, edge i is replaced by pair (α, x), where α is a uniform segment, and x is the distance from the head of α. Correspondingly, $\tilde{C}_{im}$ $(i = 1, \cdots N; m = 1, \cdots, M)$ is replaced by $\tilde{C}_{\alpha m}(x)$, which can be expressed as

$$\tilde{C}_{\alpha m}(x) = g_{\alpha m}x + \tilde{C}_{\alpha m}(0), \quad g_{\alpha m} \equiv \sum_{i=0}^{2} c_\alpha^i \delta_{m,m_\alpha^i}, \qquad (6)$$

where $\tilde{C}_{\alpha m}(0) = \sum_{\beta\in Child(\alpha)} \tilde{C}_{\beta m}(l_\beta)$, in which $Child(\alpha)$ is the set of the uniform segments outgoing from the head of α, and l_β is the length of β. Also, $c_\alpha^0 \equiv \sum_{i=0}^{2}\gamma_\alpha^i$, $c_\alpha^i \equiv -\gamma_\alpha^i$ $(i = 1, 2)$, where γ_α^0 is the unit-length ground capacitance of uniform segment α, and γ_α^1 (γ_α^2) is the unit-length coupling capacitance between α and the upper/left (lower/right) wire. In Eq. 6, m_α^0 is the label of the interconnect which contains α, and m_α^1 (m_α^2) is the label of the interconnect which contains the upper/left (lower/right) adjacent wire. Eq. 6 is the extension of Eq. 2 for the distributed circuit.

Using Eq. 6, $D_{mn} = \sum_\alpha \int_0^{l_\alpha} dx\, r_\alpha \tilde{C}_{\alpha m}(x)\tilde{C}_{\alpha n}(x)$ becomes

$$D_{mn} = \sum_\alpha r_\alpha l_\alpha \left(\tilde{C}_{\alpha m}\left(\frac{l_\alpha}{2}\right)\tilde{C}_{\alpha n}\left(\frac{l_\alpha}{2}\right) + \frac{g_{\alpha m}g_{\alpha n}l_\alpha^2}{12}\right),$$

where r_α is the unit-length resistance of uniform segment α.

The algorithm to calculate $\tilde{C}_{mn}$ and D_{mn} is as follows:

Algorithm getM(α)
1. $\vec{y} := 0, \vec{z} := 0$;
2. **for(**$\beta \in Child(\alpha)$**)** $\vec{y} := \vec{y}$ + getM(β) ;
3. **for(**$i = 0, 1, 2$**)** $z_{m_\alpha^i} := z_{m_\alpha^i} + c_\alpha^i l_\alpha/2$;
4. $\vec{y} := \vec{y} + \vec{z}$;
5. **for(**each pair m, n such that $y_m \neq 0$, $y_n \neq 0$**)**
6. **begin**
7. $D_{mn} := D_{mn} + r_\alpha l_\alpha (y_m y_n + \frac{1}{3}z_m z_n)$;
8. **end**
9. **return** $\vec{y} + \vec{z}$;

At Line 2 and 3, $y_m = \tilde{C}_{\alpha m}(0)$, and $z_m = g_{\alpha m}l_\alpha/2$. y_m becomes $\tilde{C}_{\alpha m}(l_\alpha/2)$ (Line 4). The contribution from α is added to D_{mn} (Line 5-8). Finally, $\tilde{C}_{\alpha m}(l_\alpha)$ is returned (Line 9). `getM` must be called for all the roots.

The time complexity of the algorithm is $O(MK^3)$, where K is the maximum number of the uniform segments contained in one interconnect. The reason is as follows: $\vec{y}$ has at most $2K+1$ non-zero elements since the number of the descendant uniform segments is at most K, each of them couples with at most 2 interconnects, and '1' represents the self coupling. Hence, the time complexity of the **for** loop of Line 5-8 is $O(K^2)$. Since this **for** loop is done at most MK times, the total time complexity is $O(MK^3)$. Since K is a local parameter, the time complexity with respect to the circuit size is $O(M)$.

5. ENERGY CALCULATION

Assume that (m,a) is the last event, which means $t_m^a \geq t_n^b$ for any event (n,b). According to Eq. 4 under the one-pole model, addition of event (m,a) increases E by $\Delta E_m^a \approx \frac{1}{2}\tilde{C}_{mm}(\Delta V_m^a)^2 + \sum_{n=1}^{M} \tilde{C}_{mn} e^{-\frac{t_m^a - t_n^{w_n}}{d_{mn}}} X_{mn}^{w_n} \Delta V_m^a$, where X_{mn}^b is recursively defined by $X_{mn}^b = \Delta V_n^b + e^{-(t_n^b - t_n^{b-1})/d_{mn}} X_{mn}^{b-1}$ with $X_{mn}^0 = 0$. By accumulating ΔE_m^a sequentially for each event (m,a), the total energy E will be obtained.

The above arguments are summarized in the following event-driven energy calculation algorithm:

```
Algorithm calcE()
 1.  E := 0 ;
 2.  for(each m) w_m := 0 ;
 3.  for(each m, n such that C̃_mn ≠ 0) X_mn := 0 ;
 4.  Set up event queue EQ ;
 5.  while(EQ is not empty)
 6.    begin
 7.      Pop the first event (m,a) from EQ ;
 8.      E := E + (1/2) C̃_mm (ΔV_m^a)^2 ;
 9.      for(each n such that C̃_mn ≠ 0)
10.        begin
11.          E := E + C̃_mn e^{(t_n^{w_n} - t_m^a)/d_mn} X_mn ΔV_m^a ;
12.          X_nm := ΔV_m^a + e^{(t_m^{a-1} - t_m^a)/d_nm} X_nm ;
13.        end
14.      w_m := w_m + 1 ;
15.    end
```

The time complexity of the algorithm is $O(WK)$, where $W = \sum_{m=1}^{M} w_m$ is the number of the events. $O(K)$ is due to **for** loop of Line 9-13 since the number of n such that $\tilde{C}_{mn} \neq 0$ is at most $2K+1$ as shown in Section 4.

6. ENERGY AND SIGNAL CORRELATION

When V_m and V_n are mutually independent, it likely happens that the number of the aligned pairs is almost equal to that of the anti-aligned pairs. In this case, $E_{mn} \approx 0$ since the contribution from the aligned pairs is cancelled by that from the anti-aligned pairs. This observation is supported by the following theorem:

THEOREM 1. *$E_{mn} \approx 0$ if V_m and V_n are independent.*

[Proof] According to Eq. 3, $E_{mn} = \lim_{T\to\infty}(I_{mn}^T + I_{nm}^T)/2$, where $I_{mn}^T \equiv \int_0^\infty d\tau H_{mn}(\tau) \int_0^T d\xi \dot{V}_m(\xi)\dot{V}_n(\xi+\tau)$. We will show $P_{mn} \equiv \lim_{T\to\infty} I_{mn}^T/T$ is 0, which means $E_{mn} \approx 0$. Note that $P_{mn} = \int_0^\infty d\tau H_{mn}(\tau)\langle \dot{V}_m(\xi)\dot{V}_n(\xi+\tau)\rangle$, where $\langle\cdots\rangle \equiv \lim_{T\to\infty}\frac{1}{T}\int_0^T d\xi \cdots$ denotes the average with respect to the time. The mutual independence of V_m and V_n implies $\langle \dot{V}_m\dot{V}_n\rangle = \langle \dot{V}_m\rangle\langle \dot{V}_n\rangle$. Since V_m is finite, $\langle \dot{V}_m\rangle = \lim_{T\to\infty}(V_m(T) - V_m(0))/T = 0$. [QED]

When all the signals are mutually independent,

$$E = \sum_{m=1}^{M}\sum_{a=1}^{w_m}\sum_{b=1}^{w_m} \frac{1}{2} H_{mm}^{ab} \Delta V_m^a \Delta V_m^b. \qquad (7)$$

7. SUMMARY OF OUR MODEL

The overall procedure of our model is as follows:

1. Extraction of interconnect parameters,
2. Calculation of parameters for one-pole model,
3. Event-driven interconnect energy calculation.

The interconnect parameters include the unit-length resistance, ground and coupling capacitance for each uniform segment after decomposing interconnects in a sequence of uniform segments. Procedure 3 can be efficiently performed with any commercially available event-driven simulator, such as `Verilog-XL/PLI`.

Circuits	Error (%)			Run Time (sec.)			
	EC	E0	E1	EC	E0	E1	HSPICE
c(10,10)	76	2.4	0.6	∼0	∼0	.01	70
c(10,20)	76	-0.5	1.0	∼0	.01	.01	190
c(10,30)	88	3.3	3.0	∼0	.01	.01	560
c(20,10)	73	1.6	1.0	∼0	.01	.02	300
c(20,20)	90	2.7	2.4	∼0	.01	.05	1600
c(20,30)	94	4.6	3.9	∼0	.02	.05	4800
c(30,10)	77	3.1	1.7	∼0	∼0	.04	910
c(30,20)	89	3.8	3.3	.01	.01	.08	6200
c(30,30)	93	4.0	3.8	∼0	.01	.10	27000
c(1000,10)	-	-	-	.02	.12	2.5	-
c(5000,10)	-	-	-	.06	.55	13	-
c(10000,10)	-	-	-	.18	1.2	27	-

Table 1: Comparison of Error and Run Time

8. EXPERIMENTAL RESULTS

We implemented our algorithm to compare it with `HSPICE` on a SUN ULTRA 60 work station running at 360MHz.

We used the 70*nm* CMOS technology derived in [1] in our test, where the clock frequency is $1GHz$ and $V_{DD} = 0.75V$. We assumed minimum wire width and spacing, in which ground capacitance is $0.054fF/\mu m$, coupling capacitance is $0.119fF/\mu m$, and resistance is $0.36\Omega/\mu m$ for a unit-length wire. The unit-length inductance is assumed to be $1pH/\mu m$.

In Table 1, c(M,K) represents a circuit with M interconnects, each of which has K edges. In this case, $N = M \times K$. The topology of the circuit is randomly generated such that each edge has $0 \sim 3$ children, and couples with 1 or 2 edges. Note that such a topology may not correspond to a real layout. The wire length is determined such that the maximum Elmore delay is less than half of the clock cycle. Each interconnect is driven by a CMOS driver with output resistance 32.7Ω, and gate capacitance $23.1fF$, which is also considered as the sink capacitance. The input waveform is randomly generated such that each "proper" event (expected event by the functionality of the circuit) is followed by 0 or 2 "glitch" events (unexpected events, noise) after $40 \sim 120$(psec). The length of an input waveform is 50 clock cycles. Input signals are mutually independent.

Columns 2-4 of Table 1, labeled `EC`, `E0`, and `E1`, show the energy estimation error by the $\frac{1}{2}CV^2$ model (Eq. 5) and our models using Eq. 7 and Eq. 4 compared with `HSPICE`, respectively. The missing entries "-" are due to too long `HSPICE` run time. The total energy, including CMOS driver energy, is measured by `HSPICE` using "`POWER`" command, while that for `EC`, `E0`, and `E1` is defined as the sum of the interconnect energy and the driver internal energy, which is the product of the number of the events and the driver internal energy per event (*c.f.* Appendix A). The results show that our models are within 5% of accuracy of `HSPICE`, while the error of the commonly used $\frac{1}{2}CV^2$ model can be as large as 94%.

In Table 1, there is no obvious difference between `E0` and `E1` since the signals are mutually independent. Fig. 2 shows the relation between error and signal correlation for c(10,10). The vertical axis represents the error compared with `HSPICE`, and the horizontal axis represents the average *correlation coefficient* between two roots. The correlation coefficient between roots m and n is defined by $r_{mn} \equiv |p_{mn} - p_m p_n| / \sqrt{p_m(1-p_m)p_n(1-p_n)}$, where p_m is the probability of V_m being V_{DD}, and p_{mn} is the probability of V_m and V_n being simultaneously V_{DD}. $r_{mn} = 0$ implies V_m and V_n are mutually independent, and $r_{mn} = 1$ implies either $V_m \equiv V_n$ or $V_m \equiv V_{DD} - V_n$. According to Fig. 2, the error of `E0` is large when the correlation is

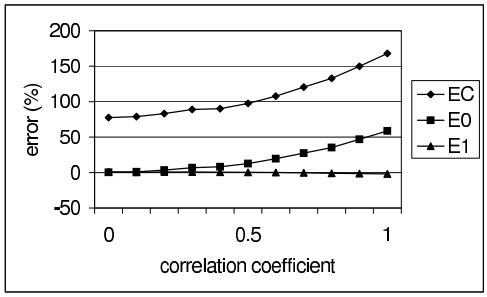

Figure 2: Error vs. Correlation Coefficient

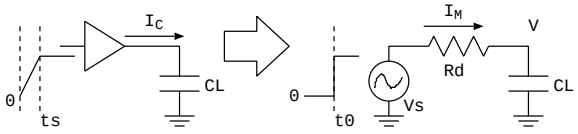

Figure 3: Driver Model for Energy Calculation

strong.

Columns 5-8 of Table 1 compare the run time, where "∼0" means "less than 0.01". The overhead to read in SPICE files is excluded for `EC`, `E0`, and `E1` since it is negligible compared with `HSPICE` run time. The results for large circuits, c(1000,10), c(5000,10), c(10000,10), show the run time of `EC`, `E0`, `E1` is linear with respect to the circuit size.

The above results show the following hybrid approach would be efficient: `EC` is used for short interconnects, `E0` is used for long interconnects, and E_{mn} ($m \neq n$) is added if the signals for roots m and n are strongly correlated. The strength of the correlation is represented by r_{mn}, which can be obtained using a probabilistic approach [3].

9. CONCLUSIONS AND FUTURE WORKS

This paper proposed an interconnect energy model with consideration of spatio-temporal coupling effects, such as crosstalk noise and incomplete voltage swing, which are significant for deep submicron design. Our interconnect energy calculation algorithm has the same time complexity as the conventional $\frac{1}{2}CV^2$ model with respect to the circuit size. We investigated the relation between interconnect energy and signal correlation to propose a simplified model (Eq. 7). Experimental results show that our approach is several orders of magnitude faster than `HSPICE` with less than 5% error. In comparison, the error of the $\frac{1}{2}CV^2$ model can be as high as 100%. The key feature of our approach is that we directly calculated the total interconnect energy, not as the sum of the individual one.

Our future work will concentrate on the probabilistic approach for interconnect energy estimation, and the power optimization at the global interconnect planning level.

Our interconnect energy model is explained in detail in [4].

APPENDIX

A. DRIVER MODEL

This appendix presents a CMOS driver model for energy calculation. For simplicity, we assume the driver is a 1-input and 1-output buffer with load capacitance C_L, and the input waveform switches linearly within the time interval $[0, t_s]$ as shown in the left hand side of Fig. 3. This driver is modeled by an output resistance R_d and a voltage source V_S switching instantly at time t_0 as shown in the right hand side of Fig. 3.

To determine the model parameters R_d and t_0, we compare the output current of the CMOS driver (I_C) with that of the model (I_M). It is easy to show that

$$\int_0^\infty dt\, e^{-st} I_M(t) = \frac{C_L \Delta V}{1 + sR_d C_L} e^{-st_0}, \tag{8}$$

where $\Delta V \equiv V(\infty) - V(0)$ is the change of the voltage. Expanding both sides of Eq. 8 around $s = 0$, and comparing the coefficients of s^n ($n = 1, 2$), we obtain

$$R_d^2 C_L^2 = a_2 - a_1^2, \qquad t_0 + R_d C_L = a_1, \tag{9}$$

where $a_n \equiv \frac{1}{C_L \Delta V} \int_0^\infty dt\, t^n I_M(t)$ ($n = 1, 2$) are moments of I_M. Replacing them with the moments of I_C, which are measured by `HSPICE`, R_d and t_0 are obtained through Eq. 9.

The driver internal energy per event is obtained by subtracting $\frac{1}{2}C_L \Delta V^2$ from the measured total energy per event.

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