

# Fast Power/Ground Network Optimization Based on Equivalent Circuit Modeling

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## ABSTRACT

*This paper presents an efficient algorithm for optimizing the area of power or ground networks in integrated circuits subject to the reliability constraints. Instead of solving the original power/ground networks extracted from circuit layouts as previous methods did, the new method first builds the equivalent models for many series resistors in the original networks, then the sequence of linear programming method [9] is used to solve the simplified networks. The solutions of the original networks then are back solved from the optimized, simplified networks. The new algorithm simply exploits the regularities in the power/ground networks. Experimental results show that the complexities of simplified networks are typically significantly smaller than that of the original circuits, which renders the new algorithm extremely fast. For instance, power/ground networks with more than one million branches can be sized in a few minutes on modern SUN workstations.*

## 1. INTRODUCTION

Power/Ground (p/g) networks deliver power supplies from the p/g pads on a chip to the circuit modules. Because of the endless push for low power and increasing transistor counts, p/g networks need to be carefully designed and optimized to fulfill more and more stringent requirements. An important design issue concerning all the circuit designers is how to use the minimum amount of chip area for wiring p/g networks while avoiding potential reliability failures due to electro-migration and excessive IR drops.

One way to improve the quality of the p/g networks is to size the wire segments assuming the topologies of p/g networks are fixed. Several methods have been developed to solve this wire-sizing problem [2, 3, 4, 5, 9]. But most of these methods formulate the wire-sizing problem into a constrained nonlinear programming problem. Existing approaches such as Augmented Lagrangian method [2], Conju-

gate Gradient method [4], Feasible Direction method [5] to this problem are known to be computationally intensive and can not be scaled to solve large p/g networks which contain millions of wire segments [6]. Research work [8] considering the capacitive and inductive effects in p/g network optimization was also proposed.

Recently, [9] presented an efficient algorithm to solve the wire-sizing problem. The method is an extension of the relaxed two-phase optimization method by Chowdhury [4]. The idea is to further relax the nonlinear objective function and then translate the constrained nonlinear programming problem into a sequence of linear programming problems. The method was demonstrated to be orders of magnitude faster than the previously best-known method using the conjugate gradient algorithm. For p/g networks with millions of wire segments commonly seen in typical ASIC designs, however, the sequence of linear programming method is still too slow to handle such networks in a reasonable time.

This paper presents a new approach to solving the large scale p/g optimization problem subject to reliability constraints. Our method is based on the sequence of linear programming method (SLP) [9]. Instead of solving the p/g networks directly extracted from chip layouts, the new method first constructs the equivalent models for many series resistor circuits in the networks. Then it replaces the series resistor circuits with their equivalent models. The resulting networks, which typically are much smaller than the original ones, are solved by the SLP method and the solutions of original networks are finally back solved from the optimized, simplified networks. The new method simply exploits the regularities in the p/g networks in which many wire segments share the same width. Experimental results have shown that the proposed algorithm scales very well to attack large p/g networks. For instance, a p/g network with 10k branches can be solved in couple of seconds and the one with more than one millions branches can be solved in a few minutes on modern SUN workstations.

This paper is organized as follows: Section 2 describes the formulation of the p/g network optimization problem, and reviews the sequence of linear programming method. The new method is presented and explained in detail in Section 3. Experimental results from some large p/g networks and comparison with the SLP method are summarized in Section 4. Section 5 concludes the paper.

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## 2. PROBLEM FORMULATION AND SEQUENCE OF LINEAR PROGRAMMING

We still follow the two-phase optimization formulation in [4, 9]. We first look at the wire-sizing problem formulation, then we review the sequence of linear programming method.

### 2.1 Problem Formulation

Let  $G = \{N, B\}$  be a p/g network with  $n$  nodes  $N = \{1, \dots, n\}$  and  $b$  branches  $B = \{1, \dots, b\}$ . Each branch  $i$  in  $B$  connects two nodes:  $i_1$  and  $i_2$  with current flowing from  $i_1$  to  $i_2$ . Let  $l_i$  and  $w_i$  be the length and width of branch  $i$ , respectively. Let  $\rho$  be the sheet resistivity. Then the resistance  $r_i$  of branch  $i$  is  $r_i = \frac{V_{i_1} - V_{i_2}}{I_i} = \rho \frac{l_i}{w_i}$ . We can express total p/g routing area in terms of voltages, currents and lengths of branches as follows:

$$f(\mathbf{V}, \mathbf{I}) = \sum_{i \in B} l_i w_i = \sum_{i \in B} \frac{\rho I_i l_i^2}{V_{i_1} - V_{i_2}}. \quad (1)$$

The constraints that need to be satisfied for a reliable, working p/g network are as follows.

1. **The voltage IR drop constraints.** To ensure the correct and reliable logic operation, the voltage drop from the p/g pads to the leaf nodes should be restricted. We then impose the following constraints to every leaf node.

$$\begin{aligned} V_i &\geq V_{min} \text{ for power networks.} \\ V_i &\leq V_{max} \text{ for ground networks.} \end{aligned} \quad (2)$$

where  $V_{min}$  and  $V_{max}$  are given constants based on the technology.

2. **The minimum width constraints.** The widths of the p/g segments are technologically limited to the minimum width allowed in the layer where the segment lies. Thus, we have

$$w_i = \rho \frac{l_i I_i}{V_{i_1} - V_{i_2}} \geq w_{i,min}. \quad (3)$$

where  $w_{i,min}$  are given constants.

3. **The electro-migration constraints.** Electro-migration on a p/g wire segment sets an upper bound on the current density of the segment [1]. For a routing layer with fixed thickness. This constraint for branch  $i$  is expressed as  $|I_i| \leq w_i \sigma$ , and can be re-written as the following nodal voltage constraint:

$$|V_{i_1} - V_{i_2}| \leq \rho l_i \sigma. \quad (4)$$

where,  $\sigma$  is a constant for a particular routing layer with a fixed thickness.

4. **Equal width constraints (coupling constraints)** In typical chip layout designs, most commercial p/g routers do not allow the widths of p/g wire segments to be arbitrary values with respect to other wire segments. Instead, certain p/g wire segments should have the same width. For example, the wire segments in a p/g ring around macro cells in ASIC designs. The constraint can be written as  $w_i = w_j$ . In terms of nodal voltages and branch currents, we have

$$\frac{V_{i_1} - V_{i_2}}{l_i I_i} = \frac{V_{j_1} - V_{j_2}}{l_j I_j}. \quad (5)$$

### 5. Kirchoff's current law (KCL).

$$\sum_{i \in B(j)} I_i = 0, \quad (6)$$

for each node  $j = \{1, \dots, n\}$  and  $B(j)$  is the set of indices of branches connected to node  $j$ .

P/G network optimization is to minimize (1) subject to constraints (2), (3), (4), (5) and (6). It will be referred to as Problem **P**. Problem **P** is a constrained nonlinear optimization problem.

### 2.2 Sequence of Linear Programming Algorithm

Sequence of linear programming is an extension of the work by Chowdhury [4], which relaxes the original problem **P** and divides **P** into two phases – **P-V** and **P-I**. The relaxed sub-problems, whose solution spaces are subsets of the original one, become simpler problems (**P-V** is a convex program and **P-I** is a linear programming problem) and thus are much easier to solve than the original one is.

#### • Phase one: **P-V**

Assume that all branch currents are fixed and node voltages are variables. Then the objective is

$$f(\mathbf{V}) = \sum_{i \in B} \frac{\alpha_i}{V_{i_1} - V_{i_2}}, \quad (7)$$

where  $\alpha_i = \rho I_i l_i^2$ . It further assumes that the current direction will not change after optimization, i.e.,

$$\frac{V_{i_1} - V_{i_2}}{I_i} \geq 0. \quad (8)$$

So the constraints for problem **P-V** are (2), (3), (4), (5) and (8).

The problem **P-V** defined so far is a convex programming problem. But it is still a nonlinear programming problem given the nonlinear objective function (7).

In [9], further relaxation was performed by linearizing the objective function  $f(\mathbf{V})$  around the initial solution  $\mathbf{V}_0$ :

$$g(\mathbf{V}) = \sum_{i \in B} \frac{2\alpha_i}{(V_{i_1}^0 - V_{i_2}^0)} - \sum_{i \in B} \frac{\alpha_i}{(V_{i_1}^0 - V_{i_2}^0)^2} (V_{i_1} - V_{i_2}). \quad (9)$$

With addition of the following constraint

$$\xi \text{sign}(I_i)(V_{i_1}^0 - V_{i_2}^0) \leq \text{sign}(I_i)(V_{i_1} - V_{i_2}), \quad (10)$$

where  $\xi \in (0, 1)$ , it was shown in [9] that the linear programming version of **P-V** will leads to the same optimal result of the relaxed, convex **P-V** problem, while in a much efficient way.

#### • Phase two: **P-I**

Assume that all nodal voltages are fixed and branch currents become variables. Then the objective function can be re-written as:

$$f(\mathbf{I}) = \sum_{i \in B} \beta_i I_i, \quad (11)$$

where  $\beta_i = \frac{\rho l_i^2}{V_{i_1} - V_{i_2}}$ , subject to following constraints: (3), (5) and (6).

The SLP algorithm starts with an initial feasible solution, then iteratively solves two linear programming problems **P-V**, then **P-I**.

### 3. NEW POWER/GROUND OPTIMIZATION ALGORITHM

The new method is based on the observation that not all the node voltages and branch currents are required to be explicitly constrained. By exploiting the regularities and their implications on the node voltages and branch currents, we can simplify a p/g network by using equivalent circuit modeling. SLP can be efficiently applied to the simplified network to obtain the optimal solution.

In the sequel, we first present how a p/g network can be simplified by using equivalent circuit modeling.

#### 3.1 Equivalent Circuit Modeling of Series Resistor Chain

Consider a series resistor chain commonly seen in the p/g network in Figure 1. There exists voltage  $V_s$ , between the two series ends,  $N_1$  and  $N_n$ , coming from the interaction of the series resistor chain with rest of the network. Suppose the positive current direction for resistive branch (wire segment)  $R_i$  is from  $N_i$  to  $N_{i+1}$ . Such a series resistor chain can be modeled by an equivalent circuit shown in Figure 2 [7], where the positive current direction of  $R_s$  is from  $N_1$  to  $N_n$ . The equivalent resistor  $R_s$  is just the sum of all the resistors in series,

$$R_s = \sum_{i=1}^{n-1} R_i. \quad (12)$$

By superposition, the equivalent current  $I_{e1}$  and  $I_{en}$  can be computed as follows:

$$I_{e1} = \sum_{i=1}^{n-2} \frac{\sum_{j=i+1}^{n-1} R_j}{R_s} I_i, \quad (13)$$

$$I_{en} = \sum_{i=1}^{n-2} \frac{\sum_{j=1}^i R_j}{R_s} I_i. \quad (14)$$

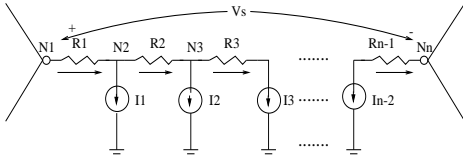


Figure 1: Series Resistor Chain.

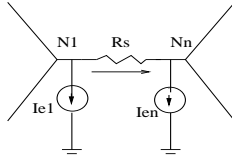


Figure 2: Series Resistor Equivalent Circuit.

Once the simplified circuit has been solved with the equivalent circuit and the voltages at the end nodes are known, the voltages at the intermediate nodes are calculated based on superposition as follows:

$$V_{i+1} = V_i - \frac{R_i}{R_s} V_s - R_i I_{ei}, \quad (15)$$

$$I_{ei+1} = I_{ei} - I_i. \quad (16)$$

#### 3.2 Equivalent Circuit Modeling for P/G Optimization

The equivalent circuit modeling method was originally developed for fast p/g network simulation [7]. To apply the method to our p/g optimization problem, we have to consider following differences:

- Firstly, in a series resistor chain circuit, not all the node voltages need to be constrained by IR drop constraints. We only need to look at the nodes whose voltages are the local minimum or the local maximum. This also means that not all the intermediate nodes in a series resistor chain can be suppressed. Figure 3 shows two scenarios where node voltages are the local minimum or the local maximum and the corresponding nodes can not be suppressed. With this requirement, a series resistor chain will be broken into several sub-chain circuits, and currents of all the resistive branches in each of the sub-chains will have the same sign (currents flow in the same direction) and we only need to look at the voltage at one end in a sub-chain circuit.

Since we assume that the current directions will not change after optimization in the SLP method [9], voltages of those nodes will still be the minimum or the maximum in the sub-chain circuit after optimization.

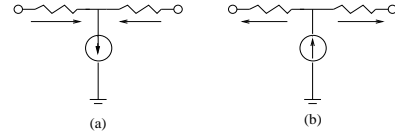


Figure 3: Nodes can not be suppressed (a) nodes in power networks (b) nodes in ground networks.

- Secondly, we observe that widths of all the resistive branches in a series resistor chain circuit are typically identical as we know that a series resistor chain is typically extracted from a straight p/g trunk or one side of a power/ground ring that commonly are routed with one layer.

With this assumption, all the equivalent currents computed in (13) and (14) will remain unchanged during optimization and we also are able to solve back the width (or resistant value) of each individual wire segment after optimization. Let's  $R'_i$ , the unknown, and  $R'_s$  be the resistant values of  $R_i$  and  $R_s$  after optimization, respectively, then

$$R'_i = \frac{R'_s}{R_s} R_i. \quad (17)$$

- Finally, electro-migration constraint (4) also needs to be modified for accommodating for the changes in equivalent circuit modeling.

Consider the series resistor sub-chain in Figure 1. The current flowing through resistor  $R_i$ ,  $I_{Ri}$ , has two components:

$$I_{Ri} = I_s + I_{ei}, \quad (18)$$

where  $I_s (= \frac{V_s}{R_s})$  is due to the voltage drop of  $V_s$  across  $R_i$  and it is also the current flowing through  $R_s$  in the simplified network.  $I_{ei}$  is the current flowing through

$R_i$  when  $V_s$  is replaced by a short circuit. That is just  $I_{e_i}$  computed in (16). Notice that all the currents  $I_{R_i}$ ,  $i \in [1, n-1]$  will have the same sign in a series resistor sub-chain. Without losing generality, we assume currents are always flowing from  $N_1$  to  $N_n$ , i.e.  $I_{R_i} > 0$ ,  $i \in [1, n-1]$ . Then we have

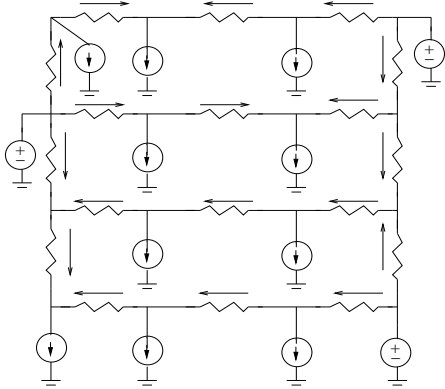
$$I_{R_i} \geq I_{R_j}, \text{ for } i < j. \quad (19)$$

This is because  $I_{e_i} > I_{e_j}$  for  $i < j$  according to (16). Since all the resistors in a series resistor chain share the same width and  $R_1$  experiences the largest current, we only need to consider the current of  $R_1$  for the EM problem. Similarly, for a ground network, with the same assumption of the positive current direction for each resistive branch, we only need to consider current of  $R_n$  for the EM problem. By using the  $I_{R_1}$  or  $I_{R_n}$  as the current for the equivalent resistor  $R_s$ , EM constraint (4) for  $R_s$  shown in Figure 2 will become

$$\begin{aligned} |V_{s1} - V_{s2}| &\leq \frac{\rho l_s \sigma}{1 + \frac{I_{e_i}}{I_s}} \text{ for power networks,} \\ |V_{s1} - V_{s2}| &\leq \frac{\rho l_s \sigma}{1 + \frac{I_{e_n}}{I_s}} \text{ for ground networks.} \end{aligned} \quad (20)$$

Note that constraint (20) is a linear constraint for both **P-V** and **P-I** phases and we have to explicitly consider the EM constraints in the **P-I** phase now.

Figure 4 and Figure 5 show, respectively, a  $3 \times 3$  power network and its corresponding simplified network.

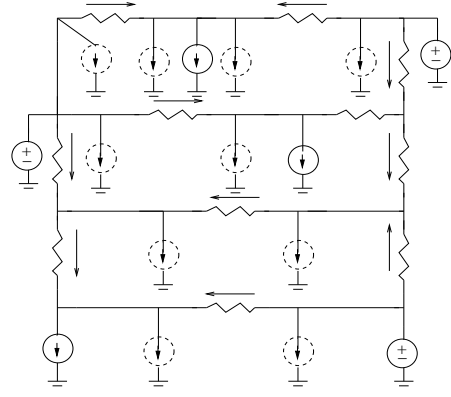


**Figure 4: A  $3 \times 3$  power network. Current direction in each resistive branch is marked.**

Now we summarize the entire new optimization procedure as follows:

#### New P/G Optimization Algorithm

1. Analyze the network  $G$  to obtain an initial feasible solution and construct the equivalent network  $G_e$  of  $G$  and designate the initial solution in  $G_e$  as  $\mathbf{V}_e^k, \mathbf{I}_e^k$  for  $k = 0$ .
2. Construct the minimum width constraints (3), equal width constraints (5), additional constraints (10) and EM constraints (20) using  $\mathbf{I}_e^k$ .



**Figure 5: The equivalent circuit of the  $3 \times 3$  power network. All the equivalent resistors are marked with dotted surrounding boxes and the equivalent currents are shown at both ends of the equivalent resistors.**

3. Minimize  $g(\mathbf{V}_e^k)$  subject to constraints (2), (3), (5) and (10) and (20) by a sequence of linear programming, record the result as  $\mathbf{V}_{e,l}^k$ , where  $l$  begins from 1. If  $f(V_{e,l}^k) > f(V_{e,l-1}^k)$ , do the line search along the direction  $\mathbf{d} = (V_{e,l-1}^k - V_{e,l}^k)$  until  $f(V_{e,l}^k) \leq f(V_{e,l-1}^k)$ . Record the result from the last iteration  $l$  and line search in step 3 as  $\mathbf{V}_e^{k+1}$ .
4. Construct the minimum width constraints (3), equal width constraints (5) and EM constraints (20) using  $\mathbf{V}_e^{k+1}$  for each branch.
5. Minimize the objective function (11) subject to the constraints (3), (5) (6) and (20) by linear programming and record the result as  $\mathbf{I}_e^{k+1}$ .
6. If  $|f(\mathbf{V}_e^{k+1}, \mathbf{I}_e^{k+1}) - f(\mathbf{V}_e^k, \mathbf{I}_e^k)| < \epsilon$ ,  $\epsilon$  is the termination criterion, then stop, otherwise  $k = k + 1$  and goto step 2.
7. Back solve the  $\mathbf{V}$  and  $\mathbf{I}$  of  $G$  from  $\mathbf{V}_e^{k+1}$  and  $\mathbf{I}_e^{k+1}$  and obtain the wire width for each wire segment in  $G$ .

## 4. EXPERIMENTAL RESULTS

A program for p/g network optimization has been developed based on the proposed method. We tested the program on a set of p/g networks on SUN workstation with 296 MHz SUN Sparc processor. The set of p/g network test cases have the complexities ranging from ten to one million wire segments. The proposed method is also compared against the pure SLP algorithm [9] in terms of CPU time and quality of results. For all the test cases, we assume that all the wire segments in a series resistor chain share the same width and the same width constraints are enforced in both new algorithm and the pure SLP method. The results are summarized in Table 1.

In Table 1, column 1 shows the names of the p/g networks tested. Columns 2 to 5 list, respectively, the number of nodes in the circuit (*# nodes*), the number of branches (*# bchs*) which accounts for both resistive branches and current branches, CPU time in seconds (*time(sec)*) and the reduced chip area of the original area in percentage (*area reduced*).

**Table 1: Comparison of the new algorithm against the SLP method.**

ckt	pure SLP method				new algorithm				Speedup
	# nodes	# bchs	time(sec)	area reduced(%)	# nodes	# bchs	time(sec)	area reduced(%)	
pg4x4	17	23	0.28	50.0	7	13	0.01+0.22	50.0	1.22
pg20x20	400	439	4.02	50.0	31	70	0.01+0.30	48.4	12.97
pg300x10	3001	3599	110.88	50.0	429	1027	0.46+6.42	50.0	16.12
pg100x100	10001	10199	1079.30	49.99	154	352	3.04+1.39	49.99	243.63
pg1000x1000	$1 \times 10^6$	$2 \times 10^6$	>10 hrs	-	3529	9089	38.04+92.31	9.85	>276.18

(%) for the pure SLP method. Columns 6 to 9 show the same criteria for the new algorithm. The last column gives the speedup of the new algorithm over the pure SLP method. The CPU time for the new algorithm consists of two parts. The first part is due to the construction of equivalent circuits and the second part is the time for the p/g optimization by SLP and back solving of original networks.

It is shown in Table 1 that equivalent circuit modeling can significantly reduce the complexities of the p/g networks. For instance, for circuit *pg100x100*, 98.4% nodes and 96.5% branches have been suppressed. For *pg1000x1000*, 99.6% nodes and 99.5% branches are gone. With the simplified p/g networks in which node and branch counts are no more than a few of thousands, SLP can be performed very efficiently. The two orders of magnitude speedup over the pure SLP algorithm on larger test cases is a clear evidence of the effectiveness of the equivalent circuit modeling technique. With this, network *pg1000x1000*, which has more than one million branches, can be optimized in a few minutes. To the best of our knowledge, this is the largest p/g network ever optimized by a p/g optimization algorithm in a reasonable time. On the contrast, the pure SLP algorithm failed to deliver any results on this network, after running for 10 hours<sup>1</sup>.

Also we notice that the percentages of the numbers of nodes and branches which can be suppressed depend on the topologies of the p/g networks. Networks with the same complexities but different topologies may lead to different optimization times by the new algorithm in general.

The areas reduced for most of the tested p/g networks are about 50%. The actual improvements, however, strongly depend on the initial solutions. It can be seen that both algorithms almost gives the same results for most of test cases. The discrepancy in network *pg20x20* is due to some numerical issues in the linear programming process.

Our work is mainly based on the resistant-only models for p/g networks. But the capacitive and inductive effects in p/g networks with latest technologies have reached the point where they are no longer second-tier effects. Further optimization techniques have to explicitly consider the dynamic behaviors of p/g networks.

## 5. CONCLUSIONS

A fast power/ground optimization method based on equivalent circuit modeling was proposed for sizing the widths of the wire segments in a power/ground network under reliability constraints.

Experimental results have shown that new algorithm can be more than two orders of magnitude faster than the sequence of linear programming method, the best-known power/ground optimization algorithm, on large power/ground networks. The effectiveness of the new algorithm was fully

demonstrated with the optimization of a power/ground network with more than million branches in a few minutes on modern SUN workstations.

## 6. ACKNOWLEDGMENTS

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<sup>1</sup>The run actually took about 70 hours before terminated.