Inductance 101: Modeling and Extraction†

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Abstract—Modeling magnetic interactions for on–chip interconnect has become an issue of great interest for integrated circuit design in recent years. This tutorial paper describes the basic concepts of magnetic interaction, loop and partial inductance, along with some of the high frequency effects such as skin and proximity effect.

Index Terms—Inductance, Magnetic Interaction, Interconnect Modeling.

I. Introduction

UNTIL recently the impact of magnetic fields created by the current flow in integrated circuits was generally neglected in terms of its impact on the performance of these systems. The circuit operation frequencies were low enough such that induced voltages were generally negligible compared with the effects due to parasitic resistance and capacitance of the interconnect. Increasing clock speeds and the desire to push technologies to their ultimate performance limits have made magnetic modeling of ICs one of the most urgent issues for high performance integrated circuit design. The global nature of magnetic coupling makes this an extremely challenging modeling and analysis problem.

This paper is an introduction to the problem of modeling and analysis of inductance for integrated circuits. We begin in Section II with the basic physical processes which cause inductive coupling between conducting loops and address some key assumptions. In Section III the more specific issues regarding inductive modeling of on–chip circuits are addressed and the significance of modeling the magnetic interaction for these structures is demonstrated on a small bus example. The partial inductance approach, which is the key to modeling inductance in complex circuits, is discussed in more detail in Section IV. The paper concludes with coverage of some high frequency effects. Coverage of some design and extraction efficiency issues can be found in [1].

II. Magnetic Induction

The process of inductive interaction between conductors carrying currents can be decomposed into three effects which take place concurrently:

1. Currents flowing through conductors create magnetic fields (Ampere's Law);
2. Magnetic fields varying with time create induced electric fields (Faraday's Law);
3. Induced electric fields exert forces upon the electrons in the conductors and cause electric voltage (Electric Potential) drops.

A. Ampere's Law

Currents flowing through conductor loops and time–varying electric fields create magnetic fields. This relationship between current density *j*, the electric field *E* and the resulting magnetic field *B* is *Ampere's Law*:

$$\vec{\nabla} \times \vec{B} = \mu\vec{j} + \mu\varepsilon\frac{d\vec{E}}{dt} \tag{1}$$

The first term on the right hand side of (1) represents the contribution of the current density to the magnetic field on the left hand side. μ is the magnetic permeability of the insulator surrounding the wires and ε its electric permittivity. The curl operator on the left hand side causes the resulting magnetic field to be 'wrapped around' the existing current flow patterns (see Figs. 1 and 3). The integral form, which can be derived from (1) via Stokes' Law, is

$$\oint_{\text{edge(S)}} \vec{B} \cdot d\vec{l} = \mu \int_{S} \left(\vec{j} + \varepsilon\frac{d\vec{E}}{dt}\right) \cdot d\vec{S} \tag{2}$$

where *S* is a surface which intersects the wire (see Fig. 1). The current through *S* creates a magnetic field around the wire. For a general, three–dimensional current flow this field is difficult to predict intuitively, but for one–dimensional wires the field direction can be predicted with the *right–hand rule*: if the thumb of the right hand points in current direction, the other fingers point in direction of the magnetic field.

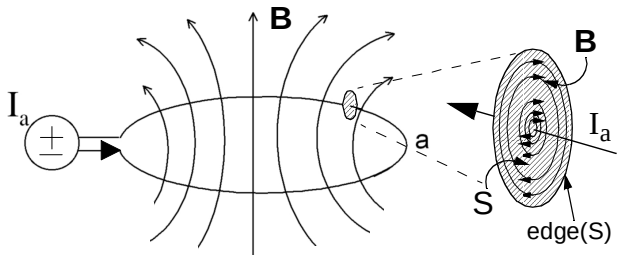

Fig. 1: Magnetic Field created by a time–variant current flowing through a conductor loop.

The second term in the right–hand side integral of (2) is referred to as the *displacement current density*, since it has the dimension of a current density and represents the *ac* current flowing between two conductors due to their capacitive couplings. Time–varying electric fields can create magnetic fields. Usually, however, this term is neglected in Ampere's Law for integrated circuits since the magnetic field created directly by the currents flowing within the conductors is larger than the magnetic field created by the displacement currents — even with dominant lateral capacitance coupling — by at least one order of magnitude.

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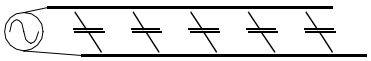
Discarding the displacement current term in (1) decouples the inductive and capacitive effects within the circuit; therefore this step is referred to as a *quasistatic approximation*, since the capacitive electric fields are assumed to be roughly ('quasi') static and variations of the potential differences between conductors are sufficiently slow such that the displacement term is negligible compared with the current term in (1). The quasi–static (differential and integral) form of Ampere's Law is:

$$\vec{\nabla} \times \vec{B} \approx \mu \vec{j} \quad \text{or} \quad \oint_{\text{edge(S)}} \vec{B} \cdot d\vec{l} \approx \mu \int_{S} \vec{j} \cdot d\vec{S} \tag{3}$$

To illustrate the validity of this assumption for integrated circuits, we compare both right hand side terms in (1) for typical values for a 0.13 micron technology [2]: If the transistor switching current is 0.3 mA, $\mu_r = 1$ and the interconnect cross–section is 0.13 x 0.26 µm, then the first term is about **12 kVs/m^3**. If the minimal distance between two conductors is 0.13 µm, $\varepsilon_r = 3$, the maximal voltage difference 2 V and the minimal signal ramp time is 20 ps, then the second term is around **0.026 kVs/m^3**. Although this is only an example, it illustrates very well that the displacement current contribution to the magnetic field is usually negligible.

The displacement current itself, however, is not negligible. We showed that the *contribution of the displacement currents to the magnetic field* is negligible. While most *ac* current flows on-chip through capacitors *at some point*, its capacitive paths are much shorter than its resistive paths. An example: Two parallel *wires* form a capacitor:



The ac source injects current which returns on average at half length of the wire pair through capacitors. If the wires are 1 mm long and have 1 µm spacing, then the ac current spends about 1000 µm in wires and only 1 µm displacing. Capacitors are necessary to get the right current return loops (on average *half* the length here, *not* through far end), but do not contribute much to the loop inductance (displacement path only a tiny fraction of the resistive path in above example). Therefore coupling capacitance must be included in the interconnect circuit model *but not* the inductance *of the coupling capacitors*, validating the quasistatic assumption.

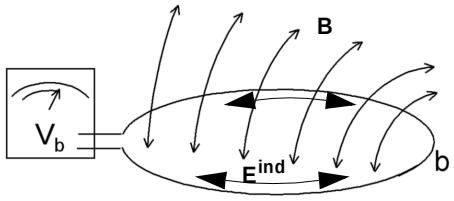


Fig. 2: Electric voltage created by time–variant magnetic field passing through a conductor loop. The integral of the magnetic field over the loop area is referred to as the *magnetic flux*.

B. Faraday's Law

Ampere's Law gives us the first part of the inductive process: the creation of the magnetic field. Only if these magnetic fields vary with time do these fields create *induced electric fields*. Therefore, time–variant currents are required for induction, the relationship of which is *Faraday's Law*:

$$\oint_{b} \vec{E}_{ind} \cdot d\vec{l} = -\frac{d\Phi}{dt} \quad \text{with } \Phi = \int_{\text{Area of b}} \vec{B} \cdot d\vec{S} \tag{4}$$

where Φ is the *magnetic flux* and E_{ind} the induced electric field. The induced electric field 'wraps around' the magnetic field lines (see Fig. 2). The portion of the induced electric field which is parallel to the wire of loop **b** in Fig. 2 exerts force on the charges in **b** and creates voltage in the loop.

Note that the *induced* electric field is a different field than the *capacitive* electric field. The capacitive E–field is caused directly by the charges located on the surfaces of the conductors (due to the individual potentials of these conductors) and governed by *Gauss' Law*

$$\vec{\nabla} \cdot \vec{E}_{cap} = \frac{\rho}{\varepsilon} \tag{5}$$

where ρ is the charge density. The induced E–field is caused by the time–variant magnetic field in Eq. (4).

The orientation of the loop with respect to the induced electric field determines the amount of induced voltage. If the loop is orthogonal to the induced E–field the total effect of the magnetic field on it will be zero (As we will see later in a more detailed derivation, this causes *partial* inductive couplings between orthogonal wires to become zero).

C. Electric Potential

The induced electric field can be integrated along the victim loop and results in an *induced voltage* which adds to the already existing voltage due to the resistance of the loop:

$$V_b^{ind} = -\oint_{b} \vec{E}_{ind} \cdot d\vec{l} \tag{6}$$

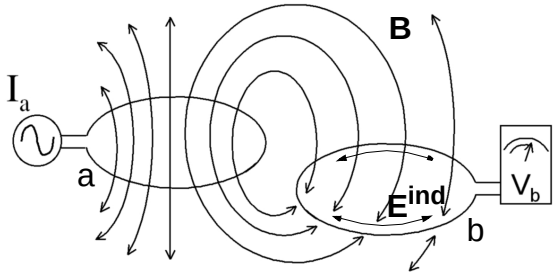


Fig. 3: Magnetic field created by the time–variant current in loop **a** induces voltage in a second loop, **b**, since some of the magnetic field passes through **b**.

D. Loop Inductance

Fig. 3 summarizes the combination of these three effects which combine to generate a voltage drop in the victim loop **b** due to a time–variant current in loop **a**. All three relationships involved, Eqns. (3), (4) and (6), are linear. Therefore, the resulting combined relationship between time–derivatives of currents in the loops and the resulting induced voltage drops is linear as well:

$$V_b^{ind} = L_{ba} \frac{dI_a}{dt} \quad \text{with } I_a = \int_{\text{Crossection of a}} \vec{j} \cdot d\vec{S} \tag{7}$$

L_{ba} is the *mutual inductance* of loop **a** upon loop **b** and I_a is the current flowing through loop **a**. For the special case where loops **a** and **b** are the same, the coefficient L_{aa} is the *self inductance* of loop **a**. The calculation of these inductance coefficients usually requires integrations over the path

of the loops and over their cross–sections as well, if these are not negligible. For some simple structures, these integrals may be solved analytically (see for instance [3], [6] or [7]). We will look at the special case of loops consisting of straight segments later in this paper.

There are instances of ICs which include inductors as components of filter and oscillator circuits. But it is the inductors *not deliberately* designed into integrated circuits, namely the *parasitic inductance*, which is the primary subject of this paper.

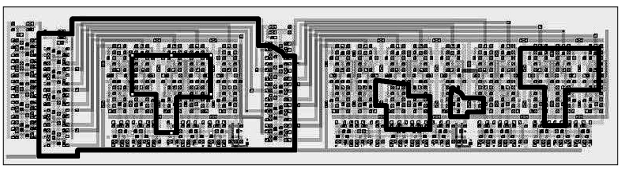


Fig. 4: A sample circuit with a few possible conductor loops formed by the interconnect wires.

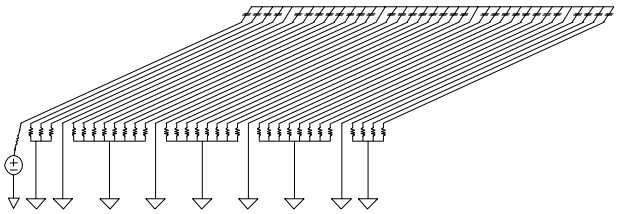


Fig. 5: 32 bit bus with four in–plane return lines. Leftmost line is active. Line numbering from left to right.

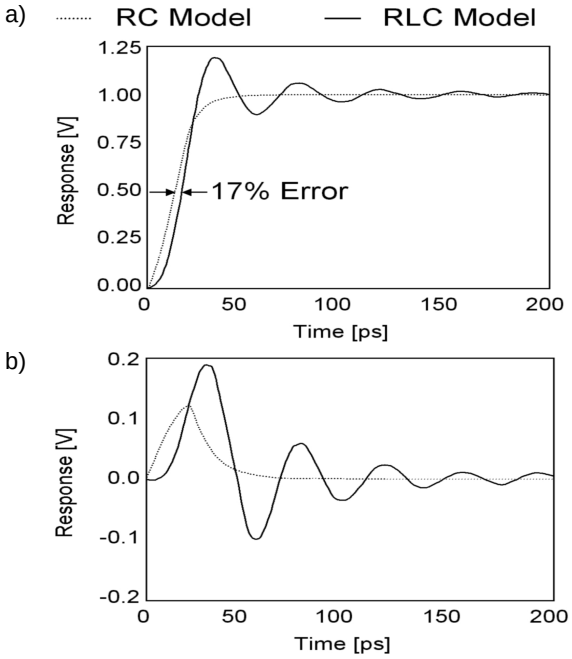


Fig. 6: Results for 32 bit bus structure in Fig. 5. *a)* shows the voltage response at the far end node of the active line, while *b)* shows the response at the far end node of the immediately neighboring 'quiet' line. The input was a 20 ps ramp from 0–1 volt.

III. On–Chip Interconnect

A. Parasitic Induction

Fig. 4 shows a small IC circuit to demonstrate the possible current loops that could occur due to the interconnection of wires. The total number of loops is on the order of $O(N^2)$, where N is the number of interconnect segments. Identifying all possible loops for an IC given the segments is difficult, and generating the inductive coefficients for all loop pairs once the loops are known is completely impractical.

Many of these loop couplings can possibly be ignored since the loops involved carry little current; but in general we need to solve for the currents to make an accurate determination on this. We take a quick look at this 'chicken–and–egg' problem of requiring an inductance model before determining the magnitude of the current, as it impacts the signals for a bus on an integrated circuits.

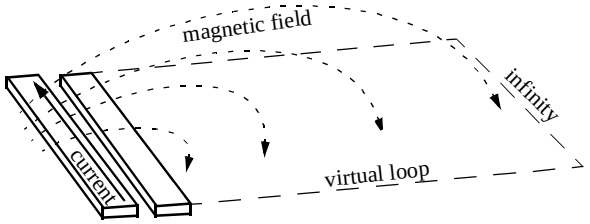


Fig. 7: Loop definition of partial inductance.

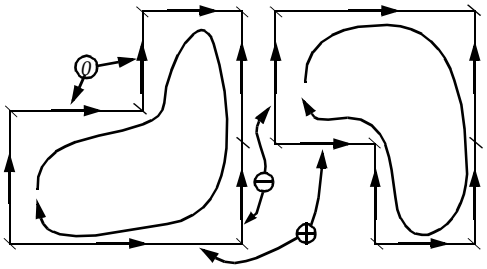


Fig. 8: Representation of current loops through partial inductance elements. The short arrows show the current directions, the long arrows identify the loop interactions. The signs of the S_{ij} terms are shown for selected segment pairs.

B. An Example

The example is a 32 bit bus structure with four in–plane return lines. The width is 0.18 μm, height and spacing are 0.36 μm and the length is 1 mm for all lines. For the signal lines the drivers are modeled by a 70 Ω resistor, the loads by a 2 fF capacitor. The resistivity of the wires is 17.5 nΩm (copper) and the dielectric coefficient is $\varepsilon_r = 3$. The input at the front end node of the active line (leftmost line) is a ramp from zero to one volt with a ramp time of 20 picoseconds.

The results in Fig. 6 show a significant difference with and without inductance for the response waveforms at the far end nodes of the active line and the immediately next neighbor. For the active line, the RC response converges exponentially to one volt, while the response for the same system including the inductive coupling exhibits ringing. The 50% delay difference is about 17% in this case. For the quiet line in Fig. 6b the positive maximum of the coupling noise is roughly 50% larger for RLC than for the case without inductance. In addition, the RLC noise becomes negative at times as well, while the RC response is always positive.

Since inductance can have a significant impact on the behavior of relatively small circuits, it becomes clear that modeling magnetic interactions for larger circuits must be made possible as well. The loop representation of inductive

interactions being obviously impractical in this case, we turn to modeling magnetic interactions between segments rather than loops via *partial inductance* models.

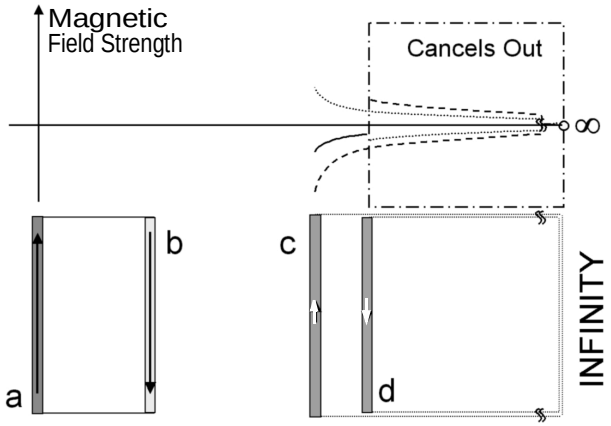


Fig. 9: Loop inductances reconstructed from partial couplings. **a** and **b** carry current, **c** and **d** have the shown orientation. The plot shows the magnetic field of **a**'s current (dotted) and **b**'s current (dashed) over the virtual loops of victim segments. Where the loops of **c** and **d** overlap, the flux from **a** and **b** cancels and what is left (solid line) is *exactly* the loop coupling similar to Fig. 3.

IV. Partial Inductance Models

A. Concept

Modeling general three–dimensional interconnects for which the return paths are not known *a priori* requires partial inductance elements. The partial inductance concept which was developed by Rosa [4] was introduced to the circuit modeling and analysis community by Ruehli [5].

Since the actual current loops are unknown, partial inductance is defined as the magnetic flux created by the current of one segment through the *virtual loop* which another (victim) segment forms with infinity (see Fig. 7). It can be shown that the loop inductances are equivalent to the sums of the partial self and mutual inductances of the segments which form all loops in the system. Referring to Fig. 8 we find the relationship between loop and partial inductances:

$$L_{ab,\,loop} = \sum_i \sum_j S_{ij} L_{ij,\,partial} \quad with \quad S_{ij} = \pm 1 \tag{8}$$

where *i* and *j* are segments of loops *a* and *b* respectively. The S_{ij} are –1 if *exactly one* of the currents in segments *i* and *j* is flowing opposite to the direction assumed when the partial inductive coupling $L_{ij,partial}$ was computed; the S_{ij} are +1 otherwise.

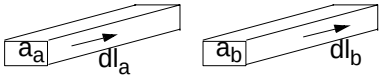
By *defining* each segment as forming its own return loop with infinity, partial inductances are used to represent the eventual loop interactions *without* prior knowledge of the actual current loops. Fig. 9 illustrates that loop inductances can be reconstructed from partial inductances and therefore the partial inductance model contains all the information about magnetic interactions which were contained in the loop inductance values. Ampere's Law and Faraday's Law apply to conductor segments as well (Figs. 10 and 11) and form the basis for deriving formulas to compute partial inductance values.

B. Partial Inductance Formula

To model magnetic interactions practically via partial inductance requires expressions to compute their numerical values. These can be found for given geometries of two coupled segments *a* and *b* by solving the integral

$$L_{ab,\,partial} = \frac{\mu}{4\pi a_a a_b} \int_{a_a} \int_{l_a} \int_{a_b} \int_{l_b} \frac{\hat{dl}_a \cdot \hat{dl}_b}{\left|\hat{r}_a - \hat{r}_b\right|} da_a da_b \tag{9}$$

Parameters in (9):



where a_a and a_b are the cross–sections of the segments and l_a and l_b their lengths. Eqn. (9) can be derived from Eqns. (3), (4) and (6). The details of this derivation can be found in Sections 2 and 4 of Reference [5]. Analytic solutions to (9) can become quite involved even for relatively simple geometries. For two parallel filaments with negligible cross–section the mutual partial inductance formula is

$$L_{ab,\,partial} = \frac{\mu}{4\pi} \sum_{k=1}^{4} (-1)^{k+1} f(s_k)$$
$$\text{with } f(s_k) = s_k \ln\left(s_k + \sqrt{s_k^2 + \rho_{ab}^2}\right) - \sqrt{s_k^2 + \rho_{ab}^2} \tag{10}$$
$$\text{and s1=d–la, s2=d+lb–la, s3=d+lb, s4=d}$$

where l_a and l_b are the lengths of the filaments and *d* their offset in length direction, while ρ_{ab} is the perpendicular distance between them. This and related expressions can be found in [7].

Expression (10) can be extended to evaluate the inductance between parallel conductors with finite cross–section by subdividing these conductors into filaments, applying (10) to each pair of filaments and adding the results. The interested reader is referred to Eq. (14) in [7] to see the exact expression for this situation. It is a correct formula, but not very robust and contains many numerical pitfalls. More analytic solutions for rectangular and triangular elements for practical implementations are provided in [6] and [7].

If all attempts at finding an analytic solution to (9) fail, there is still the possibility to use numerical integration techniques, such as Gaussian quadrature [8], to solve the integrals. These methods tend to be more robust and flexible than most analytic solutions, but also much more time–consuming during the extraction process.

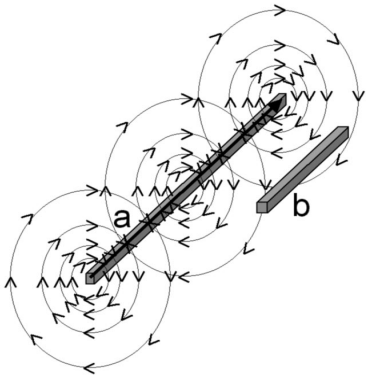


Fig. 10: Ampere's Law: Current flowing through segment **a** creates magnetic field.

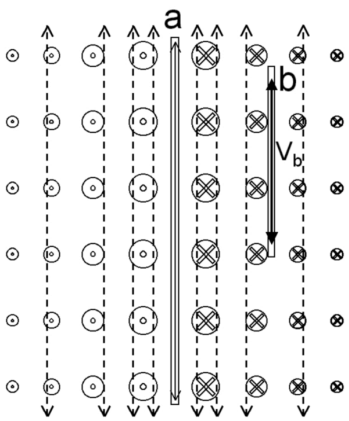


Fig. 11: Faraday's Law: Time–variant magnetic fields (circles and crosses indicate direction) create induced electric fields (dashed lines) which in turn create voltages in victim line **b**.

C. PEEC Models

Capacitive and partial inductive elements were combined with resistors in *partial element equivalent circuits* (PEEC) in [13] to enable modeling of IC interconnect using common circuit simulation tools. Each conductor segment is subdivided into filaments in cross–sectional and length direction, if necessary, to capture the nonuniform current densities in the conductors. Each filament is represented by a resistor and a self inductor in series and a capacitor to ground. Mutual inductors and capacitors are inserted between self inductors and circuit nodes as necessary for accurate modeling. These models usually exclude relativistic effects and electromagnetic radiation, but are sufficiently accurate for most integrated circuits even today. Capacitance can be sparsified quite easily, but to simulate the full partial inductive model is prohibitive. In [1], methods for reducing the model size while preserving accuracy and stability are reviewed.

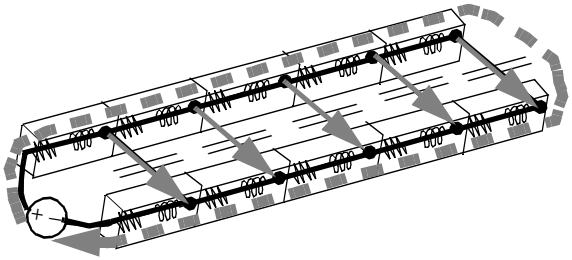


Fig. 12: Current return paths for loop inductance calculation. With capacitance (solid thick lines) and ignoring capacitance (dashed thick line). Mutual inductances not shown in this figure.

V. High–Frequency Effects

A. IC Current Return Paths

An approximation of the IC current return paths widely used for package–level systems is to assume that the signal nets are shorted at the far end to a ground or that a return line is placed nearby so that the entire return current path is known without capacitance in the model. The resulting model contains resistance and inductance only, which can be combined into a complex impedance matrix, if a single signal frequency is assumed. This RL impedance matrix can then be used to efficiently find loop inductances for long wires based on this simplified interconnect model. This assumes that the displacement currents through the capacitive couplings to neighboring nets are negligible. This would clearly be an invalid assumption for on–chip CMOS circuits, as described above (see Fig. 12).

To model the electromagnetic interaction accurately, long segments must be subdivided sufficiently in the current direction to account for the capacitive coupling at intermediate points of the line. As a consequence, assuming that all the current returns at the far end of the line can overestimate the wire inductance significantly. Coupling capacitors at intermediate points in the line drain ac current from the wire to neighboring wires before reaching the end of the conductor. This reduces the size of the current loops in the interconnect, hence reduces the loop inductance.

This suggests that for on–chip extraction the capacitive couplings should be known prior to inductance extraction. However, with this capacitance coupling information, the increased number of current loops makes calculation of the loop inductances difficult, if not impossible; hence PEEC models are necessary for on–chip interconnect.

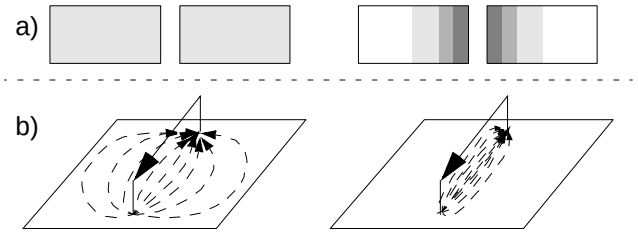


Fig. 13: *a)* Current distribution for signal line and its return; *b)* Current flow for a signal line over a ground plane; Left is low frequency, right is high frequency for both.

B. Proximity Effect

Even without considering capacitive couplings, increasing signal frequencies change the way currents flow within a given interconnect system [11]. Current will tend to flow the path of least impedance. For low frequencies the impedance is dominated by the resistance of the conductors. Since the conductors have a finite cross–section, the current will spread out over the given cross–section to minimize the overall resistance (see Fig. 13a, left).

As the signal frequency increases, the inductive component of the impedance, $R+j\omega L$, starts to dominate. The frequency at which this starts to happen depends on various factors such as resistivity and the dimensions of the conductors involved. To minimize the impedance, the loop size must now be minimized to reduce the loop inductance L. Therefore the current tends to return closer to the signal line (see Fig. 13a, right). Fig. 13b shows a similar example for a ground plane.

C. Skin Effect

A different cause for non–uniform current distribution within conductors for high signal frequencies is the *skin effect*. Electromagnetic waves are attenuated as they pass through conducting material (see Fig. 14). At a sufficient depth, all electric and magnetic fields are negligible and no currents flow. As a result, all currents flow close to the surface. The thickness of this surface layer is determined by the signal frequency and the conductivity of the material.

In Fig. 15 we find that this situation applies to conductors carrying high–frequency currents as well. An electric field *E* is created along the conductor by applying a high–frequency voltage. The resulting current creates the magnetic field *B* with the same frequency but with a quarter–period phase difference to *E*. Observing this locally (Fig. 15, right), the situation is equivalent to an electromagnetic wave with the given frequency trying to pass into the conductor and resembles the situation in Fig. 14. Therefore both fields *E* and *B* will be attenuated as we look further into the conductor. As the electric field weakens, the current flow will be less as well. Therefore, for sufficiently high frequency, current only flows within a layer close to the surface of the conductor.

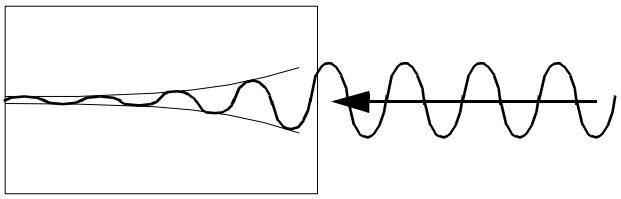


Fig. 14: Attenuation of electromagnetic wave as it passes through a conducting material.

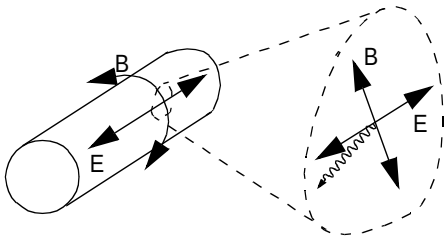


Fig. 15: High frequency electric/magnetic field form electromagnetic wave penetrating the surface of a cylindric conductor.

The skin depth δ is defined as the depth at which the field drops to 1/*e* of its surface magnitude, which is given by [9]:

$$\delta = (\pi f \mu\sigma)^{-0.5} \qquad (11)$$

where σ is the conductivity and *f* is the signal frequency. Usually the skin effect is modeled by subdividing the conductor into smaller filaments in the cross–section, each carrying a uniform current. The filaments on the surface are usually δ or 2δ thick. This allows the simulator to distribute the current non–uniformly throughout the cross–section, but causes the complexity of the interconnect model to increase. Some approaches try to model the frequency dependence via surface formulations to reduce the complexity increase [12].

Obviously, the skin effect will only be a problem if δ is significantly smaller than the largest cross–sectional dimension (usually width). For a signal frequency of 1 GHz and a conductivity of 5.7 x 10^8 $(\Omega\text{m})^{-1}$ (copper) the skin depth is roughly 1.2 μm. In general, for wires which are more than a micron wide *and* thick modeling the skin effect would be important. These are in general global power/ground and clock distribution nets [1].

VI. Conclusion

Magnetic interaction within on–chip interconnect is becoming a problem for the global power/ground and clock wiring. The complexity of integrated circuit wiring makes it necessary to use partial inductance, which models magnetic influence between pairs of conductor segments rather than loops, since the loops are usually unknown *a priori*.

The basic concepts of inductive interaction between conductive loops and segments were discussed and their application to circuits in form of PEEC models illustrated. Partial inductance formulas for calculating the interaction between linear segments were derived and approaches to modeling high frequency effects such as skin and proximity effects via partial inductance were presented.

Due to the slow decay of inductive couplings with distance between conductors and the resulting global nature of magnetic couplings, it is necessary to sparsify the partial inductance matrix to make the simulation of the RLC model more efficient. Furthermore, there exist some design techniques, such as including *shielding wires and layers* as well as using *staggered inverter patterns* for long bus structures to reduce or even remove inductive effects (see [14]). Limitations and advantages of these approaches to inductance sparsification and inductance avoidance will be discussed in the second part of this overview in [1].

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