Fault Characterizations and Design-for-Testability Technique for Detecting I_{DDQ} Faults in CMOS/BiCMOS Circuits

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ABSTRACT

This paper provides the results of a simulation-based fault characterization study of CMOS/BiCMOS logic families. We show that most of the shorts cause I_{DDQ} faults, while open defects result in delay or stuck-open faults. We propose a design-for-testability technique for detecting short and bridging faults in CMOS/BiCMOS logic circuits. The impact of this circuit modification on the behavior of the circuit in normal mode is investigated.

1. INTRODUCTION

Various modes of failures can occur in VLSI devices, where bridging fault has been shown to be a major contributor [4, 13]. Bridging faults are particularly important in BiCMOS technology because the high density of integration reduces the distance between lines and/or contacts.

We have reported in [11, 10] that the traditional stuck-at and delay fault models are not adequate for modeling the fault behavior of BiCMOS families. We considered delay faults, I_{DDQ} faults, intermediate level faults, stuck-open faults, and soft-level faults.

In this paper, we propose a new DFT technique for detecting the shorts and bridging faults in CMOS/BiCMOS logic families. We examine the effectiveness of this technique by investigating the fault characterization of different BiCMOS families, and by finding the percentage of defects which can be detected by this technique. This technique provides on-line testing of I_{DDQ} faults in Fully-CMOS (FCMOS) circuits. Therefore, it eliminates the need for test generation algorithms.

2. FAULT CHARACTERIZATION

The conventional BiCMOS gate, as shown in Figure 1 consists of a CMOS section which implements the logic, followed by a bipolar output stage for high driving capability. To examine the effects of possible manufacturing–related defects, a circuit level modeling and simulation was used. We consider the possibility of a short in each two terminals of a transistor, as well as an open in each of the three transistor nodes. Shorts are modeled as a small resistor (10Ω) between the two nodes. Open-circuits are modeled as a large resistor (10 MΩ) inserted between the affected node and the node to which it would normally have been connected. To model an open in the gate of an MOS transistor the resistance was tied to the substrate.

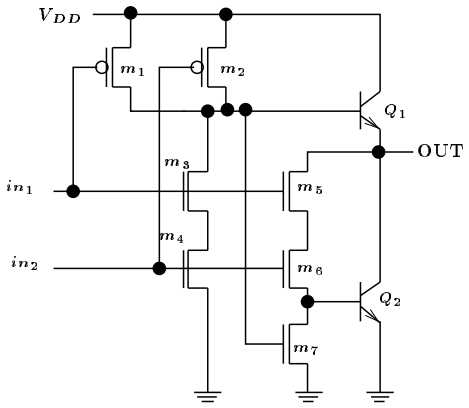

Figure 1: Typical implementation of a conventional BiCMOS NAND gate.

In order to make it easier for the reader to locate each fault on the circuit, we use the following notation: If a fault is caused by a short between two nodes, we refer to it by the first letters of those nodes, followed by the name of the transistor; e.g., a fault caused by a short between the base and emitter nodes of q_2 will be referred to as beq_2, while a short between the drain and source of m_3 will be called dsm_3. A fault caused by an open in a node, will be referred to by the first letter of that node, followed by the name of the transistor; e.g., an open in the collector of q_1 is called cq_1, while one in the gate of m_2 is gm_2. To avoid the complexity of dealing with multiple-defect case, we assume that not more than one defect can occur at a time.

A comprehensive simulation study was done for all possible single defects in the circuit. Simultaneous current monitoring was performed during simulations to measure I_{DDQ}.

Table 1 summarizes the fault distributions corresponding to solid short/open defects for the four mentioned structures. We have realized that most of the short defects in CMOS/BiCMOS circuits cause an I_{DDQ} fault, while most

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Fault	Percentage			
	Conv.	BiNMOS	Full-Swing	CMOS
Delay	30	22	43	25
I_{DDQ}	44	43	53	46
Intermediate	19	20	26	13
Stuck open	31	40	0	29
Soft level	17	13	16	25

Table 1: *Fault distribution for BiCMOS/CMOS NAND gates. The Full-Swing structure is actually a CMOS gate, connected in parallel with a conventional BiCMOS gate.*

of the open defects result in delay or stuck-open faults.

The sum of the fault percentages for each family of circuits studied is more than 100%. This fact shows that there are faults which fall under different categories because they behave differently depending on what the input excitations are.

3. DFT TECHNIQUE

Bridging between two nodes (including terminals of transistors) may create a low impedance path between V_{dd} and GND, thus increasing the quiescent supply current. Another effect of these defects is driving the output to an intermediate level, which is an undetectable fault in functional testing.

In this section, we show a circuit modification that can be applied to CMOS/BiCMOS circuits to improve their testability. The technique presented here is schematically illustrated in Figure 2.

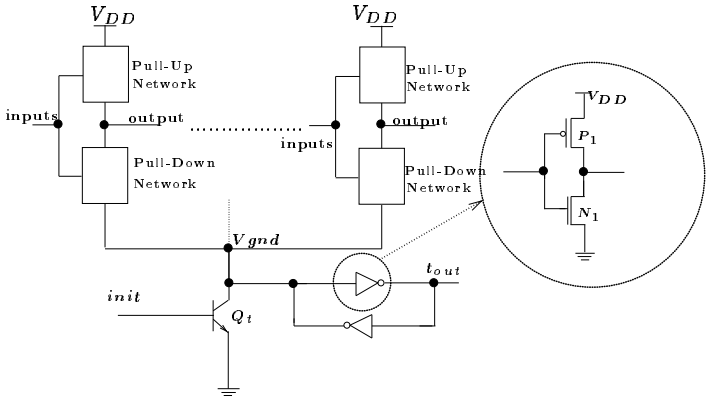

Figure 2: *Introducing virtual GND for detecting shorts.*

The basic idea is to introduce a virtual GND (V_{gnd}), which is forced to GND in the initialization mode. To achieve this, the control signal *init* must be ONE in initialization mode, thus connecting V_{gnd} to GND via the bipolar transistor Q_{t1}. In normal mode, the control line *init* is switched to ZERO. If no fault is present, no conducting path is established between V_{dd} and V_{gnd}. So, this node remains at logic ZERO. As a result, the output of the CMOS inverter (node t_{out}) will be logic ONE. On the contrary, if a path exists between V_{dd} and V_{gnd} due to a bridging, V_{gnd} can be charged to a high value, thus t_{out} is lowered to logic ZERO.

The main advantage of this technique over the proposed technique by Favalli *et al.* [2, 3, 5] is as follows. Since V_{gnd} is floating in test mode under fault-free condition in their proposed technique, its voltage is not guaranteed to be ZERO, and the normal leakage current may drive it to a voltage which is high enough to lower t_{out}. To overcome this problem, we have added another inverter in a feedback path. This extra inverter stabilizes t_{out} against temporary variations during transitions and keeps V_{gnd} at ZERO in the fault-free case.

An important feature of this technique is that there is no need for the input test sequence to excite the fault or propagate its faulty behavior to the primary output. Simulation is thus straightforward, as is its detection.

It should be noted that several stages in a VLSI circuit can share a common V_{gnd}, thus using a single test circuit.

Simulations were done for all the possible defects, including the possible defects in the test circuit. The input CMOS inverters were also modified by using V_{gnd} instead of GND. Transistor Q_t is replaced by an NMOS transistor, when applying the technique to CMOS structure. This is necessary, in order to keep the circuit compatible with CMOS technology.

67% of all possible shorts and bridging faults are detectable at t_{out}. All of the bridgings in the BiCMOS NAND gate which are not detectable are among those that create a conducting path which includes the base of Q_2. Since this point is kept at a low voltage ($V_{BE,on} \leq 0.8$ V), V_{gnd} cannot reach a voltage high enough to turn m_{t2} on. Since the BiNMOS and CMOS structures do not have a bipolar transistor in the pull-down path, their detection ratios increases significantly.

The DFT scheme of Figure 2 presents a few undetectable faults at the test circuit itself. For the BiCMOS NAND gate, ten (33%) defects at the test circuit are undetectable. However, none of them change the functional behavior of the NAND gate in normal mode, while in test mode they can produce masking problems only in the case of multiple faults. It should be noted that among 33 defects which cause an I_{DDQ} fault in the gate, approximately 78% are detectable by this method. All of those which are not detectable create the excessive current only through the node at the emitter of Q_2. Another method for achieving a complete I_{DDQ} fault coverage is to connect the emitter of Q_2 to V_{gnd}. However, this may degrade the noise margin as well as the delay performance, unless the area of Q_t is chosen properly. Table 2 shows the effectiveness of the proposed technique for the four studied structures. It should also be noted that as the

	BiCMOS	BiNMOS	FS	CMOS
Detectable I_{DDQ} faults	78	88	84	83

Table 2: *Fault detection comparison for 4 structures including the test circuit.*

number of the stages in the circuit increases, the detection ratio will increase, because there will be more paths to V_{gnd}. In order to verify this, a fully-CMOS master-slave JK flip-flop was designed using two-input NAND gates. Simulations showed that 98% of all the short defects in the functional part of the circuit are detectable by the proposed DFT technique. If the shorts in the test circuit are also taken into consideration, the figure drops to 92%, which is still a very high coverage.

Simulations show that this technique is still effective, if we model the shorts with larger resistances (e.g., 1K-10K).

In the test circuit, the sizes of m_{t2} and m_{t3} transistors (the first inverter) determine the required voltage at V_{gnd} which can lead to a fault detection, while the size of m_{t4} determines the maximum allowable I_{DDQ}. Thus, based on the complexity of the main circuit, the widths of m_{t2} and m_{t4} can be adjusted for correct operation of the test circuit.

Applying the proposed technique has the following effects on the normal behavior of the circuit:

- The output voltage, corresponding to the ZERO level (V_{OL}) increases by only 80 mV. Also, the $V_{IH,min}$ and $V_{IL,max}$ values remain unchanged. As a result, there is not a noticeable degradation in noise margin.

- In BiCMOS structures (conventional, and full-swing), the increase in the delay characteristics is minimal, because the bipolar transistors which drive the output capacitance remain unchanged. For BiNMOS and CMOS structures, there is a delay overhead, which can be minimized if Q_t (or its NMOS counterpart for CMOS) is chosen appropriately.

- There is an area penalty due to the added devices, and the two extra pins required for t_{in} and t_{out}. It should be noted, however, that since a test circuit can be used for several independent stages, this area overhead is not significant for VLSI circuits. If a circuit is large enough to need more than one test circuit, a single t_{in} can be used for all of them, and the local t_{out} outputs can be applied to a CMOS NAND gate to make a single test output.

- No DC power is dissipated in the test circuit, because it is fully CMOS. Also, the transistor Q_t which is ON in normal mode does not contribute excessive power, because it is in saturation region at steady-state situations (for CMOS structure, the NMOS transistor which replaces Q_t will be in linear region, with no power dissipation). For the conventional BiCMOS NAND gate, the steady-state power dissipation increased from 0.3nW to 0.5 nW. For a more complex system with a higher power dissipation, the increase will be quite insignificant, because only one test circuit will be used for the circuit.

These overheads can be well justified by the enhanced testability of the circuit.

4. MEDIUM SIZE LOGIC CIRCUITS

We have explained how the proposed I_{DDQ} test circuit works and compared its performance with those available in the literature. Advantages and disadvantages have been outlined. This comparison is limited to the functionality of the test circuit for the following reasons.

Automated Test Pattern Generation programs have been developed to find test vectors for I_{DDQ} fault detection purposes. Such test patterns have been graded 92% [9], 97% [12], and 98% [8]. Fault coverage reported by ATPGs is not the same as fault coverage reported for actual hardware[1].

Many published results on I_{DDQ} faults do not provide exact transistor sizes or the schematic diagram of the circuit under test. Moreover, there is no benchmark for I_{DDQ} fault testing.

Injecting I_{DDQ} faults on a fabricated chip and testing the chip for I_{DDQ} fault using DFT techniques is not helpful since each injection requires one chip being fabricated. This is not practical, and for this reason, there is no fault coverage reported in the literature today on this bases.

Obtaining fault coverage using I_{DDQ} fault injection on a circuit at the simulation level is also difficult. This means that a faulty circuit should be simulated using SPICE. The fault coverage is obtained after simulation is performed for each I_{DDQ} fault. This is tedious as it has to be done manually. For this reason, there is no fault coverage reported in literature for I_{DDQ} fault testing using DFT testing techniques. To the best knowledge of the author, DFT fault coverage for I_{DDQ} faults has been reported in this paper for the first time.

We have selected three circuits for fault simulation which satisfy the following conditions.

- *Medium Size Circuits:* Since HSPICE simulation should be carried out for each line stuck-at fault which causes increased I_{DDQ}, we have selected medium size circuits.

- *Modularity:* In order to simplify data entry for HSPICE, we have used modular designs. Such designs are easily duplicated in HSPICE entry file giving us an opportunity to increase the size of the circuit as we wish. This will allow us to observe relationships between test circuit and circuit under test in terms of area overhead and fault coverage.

- *Input Criterion:* We have proposed I_{DDQ} testing technique which works on-line, and there is no need for ATPGs. Since we have simulated faulty machines for each input combination to test the design exhaustively, we have selected designs which have only a few inputs.

An 8-bit parallel binary full-adder [7], an 8-bit digital multiplier [7], an ALU (74181), and an 8-to-256 decoder[2] [7] are the subjects for our I_{DDQ} testing.

The simulation has been carried out as the following steps describe.

- The logic designs have been changed to include only 2-input NAND gates and inverters.

- Gate-level designs have been transformed to transistor-level designs using CMOS NAND gates and CMOS inverters. NMOS and PMOS transistor sizes are the same as the ones we considered in this paper.

- We have considered fault-free input signals. All possible input combinations have been employed at the inputs using phase shift technique[3] similar to the inputs

[1]We distinguish between fault coverage produced by test generation programs, and the transistor-level fault coverage. Fault coverage provided by a simulator is the ratio of the number of faults detected by test set to the total number of simulated faults. This figure is directly relevant only to the faults processed by the simulator; hence, a test with 100% fault coverage may still fail to detect faults outside the considered fault model by the simulator. Here, we have provided the actual fault coverage. We have counted every possible fault. Our fault coverage report is the first of its kind.

[2]An 8-to-256 decoder is constructed using seventeen 4-to-16 decoders.

[3]Other possible techniques are *frequency division* and counter.

we applied for NAND gate simulations. This allows us to manage an exhaustive testing.

- We have injected line single stuck-at faults and short faults and enumerated I_{DDQ} faults by monitoring the power supply current. This is performed without test circuit.
- We have connected our proposed I_{DDQ} test circuit between virtual ground and actual ground, and simulated the circuit with single stuck-at faults. The only output monitored was t_{out}. (The primary outputs have been ignored.) A fault is detected if t_{out} is zero, and the fault is not detected if t_{out} is one.

Table 3 provides simulation results. We have been able to

Circuit structure	8-bit Adder	8-bit Multiplier	ALU 74181	Decoder
Detectable I_{DDQ} faults (%) including the test circuit	98.6	99.4	98.7	99.6

Table 3: *Fault detection comparison for four MSI structures.*

make the following observations through simulations.
Observation 1: Our I_{DDQ} test circuit works based on the observation of supply current and it is independent of the voltage levels of internal nodes or primary outputs.
Observation 2: The area overhead is linearly proportional to the size of the circuit. We have used one proposed I_{DDQ} test circuit (two CMOS inverters) per nineteen 2-input CMOS NAND-gates. This is roughly 5.2% increase in area overhead. The transistor sizes for test circuit are selected by try and error technique, and we speculate that this area overhead could be reduced. However, this area overhead is little price to pay to gain high I_{DDQ} fault coverage without the price of test generation attached.
Observation 3: The structure of a group of nineteen NAND gates have the same static and dynamic supply currents when the same number of transistors in circuit under test turned *on* or *off*. That is why we speculate that the fault coverage obtained would be roughly 99.5% for LSI circuits. This speculation can best be visualized using dual adder (multiplier) where the corresponding inputs of 8-bit adders (multipliers) are tied together. Any change that happens in one adder (multiplier) is duplicated and detected in the other part as well. Like other proposed I_{DDQ} testing techniques, partitioning should be used to deal with LSI circuits. However, our proposed I_{DDQ} test circuit has only four transistors which is very small compared to 23 NMOS and PMOS transistors proposed in [6] or 12 NMOS and PMOS transistors in the I_{DDQ} test circuit proposed in [1].

5. CONCLUSIONS

In this paper, we have characterized the effects of physical defects on different PUPD CMOS/BiCMOS families. Our study confirms that the traditional stuck-at and delay fault models are not adequate for modeling the fault behavior of BiCMOS families. In order to achieve a high level of defect coverage, I_{DDQ} testing must also be employed. We presented a new design-for-testability technique for BiCMOS/BiNMOS/CMOS logic gates that results in a high coverage for shorts and bridging faults. It eliminates the need for fault excitation or propagation. The voltage levels of internal nodes remain in their defined logic level range of ZERO or ONE in fault-free circuit.

The impact of this circuit modification on the behavior of the circuit in normal mode has been investigated.

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