Improving Bus Test Via I_{DDT} and Boundary Scan

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ABSTRACT

This paper presents a systematic test methodology targeting bus line interconnect defects using I_{DDT} testing and Boundary Scan. Traditional test is unable to detect all possible defects, especially timing-related faults. Open and short defects on interconnects between embedded modules can be detected by I_{DDT} testing. Boundary Scan can provide accessibility to internal buses. A statistical analysis is presented discussing the uncertain factors due to process variations and power fluctuation. The effectiveness of the proposed technique on shorts, opens or the other non stuck-at fault type defects is also illustrated.

Keywords. IDDT, Current Test, Boundary Scan, Interconnect.

1. INTRODUCTION

Today's advanced VLSI technology uses a variety of embedded cores in a single chip connected through buses. They are connected together through a common interface, drivers and/or receivers. Specific drivers are used to drive long metal lines in order to propagate the signals to other ends. Consequently, a bus system with long wires their resistance and capacitance may cause excessive noise affecting circuit's performance [1]. According to the SIA Roadmap, significant rise in the critical path delay in Deep SubMicron (*DSM*) technologies is mainly attributed to interconnects [2]. Although noises might be minimized during design, manufacturing introduced defects, e.g. bridging or opens, may exaggerate their effects. These effects include delay, glitches or transient faults [2][3][4]. Other DSM defects are due to Electromigration [5].

Traditional test techniques are unable to detect DSM defects in advanced circuits. The I_{DDQ} test methodology supplements traditional testing by monitoring the static supply current in CMOS. However, the effectiveness of I_{DDQ} testing in DSM is reduced by the increasing sub-threshold leakage in CMOS transistors. Thus, I_{DDT} testing becomes a better alternative than I_{DDQ} testing for DSM. The essence of I_{DDT} is to capture the current due to the transistor switching activities. This current could range from μA to mA, which is much larger than I_{DDQ} (about hundreds of nA). Moreover, I_{DDT} testing can perform at a higher speed and higher resolution than I_{DDQ}, which has to wait till the current reaches the quiescent state [6][7][8][9][10].

Frenzel et al. applied a Power Supply Signature Analysis to compare the complete power supply current of the circuit under test to the one of the fault-free circuit [11]. Makki et al. monitored the dynamic current across a resistor connected from the power supply to the circuit power bus [12]. Plusquellic et al. analyzed the transient signals of a device measured simultaneously at multiple test points [13]. Beasley et al. monitored the transient current by pulsing the power supply rails [14]. Cole et al, detected the changes in power demand of ICs owing to the limited response time of a voltage source [15]. Vinnakota reduced the impact of process variations by using the ratio of the energy dissipated from two distinct input vectors [16].

For an embedded design, test access to each individual core has to go through the core's test interface. Many proposals presented at the IEEE P15000 suggest that boundary scan design is still an appropriate test structure for interconnects. Therefore, we adapt Boundary Scan to be our test access structure [17]. Since the fault detection mechanism of Boundary Scan is based on the stuck-at fault model, improving the defect coverage of boundary scan by integrating I_{DDQ}/I_{DDT} testing is needed. Reed et al. integrated Boundary Scan and I_{DDQ} by using an on-chip monitor [18]. Since transient current only exists during the transitions of the MOS transistors and the period is short, it is very hard to trace it without using expensive probing equipment. We propose a charged-based on-chip current sensor to solve this problem.

2. BACKGROUND

The embedded cores have an interface circuitry to interact with the interconnect system. At output/input ports, drivers/receivers isolate interconnects from the core logic and bus repeaters maintain signal integrity. An interconnect line (metal) could simply be modeled as a group of uniformly distributed RC networks.

The shape of transient current waveform could be very complicated to inspect. We propose a charge-based methodology that applies I_{DDT} testing systematically to collect the dissipated charge of interconnect bus during test. Our assumption is that the driver block usually is composed of inverters with power transistors. The dissipated charge is caused by the following three types of current in a CMOS circuit.

1. The major contribution of the dissipated charge comes from the switching current. This current is due to the charging and discharging of parasitic capacitors (including transistor and load capacitance) associated with the transitions of internal nodes and gates.

2. Short current occurs when a direct path between the power supply node and ground is established due to simultaneously turning on both nMOS and pMOS transistors.
3. Leakage current is the background current, which is measured during a stable state. It is of the order of nano-amperes. Generally, it may be ignored for I_{DDT} testing.

3. PROPOSED TEST SCHEME

Our approach employs Boundary Scan to solve the accessibility problem of bus/interconnect from outside the die and a Built-In Transient Current Sensor (*BITCS*) to capture the test responses. Boundary Scan wraps around embedded cores by inserting Boundary Scan Cells (*BSC*) between the interconnect drivers and core logics, thus separating the two of them shown in Figure 1.

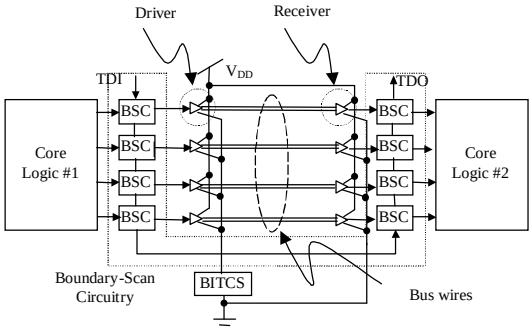

Figure 1: I_{DDT} Testing Scheme with Boundary Scan

3.1 A Feasible Built-in Current Sensor

A built-in sensor integrated in a common CMOS fabrication process with other circuitry is shown in Figure 2 [19]. A circuit mirror serves as a current sink to reduce transient current across the built-in capacitor and isolate the test circuitry to avoid disturbing the normal driver operations. Some works proposed an unbalanced CMOS current mirror to reduce the monitored transient current without losing its sensitivity [20]. The down side is the offset current continues flowing through the circuit under test while the power is engaging. Therefore, we cannot measure I_{DD} at a steady point. Using an A/D converter to interpret the analog signal also increases the cost and loses test resolution. Instead of that, we proposed an on-chip sensor converting the dissipated charge into the associated test time.

Our current mirror reduces the impact of the voltage elevation of the ground during testing by applying a negative pull down voltage ($-V_T$) equal to the threshold voltage of M1. We can also wire the ground out during normal operation via the diamond shape node. Not only did we reduce the M1 size but also eliminated the need of dual polarity power supply. The tradeoff is one extra primary output pin. M1 serves as a current sink for a large amount of current during normal operation and always operates in the saturation region. It should support the current from the driver block. Hence,

$$(\overline{W})_{M1} \geq k(\overline{W})_{Drivers}$$

where k is the number of bus drivers connected to the sensor, and (W/L) is the transistor's channel width/channel length.

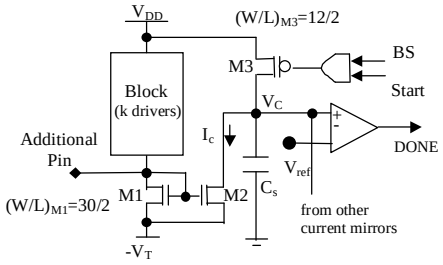

Figure 2: A Built-in Current Sensor

For large transient current, k becomes very large, ending up with an impractical W/L value for M1. To solve this problem, we partition interconnect drivers into several smaller blocks. Each small block comes with an identical current sensor. For example, after partitioning, there are m equivalent blocks and each block has k drivers which must drive different lines. Thus, we need m built-in identical sensors. For an n-bus line, $m=[n/k]_{ceiling}$. To efficiently use the sensor, k must be at least 2. On the contrary, M2 should be as small as possible to reduce the size of capacitor C_s. Since M1 and M2 are fabricated on one chip, they have common semiconductor parameters. The ratio α of the drain to source current between M1 and M2 transistor is

$$\alpha = \frac{I_{M1}}{I_{M2}} = \left(\frac{W}{L}\right)_{M1} / \left(\frac{W}{L}\right)_{M2}$$

where I_{M1} and I_{M2} are the drain to source current of M1 and M2 transistors, respectively.

3.2 VOLTAGE COMPARATOR AND BUILT-IN CAPACITOR

A voltage comparator is used to compare the capacitor voltage with a reference voltage V_{ref}. Signal **DONE** indicating the completion of one sub-test becomes high when V_c drops below V_{ref}. The value of C_s is critical. C_s cannot be too small to contain all the induced charge by the M2 current in a single cycle. Yet, a large C_s may end up with longer test time. Assume that the sensor must have at least 1% resolution and it is placed at the ground end; then we must have

$$C_s \Delta V_r > 100 \times C_{load} \times V_{DD}$$

where ΔV_r is the voltage difference between V_{DD} and V_{ref}, and C_{load} is the load capacitance of the driver block. V_{ref} is the reference voltage and usually larger than V_{th}(M2), the threshold voltage of the transistor M2. M2 keep operating in the saturation region before a sub-test completes. Transistor M3 controls the charging operation of the capacitor. Its size must be large enough in order to pre-charge the capacitor before the next sub-test starts. In CMOS fabrication, it is very hard to accurately process a built-in capacitor with a desired capacitance. We will need to use a statistical analysis to manage the influence of capacitor variations.

3.3 SPICE Simulation of the Current Sensor

Fr a 2mm×1μm metal-3 wire implemented in HP CMOS14TB 0.5μm technology (λ=0.3μm), the resulting capacitance of M3 to substrate according to the previous capacitance equation is

$2mm \times 10^3 \mu m/mm \times (0.0092 + 2 \times (0.0054 + 0.1021) fF/\mu m = 0.4484 pF$

Suppose a poly-active capacitor with 3500 aF/μm^2 and V_{ref} is equal to ½V_{DD}. V_{DD} is 3.3Volt. To reach 1% resolution, the capacitor area is 256×100 μm^2. If I_{M1}/ $I_{M2}(\alpha)$= 100, we reduce the capacitor area to 256 μm^2.

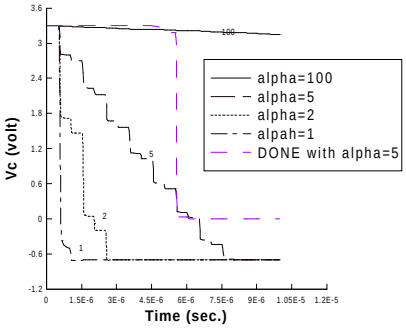

Figure 3: Dissipation Ratios of V_c due to Different α Values

Figure 3 shows the voltage drop at V_C for four different values of α, which are 1, 2, 5 and 100. The aspect ratios of p-channel and n-channel transistors of the drivers are $(W/L)_p$=(12/2) and $(W/L)_n$= (3/2) respectively. The aspect ratio of M1 is $(W/L)_{M1}$= (30/2) for all simulations while we changed $(W/L)_{M1}$ to (30/2) when α=1, (15/2) when α=2, (6/2) when α=5,or (3/20) when α=100. We assumed the drivers load capacitance and output impedance are 0.4484pf (interconnect capacitance) and 50Ω respectively. To match the load capacitance, C_s is defined as 0.4484pf. Signal **DONE** falled to low while V_C drops below 1Volt.

4. POWER CONSUMPTION SIGNATURE ANALYSIS

The efficiency of I_{DDT} testing can be significantly degraded due to process and power variations. To alleviate their impacts on testing, we propose Power Consumption Signature Analysis (*PCSA*). PCSA is to look for the high probability of matching among different components in a circuit by using statistical analysis on the information that all components on a die use a common process. It is very suitable for testing multiple identical components in a circuit like the interconnect system. For n-line bus, the dimensions and relative positions for these wires are determined and fixed after the layout completion.

Definition 1: *Given an n-line bus, its power consumption signature [PCS_1, PCS_2, .., PCS_n] is a n-dimension vector whose elements are the ratios of the amount of the dissipated charge of the wires to their average charge for a set of common input vectors.*

In Figure 4, the induced capacitance C_2 for $Line_2$ includes the area capacitance $C_{2,L}$ of $Line_2$ to top (bottom) layer and the line capacitance $C_{2,1}$ and $C_{2,3}$ of $Line_2$ to $Line_1$ and $Line_3$ respectively. The line to top (bottom) capacitance depends on the isolated distance between line and top (bottom), the geometry of line (line length × line width × height), and dielectric. The factor of line geometry mostly relies on its area capacitance (line length × line width).and fringing capacitance line (line length × height). Mostly, area capacitance for bus lines in a same layer are identical. The line-to-line capacitance also depends on the distance between two lines, the dielectric, and the line geometry. Usually, the middle line has higher capacitance than the outer lines. For bus lines, they have same geometry, dielectric and length (for most buses), so the stored charge on an individual line is proportional to the wire length. In the real world induced capacitance exists among different layers. The value of line capacitance can only be estimated after placement and routing

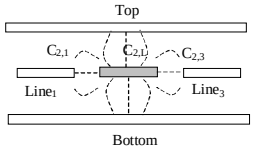

Figure 4: The Induced Capacitances in a 3-line Bus

Suppose the dissipated charges at three wires are Q_1, Q_2 and Q_3. L_1, L_2 and L_3 are the wire lengths, respectively, obtained from the layout tool. PCS vector is then

$$\overrightarrow{PCS} = [PCS_1, PCS_2, PCS_3] = (L_1 + L_2 + L_3)/(Q_1 + Q_2 + Q_3)[Q_1/L_1, Q_2/L_2, Q_3/L_3]$$

Most bus lines have identical length. In a physical circuit, the amount of dissipated charge may vary due to process variations. A successfully defined design corner is very important to the effectiveness of this method. Therefore, an escape vector is defined by specifying the limits of the safe zone

Definition 2: *An escape vector [s_1, s_2,…, s_n] is a vector whose elements are equal to the standard deviation of the power consumption signatures PCS's which are statistically obtained from the previous runs.*

Escape vector is a statistical measure of how widely values are dispersed from the average value. A safe zone is the area where a circuit is considered as non-defective if all elements of its power consumption signature are located within the region shown in Figure 5.

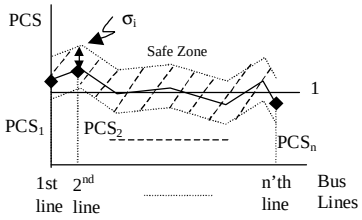

Figure 5: The PCS Vectors

PCS analysis measures the total consumption charge, which is the integral of the transient current during a given period of time T. As we know, a wire in an integrated circuit can be considered as a large capacitor. At the charging cycle, I_{DD} flows from the power supply to elevate the voltage level of the line being V_{DD}. During the discharging period, I_{DD} flows to the ground, causing the voltage level back to zero. Therefore, the charge Q_i at each node *i* can be derived by the following equations.

$$Q_i = \sum_j C_{ij} (V_i(t) - V_{ij}(t))$$

where C_{ii} is the capacitance of the *i*'th node to the substrate, C_{ij} is the coupling capacitance between the *i*'th line and the *j*'th line, and $V_i(t)$ is the instant voltage at the *i*'th node. The total dissipated charge Q_{total} for the interconnect system is the summation of Q_i. the dissipated charge for a single transition occurring at node *i* is obtained by using specific test vectors.

$$Q_i = V_{DD} \sum_j C_{ij}$$

where V_i=V_{DD}, else =0. Hence, the average power consumption (avQ) for the interconnect system becomes

$$avQ = \frac{\sum_i Q_i}{n} = \frac{V_{DD} \sum_i \sum_j C_{i,j}}{n}$$

where $1 \le i, j \le n$.

When all wires are identically long, the PCS vector besomes

$$\overrightarrow{PCS} \equiv [Q_1, Q_2, ..., Q_n](1/avQ) = \left[\frac{n\sum_i C_{1,i}}{\sum_i \sum_j C_{i,j}}, \frac{n\sum_i C_{2,i}}{\sum_i \sum_j C_{i,j}}, ..., \frac{n\sum_i C_{n,i}}{\sum_i \sum_j C_{i,j}} \right]$$

After placement and routing, the final geometry of interconnect is determined. Then, we compute the PCS values with the parasitic parameters extracted by an extraction tool. If there exists a coefficient α on C_s due to the global process variations, α will be eliminated. In the other words, PCS analysis is done extensively by computing the capacitance difference among all individual lines, so capacitance-related defects is detectable.

Ideally, the elements of the PCS vector in a interconnect system should approach 1 due to all bus lines are identically long and wide. If a short occurs in interconnects, the static current will increase due to the bridging between lines. PCSA will show extremely unbalanced shape. But if they are shorted all together, PCS could become [1,1,..,1], too. However, the short is detectable by observing the average dissipated charge. In practice, each individual line should have different line capacitance unless they are exactly identical 2-line bus or they are shorted all together.

4.1 TEST STRATEGY

A safe zone defined by a standard deviation $\pm\sigma$ is used to guarantee the successful separation of the good circuits from the bad ones with the variance of the PCS analysis. Unless all the elements of the PCS matrix for a circuit fall into its safe zone, it is considered as failed. The test strategy is shown in Figure 6.

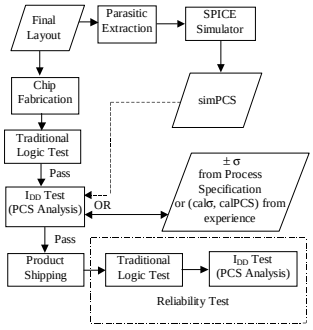

Figure 6: Test Strategy for Power Consumption Signature

When we have the final layout, we use a parasitic extraction tool to create a RCL network for the interconnect system. A SPICE tool is used to run a PCS analysis. *SimPCS* derived from technology parameters. $sim\sigma$ is an estimated value from the manufacturing yield of the past. The fabricated chips in a run have to pass traditional test. If it passes, we continue to I_{DDT} test. If this is the first run of this chip, we compare the test result with *simPCS* and simσ. Otherwise, we compare the test result with the ones (*calPCS* and $cal\sigma$). *calPCS* and $cal\sigma$ are the historical statistics from the previous PCS analysis. Under normal distribution, $calPCS_i$ is the median of the values of PCS_i, and $cal\sigma_i$ is the standard deviation. So

$$calPCS_i = \frac{\sum_{good\_ciruits} PCS_{in}}{n}$$

$$cal\sigma_i = \sqrt{\frac{\sum_n (PCS_{in} - PCS_i)^2}{n}}$$

where i is the i'th element of the PCS vector and n is the number of the good circuits that pass the traditional test. *calPCS* and $cal\sigma$ will be updated after the completion of testing. After product shipping, the PCS technique traces the variation of interconnect capacitance for reliability test.

4.2 Test Vectors for Our Test Scheme

Our test strategy is to measure each bus line individually. When we test a single line, we apply a sequence of pulses on it. A set of two-pattern test vectors is used to generate pulses. Each test vector consists of 2 different patterns applied on a single line for interconnect testing. For n line bus, we will issue 2n test patterns to n wires. Each two-pattern vector repeats until one line test completes. For example, the patterns for the first two-pattern vector in a three-line bus are (000 and 100). They are repeatedly applied on the bus wires. After one sub-test is complete, we apply the second two-pattern test vector on the second line, and so on. The test sequence is shown in Figure 7. When all done, we apply the compliments and repeat the same test again.

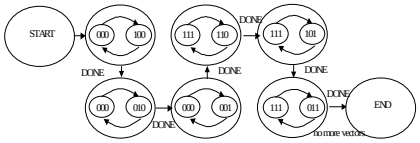

Figure 7: Test Sequence for a 3-line bus

4.3 PCS Modeling and Simulation

We conducted an experiment with four coupled identical lines in a bus environment. Our environment follows the technology HP AMOS14TB. We conducted electromagnetic (*EM*) analysis at 50 MHz to extract parasitic parameters. Four M1 wires were placed parallel with 1μm above the substrate. Their length and width are 2mm and 1μm. Artificial defects were injected into the lines by inserting notches (D1) or placing hole on the lines (D3). We also created an example of irregular geometry. Open and short faults were considered too. In our case, Line 2 is defective.

EM analysis generated a SPICE transmission line model. Port 1 to Port 4 connect to inverters individually; say Driver 1 to Driver 4. We obtained our transistor parameters from MOSIS. M1 capacitance has 0.179 variation. Therefore, if the deviation of test data is over 0.179, we consider it fails. The dissipated charge was monitored at the ground end of the driver block. Pulses were applied to the driver input while the other one remained quiescent. The pulses were at 50MHz with the duty cycle 50% and the rising and falling time of 2ns. Supply voltage is 3V. Our simulations ran at three different modes. The 1st run was at 3volts and used the MOS models derived from the 1st run. The 2nd run was conducted using the MOS models derived from different runs. The last one ran at 3.3 volts with the 1st model.

Table 1: PCS Signatures using 1st Run Models and 3 Volts

	PCS_1	PCS_2	PCS_3	PCS_4	σ_1	σ_2	σ_3	σ_4
good	0.96	1.03	1.03	0.98	0.18	0.18	0.18	0.18
open	1.13	***0.5***	1.22	1.14	0.18	***-0.51***	0.18	0.16
short	***1.92***	***1.92***	***0.08***	***0.08***	***1.00***	***0.86***	***-0.92***	***-0.92***
D1	1.08	0.89	1.12	0.91	0.13	-0.14	0.09	-0.07
D3	1.02	1.01	1.01	0.97	0.06	-0.02	-0.02	-0.01

Table 2: PCS Signatures Using 2nd Run Models and 3 Volts

	PCS_1	PCS_2	PCS_3	PCS_4	σ_1	σ_2	σ_3	σ_4
good	0.97	1.02	1.03	0.98	0.19	0.19	0.19	0.19
open	1.18	***0.56***	1.07	1.19	0.22	***-0.45***	0.04	0.21
short	***1.92***	***1.92***	***0.09***	***0.08***	***0.98***	***0.88***	***-0.91***	***-0.92***
D1	1.07	0.9	1.12	0.91	0.10	-0.12	0.09	-0.07
D3	1.02	1	1.01	0.97	0.05	-0.02	-0.02	-0.01

Table 3: PCS Signatures Using 1ST Run Models and 3.3 Volts

	PCS_1	PCS_2	PCS_3	PCS_4	σ_1	σ_2	σ_3	σ_4
good	0.97	1.02	1.03	0.98	0.19	0.19	0.19	0.19
open	1.11	***0.58***	1.18	1.12	0.14	***-0.43***	0.15	0.14
short	***1.92***	***1.92***	***0.08***	***0.07***	***0.98***	***0.88***	***-0.92***	***-0.93***
D1	1.06	0.91	1.11	0.92	0.09	-0.11	0.08	-0.06
D3	1.02	1	1.01	0.97	0.05	-0.02	-0.02	-0.01

Table 4: PCS Signatures for Curved Bus Lines

	PCS_1	PCS_2	PCS_3	PCS_4	σ_1	σ_2	σ_3	σ_4
good	0.97	1.02	1.02	0.99	0.18	0.18	0.18	0.18
open	1.10	***0.57***	1.17	1.15	0.13	***-0.44***	0.15	0.16
short	***1.91***	***1.91***	***0.09***	***0.08***	***0.97***	***0.87***	***-0.91***	***-0.92***
D1	0.97	0.98	1.03	1.01	0.00	-0.04	0.01	0.02
D3	0.96	1.03	1.01	1.00	-0.01	0.01	-0.01	0.01

Table 1-3 list the PCS signatures and standard deviations of four straight wires. Table 4 lists the cases have curves. According to these tables, opens and shorts have deviations over 20%. Obviously, PCS analysis detects opens and shorts. However, the wires defective due to their geometry and electro-migration are obviously hard to differentiate from good circuits. Therefore, another test scheme should be used to detect them. We will address it in the future research.

5. INTERCONNECT TESTING WITH BOUNDARY SCAN

The 1149.1 IEEE Boundary Scan provides a test environment that can access the I/O of embedded cores from top-level. We can just use an additional power source connected to the interconnect drivers and monitor the transient current waveform externally. This approach could reveal more signal information. However, the traditional dynamic current testing result is hard to capture without expensive external test equipment especially in a very high-speed circuit. Moreover, due to the complexity and variety of possible current waveforms, it becomes very difficult to detect a defective device by monitoring the consumption current waveform. Our idea is to use our BITCS which simply count the number of test cycles during a repeated test vector period instead of using an A/D converter to interpret the analog waveform as digital signal.

5.1 Enhanced Boundary-Scan Cell

To utilize Built-in Transient Current Sensor *(BITCS)*, we need to generate interconnect test vectors which must be able to target the defect. We had shown earlier how to design a set of test vectors and repeatedly apply these pulses to the wire under test. Since there is no extra clock cycle to wait for another vector, at-speed test is possible.

In order to provide the capability for traditional test as well as I_{DDT} testing, we modified Boundary Scan Cells *(BSC)*, as shown in Figure 8. The proposed enhanced BSC keeps the original boundary scan function but also becomes a two-pattern vector generator (a pulse generator) as needed. The identical feature for bi-directional I/O ports is available too.

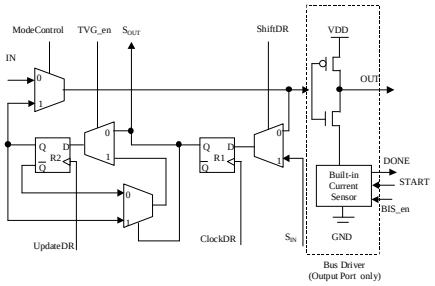

Figure 8: Enhanced Boundary Scan Cell

In Figure 8, the instruction registers control two control signals, **TVG_en** and **BIS_en**. Their mechanism is illustrated as follow

i. **TVG_en** = 0, the BSC works like a standard boundary-scan cell.

ii. **TVG_en** = 1, the BSCs at output pin are configured as a two-vector set test pattern generator, while the BSCs at input pin are used to capture the data for stuck-at fault detection.

iii. **BIS_en** = 1 is a global signal that activates the built-in sensor and Test clock bypass feature.

iv. **DONE** also is a global signal that is connected to **TDO** by muxing with the output of the last BSC in the scan path. MUX selects the **DONE** signal when **BIS_en** =1 and **START** =1.

v. TAP controller generates the signal **START**. The purpose is to trigger the sensor to start.

One additional instruction "***CEXTEST"*** utilizes this test structure. It is mostly like the EXTEST instruction except it enables I_{DDT} testing. A test clock bypass signal pauses state "UPDATE-DR" during I_{DDT} testing shown in Figure 9. Signal **START** comes out from the TAP controller to activate the bypass circuit. The bypass circuit is then disabled by signal **DONE**.

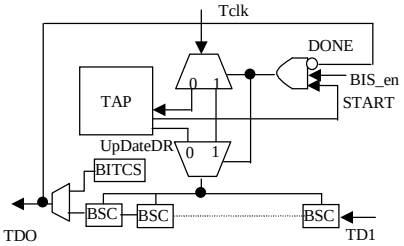

Figure 9: Modified Boundary-Scan with the Bypass Circuit

5.2 I_{DDT} Testing via Boundary Scan

A standard boundary scan instruction, ***EXTEST***, preset R2 at the output ports to a desired state. Due to the functionality of the proposed current sensor, the state of the BSCs after the

completion of a sub-test is unpredictable. The ***EXTEST*** instruction presets the BSCs by enabling the scan operation. The BSCs at the output pads are used to drive the pads. The input cells capture the test data while the TAP controller enters the Capture_DR state. Two instructions, ***EXTEST*** and ***CEXTEST***, swap back and forth for each two-pattern vector shown in Figure 10. *EXTEST* presets the data-register to the proper state. Then, we run I_{DD} test using *CEXTEST*. Therefore, the test cycle (the number of clock cycles to complete a test vector) is

$$TestCycle = 2 \times (11 + lengthIR + lengthDR) + (C_S / C_{int})(clock\_cycles)$$

where lengthIR and lengthDR are the lengths of the instruction register and the data register. C_c is the capacitance of the built-in capacitor and C_{int} is the interconnect capacitance

```
RESET/INITIALIZE all Boundary-Scan Registers;
FOR EACH I_DD test pattern
{  CLEAR counter_clk_cycle;
   SELECT IR-Scan;
    ISSUE EXTEST command;
   UPDATE IR;
   SELECT DR-Scan;
   PRESET DR with predefined vectors;
   UPDATE DR;
   SELECT IR-Scan;
   ISSUE CEXTEST command;
   UPDATE IR;
   SELECT DR-Scan;
   LOAD the I_DD test patterns;
   CHECK the Shift-out Data;
   WHILE ( DONE = '0')
    {   UPDATE data registers;
        INCREMENT counter_clk_cycle BY 1;}
       RECORD counter_clk_cycle;}
DO PCS analysis
END of PSEUDOCODE;
```

Figure 10: Pseudo-code for Interconnect I_{DD} Testing

6. CONCLUSION

This paper presents a systematical bus/interconnect testing method incorporating I_{DDT} testing and Boundary Scan. A charge-based analysis methodology for I_{DDT} test reduces impacts due to process/power variations. A proposed enhanced Boundary Scan complies with 1149.1 IEEE Std. Two-pattern test vectors are generated inside BSCs to test iinterconnects. A feasible built-in transient current sensor illustrates the practicability and adaptability of this approach in today's popular CMOS technologies. A solution to minimize the A/D signal translation effort is also presented in the paper.

7. ACKNOWLEDGMENTS

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