One-chip Bluetooth ASIC Challenges

Paul T. M. van Zeijl
Ericsson Eurolab Netherlands
Nieuw Amsterdamsesstraat 40
PO Box 2015, 7801 CA Emmen
The Netherlands
Tel: +31 591 637 593

Paul.van.Zeijl@eln.ericsson.se

ABSTRACT

This paper will describe the constraints, trade-offs and challenges for designing a one-chip (RF/radio plus baseband integrated on the same Si-die) compared to designing a separate RF/radio ASIC.

The presentation will start with an overview of the background of Bluetooth technology: the orginal purpose was to replace wires. Consequently, the RF-proposal has to be cheap (target below U$5.-) and the current consumption should be low. The desire to have a cheap radio, cannot be implemented at all cost: the user will require a robust system (performance), otherwise the Bluetooth system will fail in the market. Nonetheless, a "simple, cheap radio" is still a complex analog system, and requires RF and analog design resources. An overview of "easy" and "difficult" Bluetooth radio specifications will be given to show the problem areas in radio design.

A single-chip radio module solution based on a BiCMOS radio-ASIC will be shown to demonstrate some particulars in integrating Bluetooth radio functionality.

From this single-chip radio module, additional functionality will be described for realising a one-chip Bluetooth solution: requirements on digital functionality, requirements coming from SW implemented in ROM or FLASH and additional radio requirements.

Next, different Si-processes (CMOS 0.36u, 0.25u, 0.18u and 0.13u, BiCMOS and SiGe) will be discussed wrt our target. Due to the large amount of digital, a CMOS process is the only possibility. CMOS scaling for the digital functionality will be discussed. The scaling of radio functionality for the most critical blocks will also be presented. This insight is needed to judge whether a future CMOS processes still allows the radio to be integrated and if we gain something from better CMOS processes. A bottleneck of f.i. a 0.18u CMOS process is the breakdown of approx. 2V, as the oxide thickness is 3.5 nm. This 2V may not be enough for realising the required radio performance. Fortunately, these 0.18u processes (and probably also the newer generations) also contain a thick oxide (usually around 7 nm) which have a higher breakdown voltage (3.3 - 3.6 V). Using the thin oxide devices, however, gives a higher f_T, and a higher capacitance density, which may result in lower current consumption or smaller silicon-area.

An important technical challenge in realising a one-chip solution is in solving the issue of cross-talk. Cross-talk is present on the PCB-level, packaging-level and on the silicon. The first two problems can be solved by proper PCB-design and proper choice of package. The Si-cross-talk problem depends on the type of substrate and the specific implementation of digital and analog blocks. Measurement results on a 0.36u CMOS test-chip with a low-ohmic substrate will be compared to simple model simulations. The situation on high-ohmic substrates or processes incorporating buried-layers is much more complicated. There are tools available for doing post-layout Si-cross-talk simulations, but these only facilitates checks after finalising the complete design. A new approach is needed: one that gives guidelines at the start of the project (or at least halfway the project) and helps in improving the design. Tools are required for helping designers minimising the Si-crosstalk problem. The problem can be attacked at the generation level (i.e. in the digital part of the chip), by minimising the transfer of interfering signals by proper choice of the substrate, and by taking measures at the circuitry where it is picked-up. This new approach for minimising the Si-cross-talk problem will be discussed extensively.

The presentation will be summarised with conclusions.

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