A Static Estimation Technique of Power Sensitivity in Logic Circuits

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ABSTRACT

In this paper, we study a new problem of statically estimating the power sensitivity of a given logic circuit with respect to the primary inputs. The power sensitivity defines the characteristics of power dissipation due to changes in state of primary inputs. Consequently, estimating the power sensitivity among the inputs is essential not only to measure the power consumption of the circuit efficiently but also to provide potential opportunities of redesigning the circuit for low power. In this context, we propose a fast and reliable static estimation technique for power sensitivity based on a new concept called *power equations*, which are then collectively transformed into a table called *power table*. Experimental data on MCNC benchmark examples show that the proposed technique is useful and effective in estimating power consumption. In summary, the relative error for the estimation of maximum power consumption is 9.4% with a huge speed-up in simulation.

1. INTRODUCTION

Optimization on power consumption in VLSI circuits has been actively studied for many years, and it is becoming more and more important due to the popularity of high density and high speed devices. Numerous papers have been published either on power estimation techniques or on synthesis techniques to generate low power designs. Most of the techniques have addressed one of the two issues, namely, how to estimate the power consumption of the circuits and how to minimize the power consumption by either synthesizing a new circuit or restructuring a pre-synthesized circuit targeting low power.

The paper addresses a novel technique which *statically* estimates the power sensitivity in a given logic circuit. The power sensitivity defines the characteristics of power dissipation due to changes in state of primary inputs. The power sensitivity analysis will generate the result which shows for which primary input, the circuit will be most sensitive in terms of switching activity, and collectively, for which input vector, the circuit will have the maximum amount of switching activities. The proposed static analysis technique is very useful in the two areas: (1) when we want to measure the maximum power consumption of a predesigned block, the technique enables us to estimate it without applying input vectors to the block exhaustively. Obviously, the static method has a huge advantage over any simulation-based method in terms of runtime. The key consideration is its accuracy. (2) It helps to build a low power system by making it possible to provide an interface logic which effectively reduces the switching activities in the overall system without resynthesizing the individual pre-designed IP blocks in the system.

Even though most of the previous works [1, 2, 3, 4, 5, 6, 7, 8, 9] have addressed the problem of estimating power consumption accurately and efficiently while understanding the fact that the power dissipation in a circuit strongly depends on the properties of primary input signals, none of them directly have addressed the problem of static analysis for estimating the power sensitivity of logic circuits.

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2. POWER SENSITIVITY: AN OVERVIEW

Suppose a circuit is technology mapped. We want to analyze the circuit to understand the power characterization. In this paper, we call the characterization *power sensitivity*. To achieve the goal we should analyze the circuit in two respects: (1) how certain states at the primary inputs maximize/minimize the amount of the propagation of unnecessary switching activity, and (2) which primary inputs influence the maximum amount of switching activities in the circuit. By using a measurement for (1) we can find how many gates are controlled by a (0/1) state of each primary input, from which the 'preferred' state for the input can be determined. On the other hand, by using a measurement for (2) we can tell which primary input should be considered the most important to minimize the switching activities in the circuit. Since the measurements for (1) and (2) are highly correlated, in our proposed technique for estimating power sensitivity, a single metric which reflects both (1) and (2) is formulated. The details of the metric is discussed in Sec. 3.

Suppose we are given the circuit shown in Figure 1. Our goal is to analyze the circuit in terms of the power characterization with respect to each primary input. The following enumerates several key observations of the circuit behavior and structure that will hint how the power characterization should be viewed and analyzed.

Controlling inputs: The circuit contains gates with controlling values (e.g., AND and OR) and also contains gates with

no controlling values (e.g., XOR). The existence of controlling values is very useful in reducing the switching activity in the circuit because it can be used to gate the signal propagation of the other inputs. Therefore, we need to pay more attention to the gates without controlling values since analyzing the switching activity in those gates with respect to their input values is not as simple as that of gates with controlling values.

# of fanouts: Primary input C is a support variable for more gates than primary input E, which means that the circuit would be potentially more sensitive to the state change in C than in E.

Inter-dependency between inputs: Primary input B is preferred being in '0' state for gate G1, but preferred being in '1' state for gate G3. This implies the preferred state for a certain primary input heavily depends on the structure of the given circuit. Furthermore, when B is in '0' state, it may be useful to gate any high switching activities in input C, but it may be bad for gate G2 because when B is '0', G1 becomes '0', and then any transitions in input A will be propagated through gate G2. This means that we have to have a global analysis scheme which considers all the transitive fanouts in the circuit.

Non-uniform contribution to fanout gates: Primary input C is a support variable for both G1 and G5. However, note that the probability of controlling the output state of gate G1 by C is much higher than for gate G5. For example, when C is '0', the output of the gate G1 becomes '0'. However, to control the output of G5 to '0', both of the inputs C and A should be '0'. Therefore, it is very important to compute the exact *contribution factor*[1] of each input for the gates in its transitive fanout.

Reconvergent fanouts: The circuit contains reconvergent fanouts like G5 or G8. Note that a support variable (a primary input) goes through different paths until the different paths meet at a reconvergent fanout. To minimize the switching activity at the reconvergent fanout, a certain support variable should be high (state '1') for one path or should be low (state '0') for the other(s), or the both states should be high (or low). Therefore, the technique for estimating power sensitivity of primary inputs should be able to analyze this accurately.

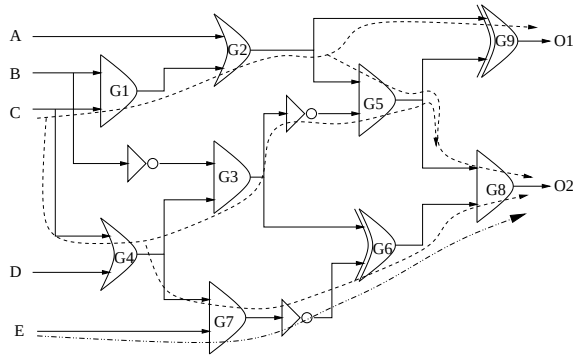


Figure 1: A circuit used to describe various factors related to power sensitivity.

[1]This will be defined formally in Sec. 3.3.

3. STATIC ANALYSIS FOR POWER SENSITIVITY

3.1 Power Sensitivity

The sensitivity of a circuit with respect to a set of vectors is a measure on how much the power consumption of the circuit will change according to the change of the on-probability of the input signal. We define the sensitivity of a circuit with respect to a set of vectors as follows: (For more detailed discussion, see [6].)

$$S_{P(x)} = \frac{1}{N}\sum_{i=1}^{N} \lim_{\Delta P(x_i)\to 0} \frac{\Delta Power}{\Delta P(x_i)}$$

where $P(x)$ denotes the set of on-probabilities of the signals $x = (x_1, x_2, \ldots, x_N)$, and $P(x_i)$ denotes the on-probability of the i-th input signal, and $Power$ denotes the average power dissipation of the circuit.

For some input, frequent state transitions in the signal lines will result in significant increase in total power dissipation. By analyzing the sensitivity of each input signal, we want to determine (1) the set of primary inputs on which the power consumption of the circuit heavily depends, and (2) the set of states of primary inputs which will minimize the propagation of the switching activities in the circuit.

Then, by using the results obtained by the analysis, we can determine a set of the preferred vectors, which should appear more frequently to minimize the power dissipation. At the same time, we can also identify a set of vectors which will generate the maximum amount of switching activities, which likely lead to the maximum power consumption. Our proposed technique for such a static analysis of power sensitivity is based a concept called *power equation*.

3.2 Power Equation

The input circuit may consist of logic gates of different types and of different fanins and fanouts. Consequently, we need to address how the power equation is computed for different gates in the target library. We illustrate the concept by presenting simple cases. Then, more formal discussions will follow.

Suppose we have a 2-input AND gate. The switching activity of a 2-input AND is computed by $SW_{AND} = (1 - P_A P_B)P_A P_B$ where A and B are the two inputs to the AND gate and P_A and P_B are the on-probabilities of A and B, respectively. It clearly shows that when either P_A or P_B is close to 0 the power consumption is minimized and the power consumption does not increase sharply with the change of either P_A or P_B. It is important to realize that when both P_A and P_B are close to 1, power consumption is also very low. However, we can observe that the power consumption increases very sharply with the change of the on-probabilities of the inputs. Therefore, in case of an AND gate, the region where P_A and P_B are close to 0 is our preferred region. Hence, $(A, B) = (0, -)$ and $(A, B) = (-, 0)$ are the preferred vectors where '-' means a don't care. The *polarity* of each signal which constitutes the preferred vector is called *preferred polarity*. Similarly, we can find that the preferred vectors for a 2-input OR is $(A, B) = (1, -)$ and $(A, B) = (-, 1)$. That is, for an OR gate, P_A being close to 1 and P_B being close to 1 will be the preferred polarity for A and B, respectively.

However, for an XOR gate, the switching activity is given by $SW_{XOR} = [1-(P_A+P_B-2P_AP_B)](P_A+P_B-2P_AP_B)$. It is not trivial to determine the preferred vector because everything is totally symmetric. This means that a different way of analyzing the signal sensitivity should be used because we cannot find any preferred region. To do this, we propose a new analysis technique based on a novel concept called *power equation*, which not only takes into account the gates with controlling values but also the gates with no controlling values.

Definition 1 (Power Equation) *The power equation is a Boolean equation written in terms of the primary input variables and defined for each gate in the circuit. The power equation of a gate specifies a condition which should be true in order for the switching activity of the gate to be minimized. The power equation is used to compute the set of preferred polarity of the primary input signals.*

We now explain how the power equations of gates are derived by using the examples shown below.

• *Power Equation for AND/NAND*: For an N-input AND (or NAND) gate, the power equation is $\bigvee_i^N(\sim I_i)$ where I_i is the i-th input to the AND (or NAND) gate. It is clear that the power equation tells us that when at least one input is 0 (i.e., low) the switching activity is minimal in the AND (or NAND) gate.

• *Power equation for OR/NOR*: Based on a similar discussion for AND, for an N-input OR (or NOR) gate, the power equation is $\bigvee_i^N I_i$ where I_i is the i-th input to the OR (or NOR) gate. When N (atomic) variables are ORed (i.e., disjunction), the switching activity of the gate will be reduced if the maxterm is true.

• *Power equation for XOR/XNOR*: The power equations for AND and OR can be obtained very easily because they have controlling values. For gates which do not have such controlling values, for example, an XOR gate, we observe that the only way to reduce the switching activity is to have minimal switching activities in *all* the inputs. So, instead of deriving a condition under which the switching at the output of the gate is minimal, we compute a power equation which minimizes the switching activity in *all* inputs. This leads to the power equation for an N-input XOR which is $\prod_{i=1}^N PE(I_i)$ where $PE(I_i)$ is the power equation of the i-th input signal.

• *Power equations for primary inputs and inverters*: For primary input A, the power equation is $A+(\sim A)$. That means we do not have any preference on the state probability of each primary input. This is also true for inverters.

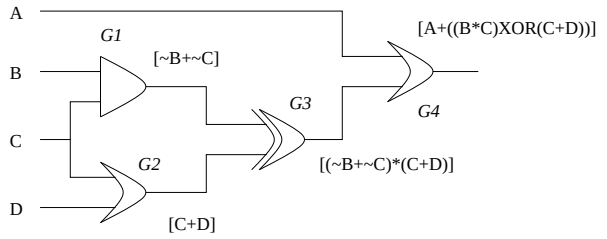


Figure 2: An example of generating power equations for gates.

Using the power equations for gates, we can obtain the power equation for each output of gates in the circuit. Consequently, it requires a linear-time effort to compute the power equations for all gates in the circuit. Figure 2 shows an example of generating the power equations of the gates in a circuit. For example, the power equation of gate *G3* is the product of the "power equations" of its two inputs, i.e., $[\sim B+\sim C]$ and $[C+D]$ because *G3* is an XOR gate whereas the power equation of *G4* is a disjunction of the "Boolean (logical) equations" for its two input signals, i.e., A and $(B*C)XOR(C+D)$ because *G4* is an OR gate.

Note that the power equations are replicative Boolean equations which represent a condition under which the equation should be true to reduce the switching at the gates and are written in terms of the primary inputs. They are replicative in the sense that the power equation for a gate at an earlier stage near the primary inputs will repeatedly appear in the power equations for the gates in its transitive fanout. Since it's a replicative set of Boolean equations, the computation done at each gate can be seen by the power equation. Therefore, multiple fanouts and reconvergent fanouts are considered because those signals will appear more than once in the transitive fanouts of the gate.

Once we obtain the power equation for each gate in the circuit, we need to evaluate all the power equations in order to determine the preferred polarity of each primary input signal. We employ a heuristic based on a probabilistic argument to evaluate the power equation for each gate. The intuition behind it is that the total power consumption of a circuit is approximately the sum of the power consumption at the gates and the interconnections. Therefore, we want to employ a heuristic which takes both into consideration. The evaluation is performed by inventing a table called *power table*, which is a collective (probabilistic) representation of the power equations for the gates.

3.3 Power Table

In this section, we present a set of rules for the evaluation of the power equations. Before discussing our heuristic in detail, we want to introduce a term *contribution factor*.

Definition 2 (Contribution Factor) *The contribution factor is the probabilistic contribution of a certain state of a primary input when the primary input appears in the power equation of the gate.*

The reason of the introduction of the contribution factor is to calculate how important for a certain input to have a certain state. For example, an output state of '0' in a 2-input AND gate, implies that at least one out of the 2 inputs should be '0'. Similarly, an output state of '0' in a 3-input AND gate implies that at least one among the 3 inputs should be '0'. One thing that can be clearly seen is when there are more inputs to the gate, it becomes less important for *each* input to have a certain state. A formal discussion on computing the contribution factor is given in Sec. 3.3.1.

Definition 3 (Power Table) *The power table is an $N \times 2$ table where N is the number of primary inputs. For the i-th variable, the table entry in the i-th row and the j-th (j being either 0 or 1) column is a real number which measures the merit if the i-th variable is low (i.e., $j = 0$) or high (i.e., $j = 1$). In other words, it measures the effectiveness of choosing a certain polarity to reduce the switching activities*

in the circuit. We use the notation $PT[i][j]$ to refer to the entry in the i-th row and the j-th column of power table PT. In fact, each entry is a sum of probabilities which represent how likely that a certain polarity of the i-th variable will reduce the switching activity of the circuit.

3.3.1 Evaluation of Power Equations

We employ the following rules to evaluate the power equations. It is very important to note that power equation is *very inexpensive* to evaluate since we are computing neither the *ON*-set nor the on-probability of the gates. Furthermore, the evaluation does not become much more costly as the number of inputs of gates is getting larger. Remember these rules are used to evaluate the power equation when the corresponding Boolean operation appears in the power equation, and are not directly related to the type of the gate for which the power equation is defined.

AND Rule: If N (atomic) variables are ANDed (i.e., conjunction) in the power equation of a gate, the switching activity in the gate will be reduced if the product becomes true. Since the probability for the product to be true is $\frac{1}{2^N}$ when we assume that all the variables are equally probable to be high or low, the contribution factor of each variable will be $\frac{1}{2^N}$. For example, suppose there is a gate whose power equation is $[\sim A * B]$. Then, we add $\frac{1}{4}$ to the power table entries[2] $A[0]$ and $B[1]$. In general, A or B may be a parenthesized clause. Then we recursively calculate the contribution factors for the clauses. For example, for the power equation, $[A * (B * C)]$, add a contribution factor $\frac{1}{4}$ to $A[1]$, and a contribution factor $\frac{1}{4} \times \frac{1}{4}$ to $B[1]$ and $C[1]$.

OR Rule: If N (atomic) variables are ORed (i.e., disjunction) in the power equation of a gate, the switching activity in the gate will be reduced if any input among the N inputs is true. Since the probability for the equation to be true is $1 - \frac{1}{2^N}$ when we assume that all the inputs are equally probable to be high or low and there are N inputs, the contribution factor for each input is $\frac{1}{N} \times (1 - \frac{1}{2^N})$. For example, suppose there is an OR gate the power equation of which is $[\sim A + B]$. Then, we add $\frac{1}{2} \times (1 - \frac{1}{4})$ in the power table entries $A[0]$ and $B[1]$. Note that $(1 - \frac{1}{2^N})$ is the probability of an N-input OR gate being TRUE when every input has on-probability of 0.5. In general, A or B may not be a atomic variable. Then we recursively calculate the contribution factors for the clauses. For example, for power equation, $[A * (B + C + \sim D)]$, add a contribution factor $\frac{1}{4}$ to $A[1]$, and a contribution factor $\frac{1}{4} \times (\frac{1}{3} \times (1 - \frac{1}{2^3}))$ to $B[1]$, $C[1]$ and D[0].

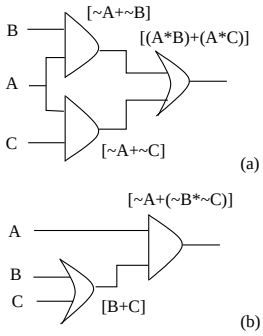
It should be noted that the evaluation of contribution factors for all the power equations of the gates can be done very fast and is much cheaper than logic evaluation because the evaluation of power equation involves only the propagation of the contribution factors at each gate until the propagation ends at the primary inputs.

3.3.2 Construction of Power Table

After evaluating the power equations for gates, we construct a power table for the entire circuit. From the table, we can observe (a) the magnitude of the total contribution factor for each state of each primary input and (b) *relative merit* for a certain input signal to be high or low. Clearly, when the magnitude is large there are many gates which are dependent on the corresponding state of the primary input. Therefore, it is safe to say that the circuit is sensitive to the state of the primary input. On the other hand, the relative merit of the i-th signal being 1 (0) in power table PT is $\frac{PT[i][1(0)]}{PT[i][0]+PT[i][1]}$. Having a relative merit which is much bigger than 0.5 implies that the corresponding state is strongly preferred over the other. We select the preferred polarity for each input based on the relative merit.

A large portion of power consumed in a circuit is mainly due to two reasons: (1) Some primary inputs have lots of switching activities; (2) Some primary inputs cause many spurious transitions to be propagated throughout the circuit. For (1), the closer to 0.5 the on-probability of a primary input is, the more the switching activities will take place. For (2), the more the state probability of being in the *non-controlling* state becomes, the more switching propagation will take place. Consequently, by exploiting both the magnitudes and the relative merits of the primary input in the power table, we can take the two reasons into consideration.

Figure 3 shows two power tables corresponding to two functionally equivalent, but structurally different circuit implementations. Each gate is labeled with the corresponding power equation. We can easily see that the summary in the corresponding power table indicates what the set of preferred polarity is. In case of (a), (A,B,C)=(0,0,0) is the best vector, and in case of (b), (A,B,C)=(0,1,1) is the best vector. This example clearly shows the dependency between the circuit structure and the set of preferred polarity.



	L(0)	H(1)	
A	3/8+3/8	3/32+3/32	L > H
B	3/8	3/32	L > H
C	3/8	3/32	L > H

	L(0)	H(1)	
A	3/8	-	L > H
B	3/32	3/8	L < H
C	3/32	3/8	L < H

Figure 3: An example of the analysis based on power equation and power table.

3.3.3 Estimation of Power Sensitivity based on Power Table

The power table indicates which primary inputs(s) is relatively more important and the preferred polarity of each input. Therefore, to measure the maximum power consumption, a set of input vectors which does not conform to the table should be applied since the values in the entries of power table is a "collective representation" of the power equations. Letting all the power equations, by our definition, be true directly means a minimal power consumption. In this section, we address how to compute the power sensitivity based on the power table. Suppose a circuit has a set of input vectors V and the corresponding inputs' on-probabilities are represented by a vector $P = (p_0, p_1, \ldots, p_{n-1})$. Let

[2]We use notations $X[0]$ and $X[1]$ to indicate $PT[X][0]$ and $PT[X][1]$, respectively, when X is the i-th variable in power table PT.

$S_i = PT[i][1] + PT[i][0]$ and $R_i = \frac{PT[i][1]}{S_i}$. S_i represents the total magnitude of power table entries for the i-th input, and R_i is the relative merit of being '1' for input i. Note that the sum of the merit is a good indicator whether a set of input vectors is a good set of vectors in terms of the power consumption. Then, we estimate the power sensitivity for an input vector using the formulation:

$$PowerSense(V) = \sum_{\forall input\ i} (c_1 \cdot S_i \cdot |p_i - 0.5| + c_2 \cdot (\frac{1}{|R_i - p_i| + 1}))$$

where c_1 and c_2 are user-defined constants to balance the important of the two terms. The first term represents that the on-probability of input i should be far from 0.5 to minimize the generation of switching activities, and the second term represents that the on-probability should conform to the relative merit in order to minimize the switching activities in the circuit. For example, when $R_i = 0.2$, it implies that $PT[1] << PT[0]$. So p_i should be low to produce a minimal power consumption.[3] It is easy to see that to minimize (maximize) the power sensitivity, the *PowerSense* should be maximized (minimized).

4. EXPERIMENTAL RESULTS

Experiments are performed to check the efficiency of estimating the maximum/minimum power consumption of the circuit by using our technique. All the programs are implemented in C++, and are executed on a Sun Sparc10 workstation. We used a set of MCNC benchmark circuits in the experiments. The power measurement was conducted using the power estimation tool in SIS 1.2 assuming a 20MHz clock and 5V. The power consumptions were computed after the technology mapping using `mcnc.genlib`.

Table 1: Comparison of max. power consumption.

Circuit	gate area	EXHAUSTIVE power(μW)	OURS power(μW)	relative error(%)
c8	496	1240.9	1161.7	6.2
b1	23	44.4	41.6	6.3
cht	501	1682	1541.0	8.4
cm42a	47	126.2	117.3	7.05
cm82a	38	125.3	111.3	11.2
cm85a	78	175	154.1	11.9
cm138a	45	112	93.2	16.7
cm151a	65	200.06	186.7	6.7
cm152a	46	167	138	17.5
cm162a	105	280.3	267.9	4.4
cm163a	98	246.1	219.9	10.6
cmb	92	231.3	195.3	15.5
count	253	567.8	495.5	12.7
cu	118	324.1	298.0	8.0
majority	26	56.7	54.3	4.2
comp	252	664.3	641.6	3.4
pm1	113	310	278	10.1
sct	298	926	866.1	6.5
tcon	64	149	130.4	12.4
x2	102	284.8	259.2	8.9
average				**9.4**

[3]Constant 1 is added for normalization.

For a given circuit we generate a random set of occurrence probability. For each gate in the initial circuit, we compute the power equation, from which the power table is constructed. To demonstrate the accuracy of the analysis, we compute the permutations of on-probabilities which are the best in terms of the power table. We measure the power consumptions for the best sets of on-probabilities. In addition, we applied a large number of permutations of the on-probabilities, one by one, and took the exact maximum power consumption, which is then compared with ours.

Table 1 summarizes the results. The third and fourth columns show the maximum power consumptions of circuits for the permutation determined by the exhaustive search and power table, respectively. In comparison, our estimation based on the power table is within the relative error of 9.4% for the maximum minimum power consumption, while achieving several hundred times speed-up in simulation.

5. CONCLUSIONS

In this paper, we proposed a new technique which statically estimate the power sensitivity of a circuit. A novel notion of *power equation* was introduced, and we illustrated how the concept is extended to estimate the power sensitivity statically. Experimental results showed that the proposed method is accurate and efficient in estimating the maximum power consumption of circuits, and also will be useful to save the power consumption by utilizing it to convert the input vectors for low power. Finally, it should be noted that there are ample opportunities to extend the scope of the utilization of the proposed technique when it is combined with other traditional approaches to the power estimation and synthesis for low power.

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