A Novel Method for Stochastic Nonlinearity Analysis of a CMOS Pipeline ADC

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ABSTRACT

An analytic approach is presented for estimating the non-linearity of an analog to digital converter (ADC) as a function of the variations in the circuit devices. The approach is demonstrated for the case of a pipeline ADC with digital error correction. Under some mild assumptions on the expected variations, the error probability is expressed as a simple explicit function of the standard deviations in the components' parameters: gain errors, comparator offset errors and resistor errors. The analytical expression is verified for Integral Non Linearity (INL), and its limits are studied using Monte-Carlo simulations of a 10 bit pipeline ADC structure.

1. INTRODUCTION

Analog to digital converter (ADC) is typically characterized by its resolution (number of bits), sampling frequency, power dissipation and its linearity parameters such as integral nonlinearity (INL) and differential nonlinearity (DNL). The linearity parameters are determined by the analog errors in various ADC components. A major challenge in ADC design is therefore to estimate the contribution of those individual errors to the overall ADC linearity parameters. Such a statistical estimation is important in order to find the more critical sources of error and design accordingly, thus avoiding over-design and improving resource allocation in the design process. This estimation can be achieved by time consuming Monte-Carlo simulations of the whole ADC structure in which the parameters of various components are drawn according to process variations and other error sources. However, analytic expressions for the various linearity parameters lead to a better insight into the main error mechanisms and speed up the design process.

Several methods have been proposed for calculating linearity parameters in various cases. A general method was presented [7] for yield calculation due to process variation, based on extensive Monte-Carlo simulations. Expressions have been derived [4] for the error in current steering DAC as a function of device mismatch. Error models have also been presented [2] for various ADC architectures: integrating, successive approximation and flash, based on polynomial expansion of nonlinearity parameters, fitted to experimental data. Several expressions were derived [10] for the dependence of the effective number of bits on individual component variations for the case of a flash ADC. High-level expressions are derived in [4] based on sensitivity analysis of the low-level components, obtained from extensive simulations. Another general approach, presented in [5] and [6], is to use a variance-covariance matrix to represent the nonlinearity parameters and their correlations, fitted to experimental data. In this paper we develop a simple analytical expression which describes the distribution of the integral nonlinearity error of a whole pipeline ADC as a function of the statistical errors in its components. Due to its simplicity, our approach may be a useful analysis tool in the ADC designer's toolbox.

Roughly speaking, our method works as follows. Based on a behavioral model of an ADC system, we first *identify* the possible sources of error, then *partition* and sum them up into groups with minimal statistical dependence, and finally *analyze* the contribution of each group to the total linearity error. This procedure can be repeated in course of the design process, taking advantage of the knowledge accumulated about the error magnitude in each group. In this paper we demonstrate the method for an N bit pipeline ADC architecture. This architecture (for $N = 10$) is sketched in Fig. 1, where each stage produces two bitlines (using a three output codes sub-ADC), subtracts this value from its input (using a Digital-to-Analog Converter (DAC)), and amplifies the resulting analog residue by two. The $2x$ gain is usually provided by a switched capacitor amplifier, which also provides the sample-and-hold (=analog latch) between the stages, therefore allowing concurrent processing. The code redundancy is used for digital error correction, in which the resulting 18 bitlines are combined by an error correcting logic (usually a synchronized adder) to yield 10 bits at the output of the ADC. This architecture has been shown to achieve high throughput at low power (e.g. [1], [9]). The digital error correction relaxes the constraints on comparator offset voltages considerably, but does not correct gain er-
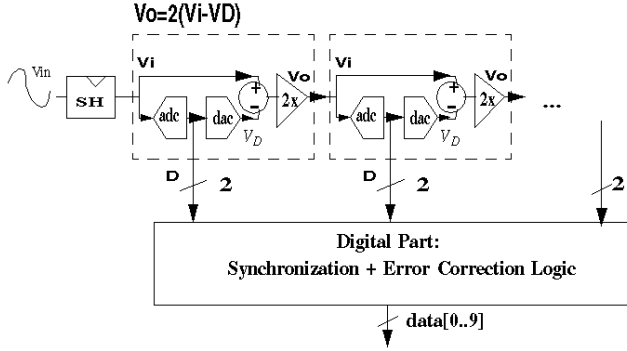
Figure 1: Pipeline architecture for a 10 bit ADC. Each stage produces two bitlines representing a digital code from $\{0, 1, 2\}$. The data redundancy is used for digital error-correction.

rors and internal DAC reference errors, as will be discussed in the sequel. The effect of this error correction is included both in our Monte-Carlo simulations and in the analytical stochastic model given below.

The paper is structured as follows. In section 2 we discuss the pipeline structure, including the error correction circuit, and calculate the distribution of the INL, given the standard deviations in the components' errors. Then in section 3 we present the Monte-Carlo simulations that were performed to verify the claims of the analytical stochastic study.

2. STOCHASTIC ERROR ANALYSIS

In this section we develop an analytical expression for the distribution of the INL error and the average INL value, as function of the errors in the ADC components. In order to enable analytical stochastic calculation of this nonlinearity, a few assumptions must be made about the ADC system and its operating conditions.

2.1 Basic assumptions

The first fundamental assumption is that the system allows for a *small error analysis*, meaning that the overall error of the ADC, referred to its input, is within the limits of a single LSB unit. This assumption is justified by the fact that several commercially available CMOS pipeline ADC's are capable of maximal INL and DNL values which are less than one LSB. Under small error conditions the ADC can be regarded as an approximately linear system, allowing for a superposition of the errors. Small error analysis is therefore similar to small signal analysis, which regards a non linear system as linear one under small signal conditions around a given operating point.

The second assumption of our calculation is that the sources of error in the ADC can be divided into a small number of groups such that the total contribution of each group can be approximated by a Gaussian distribution, centered at the nominal value, whose standard deviation represents the group (as in [5] and [6]). In the specific derivation presented below for INL we also assume that the groups are statistically independent, but this assumption can be relaxed in the general case, as will be explained in section 2.6 below. Within each group the errors can generally be statistically dependent, and we shall treat this dependency by dividing

the error into correlated and uncorrelated parts, and performing a different calculation for each part. for the case of a pipeline ADC, we define the following three error groups.

1. Comparator offset voltage errors (σ_{V_C}) in the flash ADC of each stage

2. Errors in the internal reference voltages (σ_{V_R})

3. Gain errors (σ_G) in the amplifier of each stage.

Since the errors in different groups are mainly determined by different physical mechanisms, it is reasonable to assume, as a first approximation, that the groups are statistically independent. Note that the choice of the groups affects the details of the calculation, but not the basic methodology. Each of the three types of errors defined above is the combined result of two physical effects: *noise*, which includes charge injection noise in analog switches, thermal noise, shot noise, flicker noise, and noise coupled from digital circuitry (via crosstalk or substrate), and technology *parameter variation*, e.g. device mismatch. Noise can cause the same die to behave differently even if the same inputs are applied, while process variations cause different dies to have different behavior. The error coefficients $\sigma_{V_C}, \sigma_{V_R}$ and σ_G are calculated either by direct Monte-Carlo simulations of the corresponding building blocks, or, in case of a large building block, by dividing the block into smaller sub-blocks and recursively applying the same approach.

2.2 The INL and its distribution

In Fig. 2 (a) we see a typical transfer curve of an ADC converter which shows the output code as a function of the input continuous analog value. Two transfer curves are shown: The first is an ideal transfer curve which describes an ADC with no errors. The second curve is an actual transfer curve of the investigated ADC. The equivalent error at the ADC input is given by the following Gaussian distribution:

$$f_X(x) = \frac{e^{-(x-\mu)^2/(2\sigma^2)}}{\sqrt{2\pi\sigma^2}}, \qquad (1)$$

where the variable x measures the horizontal shift between the actual and the ideal transfer curves for a specific code. The single most important parameter for this analysis in the distribution given by Eq. 1 is the statistical deviation σ.

2.3 Pipeline stage and error groups

We first look at a simplified, one-bit-per-stage pipeline structure without error correction, which contains N identical stages of the kind sketched in Fig. 3. The comparator (*comp*) is the internal one bit sub-ADC of this stage. The two resistors R and the switch $SW1$ form an internal one bit DAC. When the clock is low, the analog switch $SW2$ is connected to the input voltage V_i and the analog switch $SW3$ is shorted. At this condition the input capacitor $2C$ samples the input voltage. When the clock is high again, the analog switch $SW3$ is opened and $SW2$ is connected to the DAC reference voltage V_D. This last action transfers the charge $2C(V_i - V_D)$ from the capacitor $2C$ directly to the capacitor C, which gives a $2X$ amplified analog output $V_o = 2(V_i - V_D)$. Labeled in Fig. 3 are the three error groups as they appear in this stage. The comparator offset (σ_{V_C}) group is marked at the input to the comparator block and includes offset caused by either component mismatch,
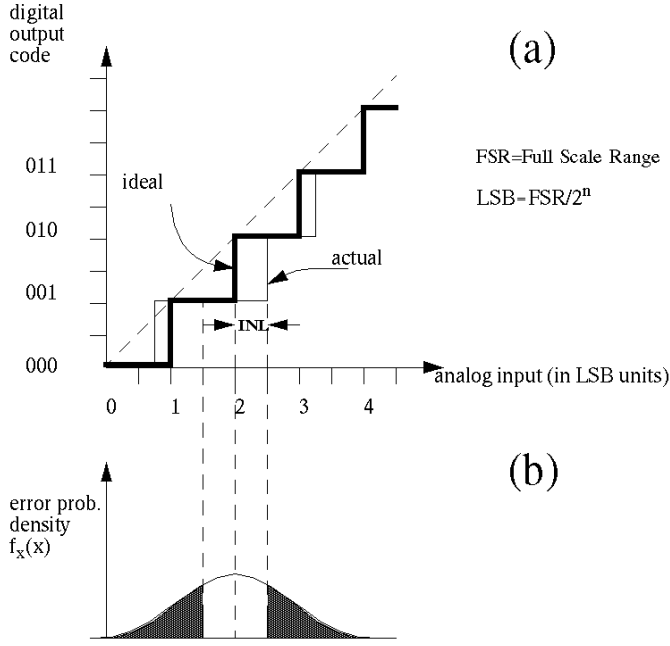
Figure 2: A typical transfer curve of an ADC converter, showing the INL as a horizontal deviation of code transition (a), and the error probability distribution function, highlighted in gray (b).
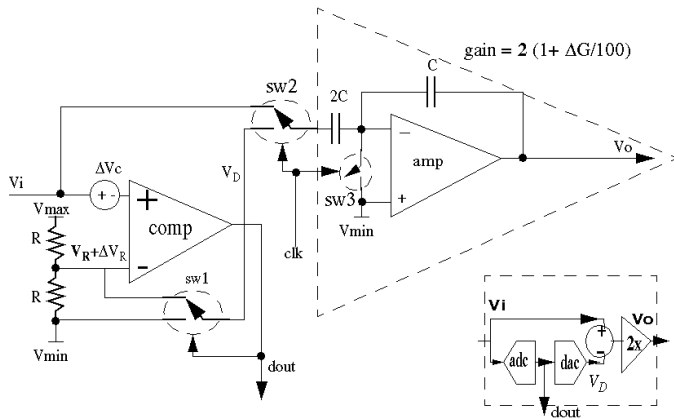

Figure 3: A simplified circuit of a stage in a one-bit-per-stage pipeline.

self heating effects, hysteresis or noise. The second error group includes reference voltage (σ_{V_R}) errors caused by resistor ladder variations and noise, as well as to errors in the switch $SW1$ which are mainly due to charge injection in the CMOS transmission gate. This second error group has a double effect: It affects the reference voltage for the comparator marked as V_R and the reference voltage for the $2X$ amplifier marked as V_D. The third error group includes all the errors of the switched capacitor amplifying circuit, including technology variations in the $2C/C$ capacitor ratio, thermal KT/C noise, charge injection in $SW2$ and $SW3$, finite gain and offset of the operational amplifier (amp).

2.4 Error paths

In order to be able to interpret the ADC as a linear system, let us connect (conceptually) in parallel to the two inputs of each of the N comparators of the pipeline ADC an ideal linear differential amplifier with a unity gain and a non zero offset, which is equal to the offset of the corresponding actual comparator connected in parallel. This additional differential amplifier will serve as a conceptual analog error probing device. The output of such an ideal amplifier in volts is always equal to the voltage difference between its two inputs minus the offset voltage. The total system with one analog input of the ADC and N analog outputs of the probing amplifiers, is a linear system if the analog input value to the ADC corresponds to a central point in an output code in the ideal transfer curve shown in Fig. 2 , and the overall error of the ADC equivalent to its input is less than 0.5 LSB. This last condition is equivalent to the condition that the output code is correct for this analog input voltage. Around this operating point, small error analysis can be applied in order to calculate the statistical linearity parameters of the pipeline ADC. This is the exact meaning of the above defined "small error condition". Let us proceed by choosing at random only one of the output bits of the ADC, denoted as the ith bit ($1 \leq i \leq N$). We assume that the analog input value corresponds to a central point in a valid output code in the ideal transfer curve shown in Fig. 2, and that the small error condition prevails. We now regard the analog input of the ADC and the output of the probing amplifier of the ith stage as the input and output of a simple linear equivalent amplifier, which will be termed the "ith equivalent amplifier". If the ADC has errors, then the output of this ith equivalent amplifier deviates from the definite value of this output at zero errors. The deviation in the output of the ith equivalent amplifier is a measure of the overall error of the ADC on the path from the input to the ith output. In general there are N *error paths* of this kind in the ADC. To calculate the overall error of the i path, we consider it as caused by noise, and calculate the equivalent of ith error path at the input of the ADC, in the same way used to calculate the equivalent noise source at the input of a conventional noisy linear amplifier. First we calculate the contribution of each of the three error groups to the overall error, and then add these contributions, based on our assumption that the groups are statistically independent.

2.5 Error groups

2.5.1 Comparator offset error group

On the error path from the analog input to the ith bit output, there is only one comparator at the ith stage. If the

standard deviation in the offset error of this comparator is a σ_{V_C}, then the resulting standard deviation of the equivalent error at the input of the ith equivalent amplifier, E_c^i is given by Eq. 2 :

$$E_c^i = \frac{\sigma_{V_C}}{2^{i-1}} \tag{2}$$

This result follows since the analog gain along the ith error path is 2^{i-1}.

2.5.2 Reference voltage error group

On the ith error path the relevant influence of the reference voltage error is as DAC reference errors (V_D) in stages $1, 2, \ldots, i-1$, and as comparator reference error (V_R) in the ith stage.

Each stage amplifies the previous DAC reference error by two, and then adds its own error. This process leads to an arithmetic-geometric series which gives e_i, the standard deviation in the analog output (V_o in Fig. 3) of the ith stage as a function of the DAC reference voltage error σ_{V_D}:

$$\begin{aligned}
e_1 &= 2\sigma_{V_D} \\
e_2 &= 2e_1 + 2\sigma_{V_D} = 3e_1 \\
e_3 &= 2e_2 + e_1 = 7e_1 \\
&\vdots \\
e_{i-1} &= e_1(2^{i-1} - 1) = 2\sigma_{V_D}(2^{i-1} - 1).
\end{aligned}$$

This simple addition of standard deviations is possible because the reference voltage errors come from the same source and are therefore fully correlated. By adding the comparator reference error σ_{V_R} in the ith stage, we further get the equivalent error at the input

$$E_R^i = \frac{2\sigma_{V_D}(2^{i-1} - 1) + \sigma_{V_R}}{2^{i-1}} \approx 2(1 - 2^{-i})\sigma_{V_R}, \tag{3}$$

assuming that $\sigma_{V_D} \approx \sigma_{V_R}$.

2.5.3 Gain error group

Here we have to distinguish between correlated and uncorrelated errors. A *consistent* technology variation across the chip may result in a consistent error in the gains of all stages, while *random* variations lead to statistically independent gain errors. Since both cases are possible we perform the two calculations, thus enabling the calculation of the "mixed" correlated-uncorrelated case. An important feature of the gain error in both cases is that its magnitude depends on the output digital code of the ADC. We start by the calculation of the fully correlated case, which is also the worst case for overall gain error. In terms of a single pipeline stage, the maximal error at the analog output V_o (see Fig. 3) is obtained when the analog output of the stage approaches its maximal voltage value, V_{max}, since the gain amplifies the input signal V_i to yield the output analog signal V_o. The overall maximal gain error is obtained for the ADC output codes $(111\ldots1)$ or $(011\ldots1)$, in which the analog output of all stages is maximal. As before, let us denote by e_i the error in the ith analog output (V_o in Fig. 3). e_1 is the error in the analog output of the first pipeline stage, which is equal to $2^N \sigma_G/100$ (in LSB units), where σ_G is the gain error in percents, provided that the analog output of this first stage V_o is approaching V_{max}. The following error e_2 is obtained by multiplying the previous error by the gain of two and adding the error of the second stage amplifier, which is

also assumed to have its worst case value corresponding to a maximal analog output. This leads again to an arithmetic-geometric series for the fully correlated accumulating gain errors, as expressed by Eq. 4:

$$\begin{aligned}
e_1 &= 2^N \frac{\sigma_G}{100} \\
e_2 &= 2e_1 + e_1 \\
e_3 &= 2e_2 + e_1 \\
&\vdots \\
e_{i-1} &= 2^N \frac{\sigma_G}{100}(2^{i-1} - 1).
\end{aligned} \tag{4}$$

Hence the input equivalent of the overall error in the i error path due to fully correlated gain errors, denoted by E_{CG}^i, is given by

$$E_{CG}^i = 2^N \frac{\sigma_G}{100}(1 - 2^{1-i}). \tag{5}$$

Let us now turn to the case of statistically independent gain errors along the i error path. Analytical calculation of the accumulating error becomes possible in this case since independent errors sum up in their variances, which means that the independent gain standard deviations sum up in their average squares. Let $e_1^2 = (2^N \sigma_G/100)^2$ denote the average square of the gain error in the analog output of the first pipeline stage in the worst case condition, where σ_G is the variance of the gain error of a stage in percentage units. The following error e_2^2 is obtained by multiplying the previous error by the square of the nominal gain which is equal to four, and then adding the new average square error of the second stage amplifier, which is also assumed to have its worst case value corresponding to a maximal analog output. This procedure leads again to an arithmetic-geometric series for the accumulating gain errors, but with different coefficients. The elements of this new series are:

$$\begin{aligned}
e_1^2 &= \left(2^N \frac{\sigma_G}{100}\right)^2 = \mathrm{VAR}(V_o^1) \\
e_2^2 &= 4e_1 + e_1^2 \\
e_3^2 &= 2e_2 + e_1^2 \\
&\vdots \\
e_{i-1}^2 &= 4e_{i-2}^2 + e_1^2,
\end{aligned}$$

Thus the statistical variance of the error at the end of the ith error path for statistically independent gains is given by

$$e_{i-1}^2 = \left(2^N \frac{\sigma_G}{100}\right)^2 \frac{1}{3}(4^{i-1} - 1). \tag{6}$$

The overall error in the ith error path due to fully independent gain errors, whose input equivalent is denoted by E_{IG}^i, is therefore given by

$$E_{IG}^i = 2^N \frac{\sigma_G}{100} \frac{1}{\sqrt{3}} \frac{\sqrt{4^{i-1} - 1}}{2^{i-1}}. \tag{7}$$

The total equivalent standard deviation at the input of the ith error path can now be expressed, due to the indepen-

dence of error groups, as:

$$\sigma^2 = (2(1 - 2^{-i})\sigma_{V_R})^2 +$$
$$\left(2^N(1 - 2^{1-i}) \cdot \frac{\sigma_G}{100}\right)^2 + \left(\frac{\sigma_{V_c}}{2^{i-1}}\right)^2$$

for correlated gain errors, and

$$\sigma^2 = (2(1 - 2^{-i})\sigma_{V_R})^2 +$$
$$\left(2^N \frac{4^{i-1} - 1}{3(2^{i-1})^2} \cdot \frac{\sigma_G}{100}\right)^2 + \left(\frac{\sigma_{V_c}}{2^{i-1}}\right)^2$$

for independent gain errors. $\qquad$ (8)

2.6 Average INL calculation

In order to calculate the expected INL of the ADC we have to consider the errors in all the error paths. The situation is considerably simplified by the presence of the given error correction mechanism (Fig. 1 and references [1],[9]). This 1.5 bits per stage structure is different from the 1 bit per stage architecture in a few aspects: there are three (rather than two) resistors in the ladder, there are two comparators (rather than one) in each stage, and - most importantly - an error correction mechanism exists which significantly reduces the number of error paths that should be considered in our analysis, as explained below. The first two differences have a minor influence since σ_{V_C}, σ_{V_R} and σ_G can be easily modified to take the extra components into account.

The error correction logic enables the ADC to tolerate much larger offset errors in the comparators of all stages except the Nth stage, before an error appears in the ADC output. This larger tolerance to comparator offset errors is possible due to the many-to-one mapping of 18 bitlines (from the 9 pipeline stages) into a 10 bit output. However, error correction logic does not correct the accumulated analog errors from stage to stage, such as gain errors. The error correction logic is efficient as long as the equivalent error at the input of the Nth error path is less than 0.5 LSB, which means that the analog signal passing through all stages is still correct. The standard deviation σ of the overall equivalent error at the ADC input in the worst case code (Eq. 1) is therefore obtained by substituting $i = N \gg 1$ in Eq. 8 :

$$\sigma^2 = (2\sigma_{V_R})^2 + \left(2^N \cdot \frac{\sigma_G}{100}\right)^2 + \left(\frac{\sigma_{V_c}}{2^{N-1}}\right)^2$$

for correlated gain errors, and

$$\sigma^2 = (2\sigma_{V_R})^2 + \frac{1}{3}\left(2^N \cdot \frac{\sigma_G}{100}\right)^2 + \left(\frac{\sigma_{V_c}}{2^{N-1}}\right)^2$$

for independent gain errors. $\qquad$ (9)

Note that the above compact result was made possible due to the error correction, which eliminates the influence of all error paths except the last.

We now calculate the expected value of the integral non-linearity (INL). The expected value of the absolute deviation x between the ideal and actual transfer curves (Fig. 2) at the worst case code is given by

$$\langle|x|\rangle = \int_{-\infty}^{\infty} |x| \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(\frac{-x^2}{2\sigma^2}\right) dx = \sqrt{\frac{2}{\pi}}\sigma \qquad (10)$$

This result is a good measure of the average maximal deviation between the actual and ideal curves on all possible codes, which is equal to the expected INL of the ADC. It can also be used for deriving specifications of the ADC building blocks from the required overall performance.

Our analysis so far relied upon the statistical independence of $\sigma_{V_C}, \sigma_{V_R}$ and σ_G. In the more general case where the three error groups are dependent, Equation 9 should be replaced by

$$\sigma^2 = A^2\sigma_1^2 + B^2\sigma_2^2 + C^2\sigma_3^2 + 2AB\sigma_{12} + 2BC\sigma_{23} + 2AC\sigma_{13},$$
$$(11)$$

where the constants A, B, and C are calculated as above and σ_{ij} is the covariance between error groups i and j. In many practical cases, the statistical dependence is due to error sources which are common to some of the groups, e.g. line-width variations can affect both the resistors (σ_{V_R}) and the capacitors (σ_G). In such cases, for two dependent groups X_1 and X_2 we get

$$X_1 = u + \alpha w$$
$$X_2 = v + \beta w, \qquad (12)$$

where u, v and the common error source w are all statistically independent, and α, β are constants representing the dependence. For this case we get

$$\sigma_{12}^2 = \alpha\beta\sigma_w^2, \qquad (13)$$

where α, β are obtained either by recursively applying a similar method of analysis on groups 1, 2 or by fitting the results of Monte-Carlo simulation of each group to Equation 11.

3. COMPARISON: ANALYSIS VS. SIMULATIONS

A whole 10 bit ADC has about 5000 devices, thus a complete SPICE run through all 1023 possible codes (one code is missing due to error correction) would take several hundreds of hours. For this reason, a behavioral simulator has been developed, based on a statistical MATLAB model of each low-level circuit, using parameters that were determined by SPICE simulations of the components of an actual ADC design. Our error analysis is compared to the results of the behavioral simulator. The results, depicted in Fig. 4, show Monte-Carlo simulations (60,000 experiments) of a 10-bit pipeline ADC, compared to analysis for INL and for the yield, which is defined as the expected fraction of good parts (those with INL $\leq$ 0.5). The simulation method is nested as follows. We first draw 100 triplets of ($\sigma_{V_R}, \sigma_{V_C}, \sigma_G$). For each such triplet we further draw 600 values of the actual errors, and then find the INL for each by means of a behavioral simulator. This batch of 60,000 experiments was done for both the cases of independent and fully correlated errors. It can be seen that the limit of the "small error" assumption is practically around $\sigma = 0.7$.

It is interesting to note that analysis and simulation keep a reasonable fit even beyond $\sigma = 1$. This phenomenon may be explained by the use of error correction which extends the linearity of the ADC beyond the expected limits. In experiments with $\sigma \gg 1$ the fit becomes much worse.

4. CONCLUSION

A method was presented for evaluating global statistical errors in terms of component errors in a large mixed-signal system. The method is based on grouping the error sources, evaluating the various error paths, and deriving approximations for the required global parameters. The method was demonstrated by showing that, under proper assumptions,
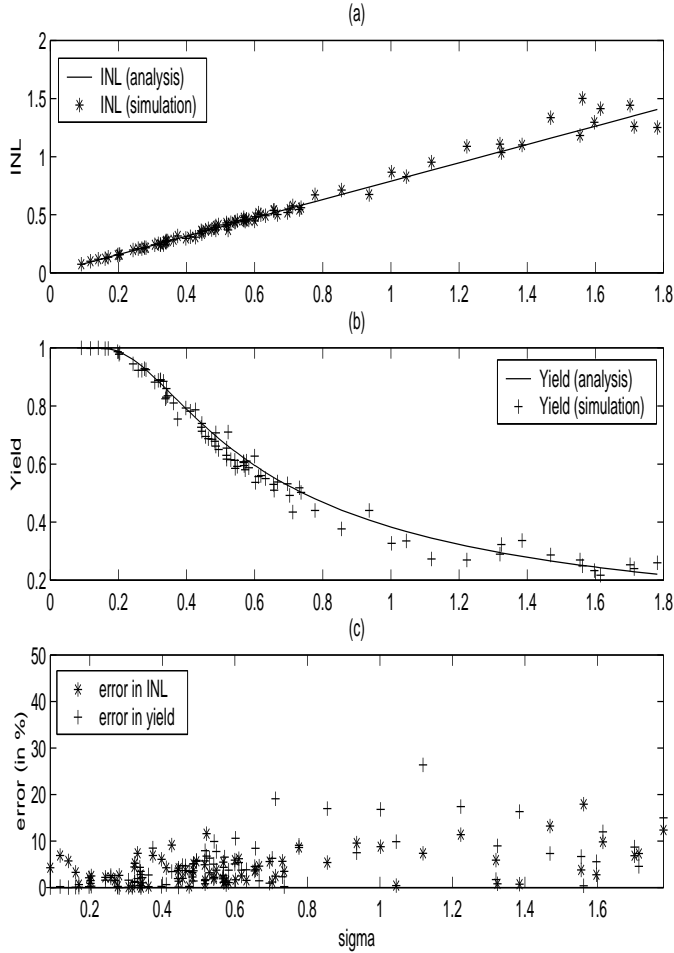
one can derive an analytic expression for integral nonlinearity in a pipeline ADC, which well approximates the results of Monte Carlo simulations. We expect that our approach can be further generalized for other linearity parameters (DNL, SNR) and other mixed-signal systems. These are the goals of our future research in this topic.

5. ACKNOWLEDGMENT

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Figure 4: Monte-Carlo simulations of a 10-bit pipeline ADC compared to analysis for (a) INL and (b) yield (% of parts with INL ≤ 0.5). 600 experiments were performed for each one of 100 random triplets of $\sigma_{V_R}, \sigma_{V_C}$ and σ_G, for both independent and correlated gain errors. The relative error (c) shows the practical limit of the "small error" assumption to be around $\sigma \approx 0.7$.