Practical Application of Full-Feature Alternating Phase-Shifting Technology for a Phase-Aware Standard-Cell Design Flow

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ABSTRACT

As the semiconductor industry enters the subwavelength era where silicon features are much smaller than the wavelength of the light used to create them, a number of "subwavelength" technologies such as Optical Proximity Correction (OPC) and Phase-Shifting Masks (PSM) have been introduced to produce integrated circuits (ICs) with acceptable yields. An effective approach to subwavelength IC production includes a combination of these techniques, including OPC and PSM. Nevertheless, as we approach silicon features of 100nm and below, Alternating PSM (AltPSM) becomes a critical part of the technology portfolio needed to achieve IC requirements. An effective EDA methodology that generates AltPSM ICs must guarantee correct generation of AltPSM layouts, maintain today's design productivity, and leverage existing tools and flows. The implementation of such a methodology becomes more complex as phase shifting is applied to all critical features, including those outside of transistor gates. In this paper, we present a methodology targeted for standard-cell or structured-custom design styles. We also present examples of designs that start from standard-cells created in a manner in which all issues regarding generation of AltPSM are effectively considered, and are then used in a typical cell-based (synthesis-automatic place and route) flow to produce design layouts that are ready for cost-effective silicon manufacturing.

1. Introduction

Now that advanced IC features have dropped below 130nm – well into the subwavelength range – IC designers and manufacturers that support them face a new challenge in meeting IC performance and cost objectives. IC feature sizes are now smaller than the wavelength of light used in optical lithography equipment (Figure 1), yet there are no currently available equipment solutions that utilize a smaller processing wavelength in a production environment. Without significant changes in the methods used to design and manufacture advanced ICs, the move towards even smaller IC feature sizes and higher IC performance stands in jeopardy.

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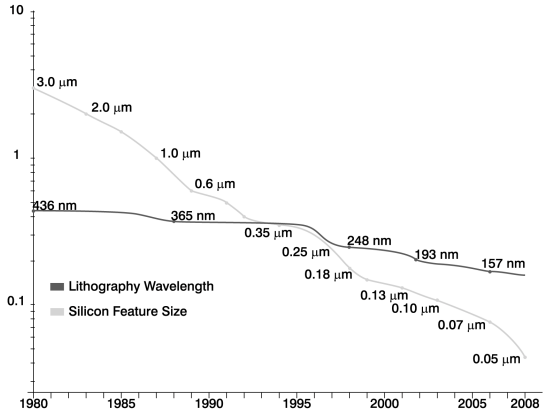

Figure 1 - The Subwavelength Gap

In this *subwavelength lithography* regime, there are two approaches used to control printability. One approach is to perturb the *aperture* (via *optical proximity correction* (OPC)). The second is to perturb the *phase* (via *phase-shifting masks* (PSM)) of light transmitted through the reticle. As a result, the correspondence between layout geometry, mask geometry, and (fabricated) wafer geometry is destroyed. The resulting loss of a "WYSIWYG" (what you see is what you get) regime creates many new constraints and challenges for layout and verification.

The approach discussed in this paper, *Phase-shifting mask* (PSM) technology, enables the clear regions of a mask to transmit light with prescribed phase shift. In a layout with two closely spaced features: the conventional *binary* (chrome on glass) mask has no phase-shifting, while in the alternating PSM (AltPSM) the two adjacent clear regions have respective phase shifts of 0 and 180 degrees. In the phase-shifting mask, light diffracted into the nominally dark region between the clear regions interfere destructively; the improved image contrast leads to better resolution and depth of focus. All PSM variants employ this basic concept, which was proposed by Levenson et al. [1] in 1982.

Currently there are many other experimental approaches to achieve features required for the 0.13-micron process technology, such as aggressive OPC and/or scattering bars. These techniques, although

sufficient for 130nm features, become ineffective or extremely costly as they are used to create smaller features. On the other hand, utilizing alternating aperture phase-shifting mask techniques has been shown to generate 100nm [2] and 70nm [3] features sizes in a production environment. In fact, these techniques have produced features sizes as small as 25nm [4]. Therefore, the alternating aperture phase-shifting masks have emerged as a prime candidate for process technology generations of 0.13-micron and below using 248nm lithography.

Although transistor gate regions are always the smallest features, at much smaller technology generations phase shifting in the gate region alone may not be sufficient. The field poly, for example, can also be difficult to print with reasonable process latitude. Both the gate and field poly regions need to be phase-shifted. In most cases where phase shifting is applied only to the gate regions, phase shifting of the gate regions after the layout has been completed would most likely not create phase conflicts [5, 6]. Application of "full-feature" (gate and field poly) phase shifting after the layout has been completed is almost guaranteed to cause phase conflicts in the result, unless existing methodology is improved. A complete design methodology for AltPSM technology must not only apply phase shifting to both gate and field regions, but it must also *guarantee* correct generation of AltPSM layouts. Furthermore, this design methodology must maintain and leverage the productivity of existing tools and flows. Therefore, a complete EDA AltPSM methodology must also fully leverage the benefits of PSM across all major layout creation flows, including cell library creation, custom layout design, automatic place and route, and physical verification.

This paper illustrates a practical application of AltPSM for a standard-cell design flow. A phase-compliant standard-cell library is first created. An 8051 microcontroller design is then synthesized to this library. The resulting netlist is then placed and routed. Silicon simulation and verification illustrate the correctness and critical dimension (CD) uniformity for both the gate regions as well as the field poly.

2. Current State of AltPSM Technology

For any AltPSM technology, the layout features are either critical or non-critical; the former are thin, and require PSM to resolve, while the latter are wider, and do not require PSM. In AltPSM, a thin critical feature is made when the clear areas on opposite sides of the feature are exposed with light of opposite phase. Indeed, whenever two opposite-phase clear regions of the mask abut, their (dark) border prints as a (possibly unwanted) feature.

Although there are other styles of AltPSM, the methodology and application described in this paper is based on Numerical Technologies (NTI) style of phase shifting. NTI Double-exposure style PSM (Figure 2) uses a first exposure (with a "dark-field" - or locally clear-field - AltPSM mask) with 0-180 transitions to define critical features. A second exposure with a standard clear-field binary mask exposes away the unwanted 0-180 boundaries while patterning non-critical features and preserving critical features [7].

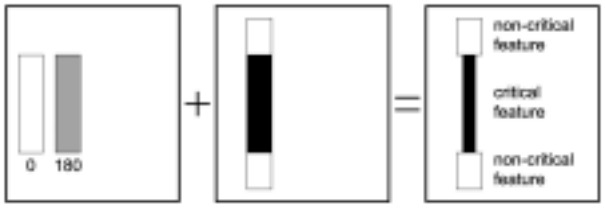

Figure 2: NTI Style PSM

3. AltPSM Implications for EDA

Fundamentally, AltPSM changes the requirements of EDA tools for layout creation and verification because "design rule correctness" is no longer a local phenomenon that can be checked by traditional physical verification capabilities. Shifters must be defined and positioned on opposite sides of each critical layout feature in order to achieve the desired printed critical dimension. The shape of these shifters is highly context dependent.

There are also two constraints on the phases that can be assigned to shifters. First, as we have already seen, shifters on opposite sides of any given critical feature must have opposite phases. Secondly, if shifters used to define different features overlap, they must have the same phase. Phase assignment for AltPSM seeks to assign phases to shifters such that these two constraints are satisfied. Intuitively, "parity" implications (0 forces 180, which forces 0, which ...) must be self-consistent in order for the layout to be phase-shifted. This can be formalized as bipartization (making 2-colorable, or equivalently, ensuring "no odd cycles") of a shifter graph with nodes corresponding to shifters and edges corresponding to (i) pairs of shifters which define critical features and (ii) pairs of overlapping shifters. In other words, determining whether a given layout can be phase-shifted requires a global analysis of a phase conflict graph defined over the layout to determine whether this graph is bipartite [8, 9].

4. Design Flow Utilized in this Application

In this application we used a fairly typical standard-cell design flow that would be used for non-PSM designs, and tested the ability to generate an AltPSM compliant design. We created a 0.13-micron standard-cell library. These cells were designed to easily handle phase-shift requirements (see Section 4.1). Subsequently, an 8051 microcontroller soft core was synthesized to this library and then placed and routed. The last stage of the design flow was to verify the correctness of the results.

4.1 Phase-Compliant Libraries

By definition a phase-compliant (also called phase-aware) library is one containing elements without intra-cell phase conflicts. A phase-compliant library also minimizes the chance that the final layout will have phase conflicts when used in a semi-custom physical design methodology.

In order to implement these library elements, three types of "rules" were utilized to ensure phase-compliance:

1) Local Geometry Rules:
    a. Promote the creation and phase-assignability of shifters.
    b. Promote phase shifter integrity.
2) Global Colorability Rules
    a. Enable legal phase assignment to phase shifters.
3) Free Composability Rules
    a. Prevent phase conflicts from arising in cell-based automatic place and route.

Examples of Type 1 rules include no minimum-width T's on the poly layer, rules to keep the distance between endpoints of two collinear critical features greater than some minimum spacing, and rules that enforce the distance between any 0-phase shifter and any 180-phase shifter to be greater than some minimum spacing. Type 1 rules can be checked via standard DRC techniques and tools.

The Type 2 rules have been recently addressed by academic researchers [10, 11]. Examples include rules to avoid odd cycles in the (planar) conflict graph. Efficient and scalable algorithms for automatic conflict resolution appear to be available, and necessary linkages with compaction-enabled layout synthesis (cf. [12]) appear very tractable.

As for Type 3 rules, an example is to allow only 180-degree phase shifters within some threshold distance of the upper cell boundary (for horizontal critical features). Another example of such rule is to require all phase shifters to be placed at a distance greater than some minimum spacing from the cell boundary.

Type 3 rules that make an attempt to guarantee complete cell composabilty (e.g. requiring a minimum space between any shifter and the cell boundary) can be verified using DRC techniques. However, guarantees of composability by placing "buffer" space around cell boundaries become increasingly costly in terms of density: the economic requirement for phase composability arises because it becomes meaningless to waste several line pitches around each cell boundary and significantly effect design density purely in the interest of "composability" (the alternative is a very narrow process window – which is also economically bad). Poly geometries also often approach the cell boundary. Notably, in modern 7- to 9-grid high libraries, complex cells such as sequential elements have forced horizontal poly runs near power and ground rails: These induce phase conflicts, especially in double-back (shared power / ground rail) cell architectures.

On the other hand, there are other type 3 rules that do not require complete cell composability, but endorse a style or requirements where phase conflicts between the cells (at the boundaries) are minimized or are of known shape and structure. These type 3 rules do not completely guarantee free composability, but they do leave the necessary degrees of freedom needed to further optimize the layout of each cell either prior or as needed during the standard cell design flow.

Assuming that all cells are free of intra-cell phase conflicts (i.e. Type 1 rules are satisfied), the specific type 3 rules are verified through ensuring that no cell interaction produces phase conflicts. However, in case of inter-cell conflicts, one or both of the cells causing this phase conflict can be exchanged with equivalent cells with regenerated phase shifters, using the phase information at the boundaries of the two cells to resolve the inter-cell conflict. The verification of these specific rules cannot be done by DRC techniques and require global phase assignment techniques and software [13].

4.2 Creating the Library for this Application

First, we created a 0.13-micron standard-cell library using Numerical's Cadabra abraCAD product and Library Factory flow. Starting from SPICE schematic netlists, the abraCAD product automatically creates DRC correct GDSII layouts given a certain architecture.

In order to create this base library, we used Cadabra RapidStart architecture on a TSMC 0.13-micron process, along with a combination of type 1 and type 2 so that there were no intra-cell phase conflicts. Intra-cell phase assignment was verified by Numerical iN-Phase, and resolved by making simultaneous adjustments to the first and second exposure mask structures. This resulted in a variant set of cells. In the future, this is an area where phase mask design and silicon simulation can be intelligently combined with layout synthesis to further automate the phase-compliant library cell design.

The final printability analysis of the variant cells was verified by silicon simulation using Numerical IC WorkBench. These Cells were extracted and then characterized using Cadence Assura RCX and Silicon Metrics CellRater.

The cells contained in this library covered a wide variety of functions and drive strengths, both for design purposes, as well as for exercising the types of rules required to meet phase-compliance. Figure 3 illustrates examples of these cells in phase-compliant layouts as well as silicon simulation results. As can be seen from the figure, extraordinary CD uniformity and CD control can be achieved through AltPSM implemented in these cells.

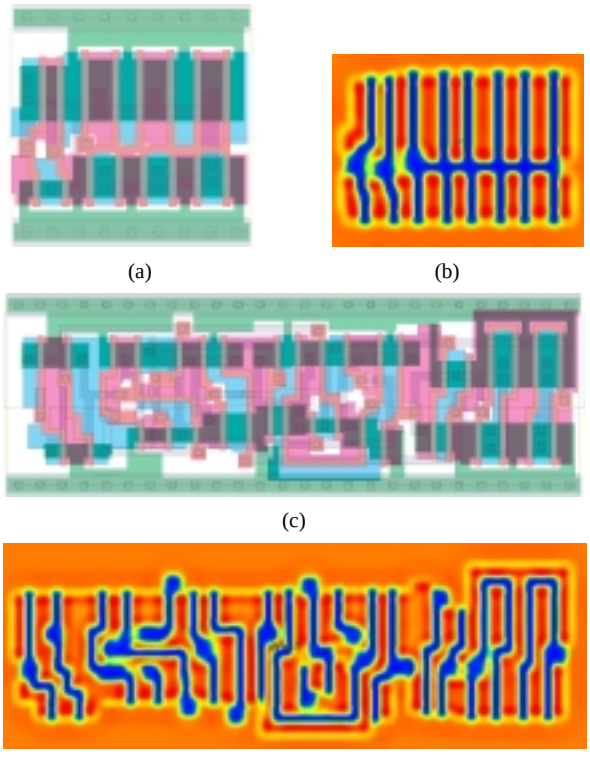

Figure 3: (a) Layout of phase-compliant cell "or23" (b) Simulation results for cell "or23" (c) Layout of phase-compliant cell "drbb1" [DFF with set and reset] (d) Simulation results for cell "drbb1"

4.3 Implementing the DW8051 Microcontroller with AltPSM

A DW8051 microcontroller soft core from Synopsys was synthesized to this library using Synopsys Design Compiler. The resulting netlist was then placed and routed and optimized for density using Cadence Envisia SiliconEnsemble. The final stage of the design flow was to add optical proximity correction features and to verify the correctness of the results. The tools used in this final stage included Numerical iN-Phase and SiVL (Silicon vs. Layout Verification).

Figure 4 illustrates silicon simulation results of several locations on the layout including various inter-cell boundaries. It can be seen that using phase-compliant libraries and a place and route tool, phase conflicts between the cells are easily handled in a way that the final silicon pattern shows CD uniformity and CD control in the gate and field poly geometry close to cell boundaries where phase-conflict detection, phase-conflict resolution, and phase assignment are impossible prior to place and route.

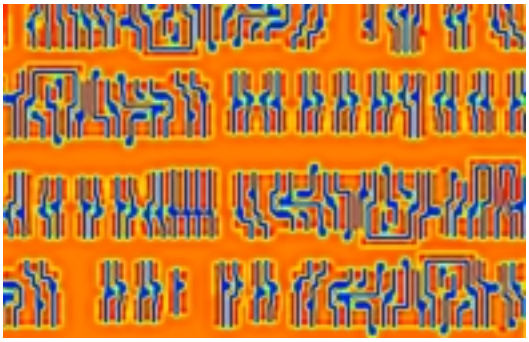

Figure 4: Simulation result of multiple interactions among standard-cells between adjacent rows and within each row

5. Future Work

In the future we plan to expand this work to include the effects of AltPSM on the timing aspects of the design flow. It is obvious that as AltPSM is applied to gates (and perhaps the field poly) the performance of the transistors and hence the library cells are significantly increased. Our future work will study the effect of this change – which can be selectively applied within the netlist – on synthesis, timing analysis, clock and buffer insertion, and timing verification.

6. Conclusion

In conclusion, we have described a feasible, complete design methodology for AltPSM – a standard-cell design methodology that transparently distributes the burden of PSM-awareness over library cell creation, and standard-cell place and route. We emphasize that this is a real methodology that multiple EDA vendors are working to deliver in production tools (from custom layout to automatic place and route to physical verification), and discuss rules specific to creating library cells that are phase-compliant as well as composability requirements to support automatic standard-cell place and route.

These techniques are currently under development for the commercial EDA context. From a structural viewpoint, establishing a common AltPSM strategy for cell library providers, layout synthesis vendors, automatic place and route tool vendors, as well as constituencies in physical verification and mask inspection, will help reduce the development time before the semiconductor industry reaps the full benefits of AltPSM technology.

7. References

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