Reticle Enhancement Technology: Implications and Challenges for Physical Design

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ABSTRACT
In this paper, we review phase shift lithography, rule vs. model based methods for OPC and model-based tiling, and discuss their implications for layout and verification. We will discuss novel approaches, using polarizing films on reticles, which change the game for phase-shift coloring, and could lead to a new direction in c:PSM constraints on physical design. We emphasize the need to do tiling that is model-driven and uses optimization techniques to achieve planarity for better manufacturing tolerance in the subwavelength dimensions era. Electromagnetic solver results will be presented which estimate the effect of tiling on circuit timing.

Keywords
RET, Reticle Enhancement Technology , subwavelength lithography, mask data preparation, OPC, PSM, optical proximity correction, tiling.

1. INTRODUCTION
As the semiconductor industry evolves toward higher densities of integrated circuits at smaller dimensions, the lithographic patterning process margin is reduced. In 1998 we were manufacturing 250 nm minimum feature circuits, using steppers with 248nm wavelength. Today we are about to qualify 130nm processes, while the next generation of lithography, at 193nm, is not yet mature.

One consequence of this trend is that in order to print manufacturable features on Si, we must modify physical design data post tapeout. In this new post-GDS flow for physical design, optical proximity correction (OPC), phase shift mask (PSM) design, and model-based tiling may all be required. Together these techniques are designated Reticle Enhancement Technology (RET).

For phase shift, we describe new, less restrictive design methods which can be achieved by adding polarization to phase shift modification of the lithographic imaging process. OPC is described and related to the new challenges it brings to design verification.

Tiling adds new features in sparse areas to ensure better planarity, as the chemical-mechanical polish progresses at different rates in sparse and dense areas. Planarity of polish achieves manufacturable results due to more uniform processing of features such as vias, and depth of focus benefits.

However, adding new shapes AFTER the circuit designer has performed timing analysis could potentially require design retiming. Our electromagnetic analysis shows that this issue is less of a concern than intuition might have indicated.

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2. COMPLEMENTARY PHASE SHIFT DESIGN ISSUES
Primary implications for physical design of complementary phase shift masking (c:PSM) are new design constraints, additional data types and volume, new forms of design rule checking, and validation that the c:PSM design will print what the designer intended (Silicon vs. Layout (SiVL) validation).

2.1 New Design Constraints
Complementary Phase Shift Mask design (c:PSM) places new constraints on device layout that, like other physical design rules, are required both for mask and wafer manufacturability. These constraints are in addition to those imposed in conventional layout because they provide clearance for phase shift structures that are not present in the original layout, but rather are to be added later during mask data prep. OPC is not subject to these issues, as it introduces relatively small changes to the design data. Of course, the design process could in principle provide for simultaneous layout of the c:PSM structures and the Si-based structures, but such a new paradigm would require substantial retraining of layout people and modification of legacy automated layout algorithms. A neighboring paper in this session [1] describes many of these issues in significant detail, as does reference [2].

As an example of the type of layout rules that must be imposed, consider the "perpendicular gate problem" (Fig.1.). Conventional lithography leads to a familiar design rule that there is some minimum space between the poly of one gate and the active (source-drain) region of the other. Additional spacing rules are imposed if c:PSM is to be used for the lithographic process. The c:PSM "phase mask" must be constrained to provide *at least* minimum chrome feature size between each aperture, as is required for mask inspection. If regions of alternating phase were allowed to touch (chromeless phase shift mask) the resulting phase edge would be indistinguishable from a reticle defect -- a "phase defect". In addition to this mask manufacturing requirement, the wafer lithography process imposes additional constraints. A complementary mask pair has an embedded phase shift region on the "phase" mask and a protective shadow region on the "trim" mask. The size of these structures is characteristic of

a specific wafer lithographic process and is best determined through a combination of experimentation and modeling. Furthermore, a minimum shifter width and minimum shifter extension past the active region is required. These constraints must be captured in the design rules in an efficient way to avoid wasted silicon area. (Fig. 1).

The purpose of the trim mask in the c:PSM pair is to protect a gate which has been formed during the phase mask exposure and "trim away" unwanted photoresist, as well as defining poly lines over the field (isolation oxide) region. The trim width is empirically determined so as to be large enough to minimize impact of the exposure process on the gate that it is protecting. Too large a trim width will waste silicon area , while too small trim width will allow unacceptable critical dimension (CD) variation

Phase regions, which are clear apertures in a negative density mask, must be large enough to be imaged well by the wafer exposure tool. However, the main trim size and main shifter size are not independent. Phase regions must enclose any trim that does not abut drawn poly. The amount of the required enclosure is characteristic of both the wafer exposure process and the reticle manufacturing process.

One additional characteristic parameter is required to specify the design rule that must be imposed to insure that phase shifters may be successfully placed to define the perpendicular gates of Figure 1. Some extension of the phase shifter past the active edge must be designed to provide for uniform CD of gate as poly crosses from active to field oxide. Once again this parameter is characteristic of the wafer lithographic process.

2.2 Design Rule Checking

It is essential to check the output of an automatic c:PSM conversion algorithm to verify that the design constraints have been met. This requirement is similar to running Design Rule Checks (DRC) on layout that has been generated by automatic place and route tools. However new rules are required which reflect mask manufacturing and overlay tolerances, rather than Si process rules alone.

2.3 Silicon vs. Layout Validation

Ultimately, a full chip calibrated process model is important for validating that subtle interactions of a specific c:PSM design and the wafer process are not problematic. For example, because c:PSM is a two-mask double exposure technique, the overlay of complementary masks is a critical process parameter. While the initial parameters supplied to the c:PSM algorithm are chosen to allow for process capabilities such as overlay, it is important to verify that there is no layout situation which somehow thwarts the attempts to allow for process variations. A simple aerial image threshold model is not sufficient to resolve such cases. The detailed process response to many general situations should use a calibrated model to validate the final c:PSM design.

3. Polarized Phase Shift Mask and Its Potential Impacts on Gate Design

Recently a polarized phase shift mask (p:PSM) was invented by some of the authors. The p:PSM utilizes polarization properties of light to eliminate phase conflict in a phase shift mask and thus obviates the 2nd exposure and mask of the c:PSM technology. This novel approach imposes fewer constraints on the design of gate patterns than c:PSM does, and therefore increases the design flexibility.

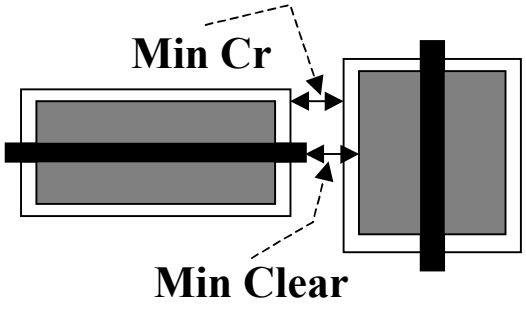

Figure 1: Parameters limiting perpendicular gate space

3.1 Basic Concept of Polarized PSM

A p:PSM, like any typical phase shift mask, contains transparent regions which generate either 0 or 180 degree phase shift to incident light. However, in a p:PSM the transparent regions also polarize transmitted light with either the same or orthogonal polarization states. Regions with one polarization state but opposite phases are utilized to define desired features, as in a conventional hard phase shift mask. In the area where no feature is present and yet two regions with same polarization state but opposite phases unavoidably meet, a third transparent region with a polarization state orthogonal to the first one is placed in between these two regions (The c:PSM strategy would make this third region opaque in the first, phase shift mask, and transparent in the second, binary mask). Fundamental physics dictates that illumination with orthogonal polarization states does not interfere at the boundry. Therefore the third region, be it 0 or 180 degrees in phase, transmits light without leaving undesired features due to destructive interference of light at its borders with either one of the first two regions.

Shown in Fig. 1 is a typical pattern whose minimum spacing is determined by avoiding the phase conflict problem, and in Fig. 2 a p:PSM is used to define this pattern. The black regions are opaque and represent the features. The hatched regions transmit light with a polarization state parallel to the hatch marks, and the numerals in these regions designate the phase shift.

The dual mask / double exposure c:PSM technique creates serious difficulties in process, including alignment errors between the two exposures, which drives mask layout rules to looser design densities, and also leads to decrease of process throughput. The alignment problem, especially, becomes increasingly detrimental as feature size reduces. Therefore, implementation of one mask / single exposure p:PSM has clear advantages for the photolithography process. It will also favorably impact the physical design of the gate/polysilicon layer.

3.2 Potential Impacts on Gate Pattern Design

As discussed in previous section of this paper the phase shift technology imposes on physical design constraints due to mask manufacturability, wafer process capability, and phase coloring

scheme. All these constraints will be different when the p:PSM technique replaces c:PSM, as is shown in Table 1:

Table 1. Comparison of Constraints on Physical Design from c:PSM and p:PSM

Cause of Constraint on Gate Pattern Design	Constraints from c:PSM	Constraints from p:PSM
Phase Shift Mask Manufacturability	Minimum Chrome. Minimum Space.	Minimum Chrome. Minimum Space.
Binary Mask Manufacturability	Minimum Chrome. Minimum Space.	None.
Wafer Process Capability	Minimum Printable Space and Line. Alignment Margin. Minimum Protecting "Shadow".	Minimum Printable Space and Line.
Coloring Scheme	Opaque. Transparent with 0 or 180 phase.	Opaque. Transparent with 0 or 180 phase, and X or Y polarization.

The table demonstrates that p:PSM imposes less constraints on gate pattern design than c:PSM does. This can be illustrated using Fig.1 as an example. Constraints on the minimum poly-to-poly distance d_{min} from c:PSM technique was discussed above. Using p:PSM, however, the only constraint is:

d_{min} = minimum width of polarizing film + minimum width for isolated shifter.Here the minimum width for an isolated shifter only needs to be printable. It should be significantly smaller than that required by c:PSM, where it must be large enough to avoid the problem of CD variation caused by overlay error. Assuming the minimum width of polarizing film is determined by the same mask manufacturability issues as for c:PSM and that the minimum chrome rule is the same, then d_{min} will be smaller when p:PSM replaces c:PSM. The same conclusions can be reached for other more complicated patterns. Therefore, p:PSM has the potential to increase gate density since it eliminates constraints on gate pattern design which are caused by the 2nd mask/exposure of c:PSM.

4. Optical Proximity Correction Issues

In silicon patterning processes, the resulting wafer images can be very different from the ones drawn by the designers. This loss of pattern fidelity happens during the mask masking, wafer imaging and etch steps. One way to overcome the problem is to predict the loss of pattern fidelity up-front, then modify the design layout on the photo-mask to compensate for it. This layout modification is commonly referred to as optical proximity correction (OPC)[3] since optical proximity effect in wafer imaging has traditionally been the primary cause of fidelity loss.

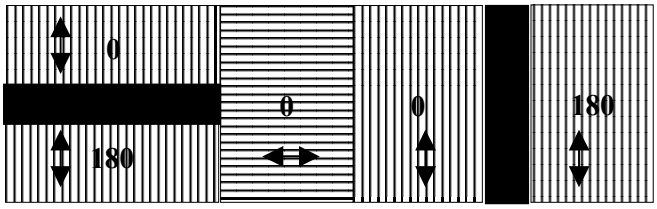

Figure 2: Layout of p:PSM to Define the Pattern in Figure 1.

OPC began to be widely deployed in the IC industry starting approximately at 0.25µm technology generation. Today, for the 0.13µm generation to be in production later this year, roughly 10 critical lithography layers will require OPC. Since OPC has become a standard process in IC technology, people consider a particular physical layout manufacturable as long as the layout after OPC can reproduced with good image fidelity on silicon wafers. Naturally, *OPC-compliant* design rules for physical design will be desirable to guarantee the success of OPC during the down-stream process.

However, it is impractical to come up with OPC-compliant design rules in many companies. A typical flow of interaction between design rule generation and OPC is illustrated in Fig. 3. Design rules for a particular technology generation are defined early in the development stage. This is done by extrapolation of the design rules from the previous generation, and prediction of silicon imaging capabilities with existing data. Then, designers use these rules to do physical layout for all library cells. Some of these cells will be corrected by the OPC step, and the corrected layout will be evaluated for its manufacturability on silicon wafers. Typically, a few iterations are needed to refine the OPC algorithm and silicon

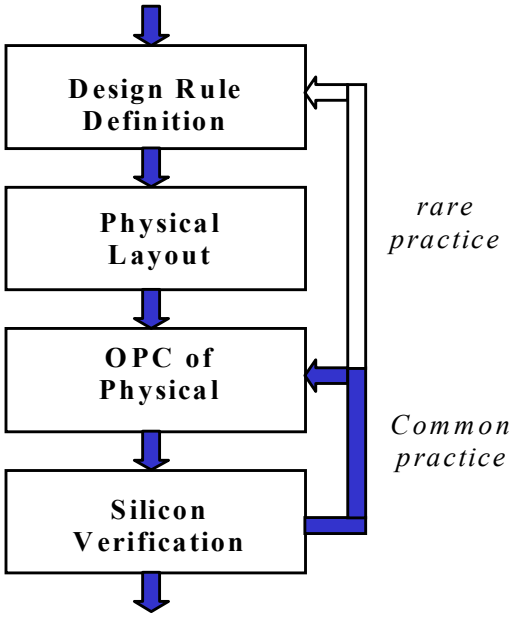

Figure 3: A typical flow of interaction between design rule generation and OPC.

processes before one finalizes the OPC algorithm, or determines some design rule which is so ill-defined that even OPC can not make it manufacturable.

If the latter happens, ideally one can go back and modify the design rule to make it OPC-compliant. However, by the time one is certain about the deficiency of certain design rules, designers have devoted a lot of resources to the physical design already. Unless it is a minor design rule change, it is very expensive to

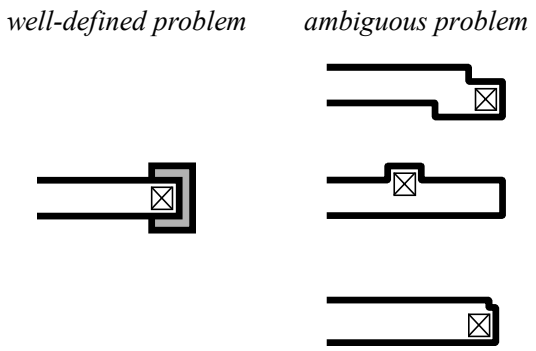

Fig. 4: Examples of well-defined and ambiguous OPC problems

modify the design rule at this stage.

A common solution to this problem, especially if it happens late in the development cycle or in production, is to modify the physical layout away from what was originally designed to buy back manufacturability in silicon processing. For example, if a process engineer cannot produce with good process latitude a 0.20μm isolated gap drawn by the designer, he/she may decide to modify the layout so a 0.22mm gap is imaged. By doing so, the process engineer has made a trade-off between having good image fidelity with little process latitude, and having poorer image fidelity with larger process latitudes and the risk of poorer circuit performance.

Even though it is not practical to come up with design rules to guarantee physical layout to be fully OPC-compliant, it is possible to devise general rules so the physical design is more *OPC-friendly*. By OPC-friendly, we mean geometry in the design requiring OPC is well defined and easily recognizable. For rule-based OPC, presumably we know which specific design situations require correction, and thus implement rules to correct for it. A simple example is illustrated in Fig. 4 (left), where a hammerhead is added at metal line-end to ensure proper contact coverage. The problem is not as well-defined in Fig. 4 (right), where a simple algorithm to add a hammerhead at line-ends may not work. One has to devise a more robust algorithm to handle these situations, probably at the expense of adding extra polygons that are not needed. The same problem can be alleviated but not removed by using model-based OPC, since one still has to specify the minimum jogs in the layout that can be ignored. If design rules can be defined so that cases in Fig. 4 (right) can never happen, then the layout is considered OPC-friendly, and it can drastically reduce the OPC development time, the OPC correction run time, and the OPC output file size.

5. MODEL-BASED TILING

Chemical-mechanical polishing (CMP) is the widely adopted technique of choice for global planarization. Its current applications include vital process steps such as shallow trench isolation (STI) and multi-level inlaid copper interconnection. Control of post-CMP topography variation is crucial in meeting challenges like the ever decreasing depth-of-focus in photo-lithography and the ever increasing levels of interconnect due to routing complexity.

All experiments conducted up-to-date conclude that post-CMP topography variation is strongly dependent on layout pattern. Therefore, layout optimization in physical design, utilizing dummy features, is necessary to change the layout pattern distribution and thus control post-CMP topography variation. However, inserting dummy features of a prescribed density ad hoc, wherever there is empty space in layout that is large enough, is neither effective nor efficient. Recent studies on inter-layer dielectric (ILD) CMP are based on linear models oxide polish [5,6,8]. Specifically, global density assignment followed by local insertion, proposed by Tian et al. to solve the dummy feature placement problem in the fixed-dissection regime with both single-layer and multiple-layer considerations, gave excellent results by reducing simulated post-CMP topography variation from 768A to 152A. Figure 5 of Reference [11] shows the density maps and simulated post-CMP topographies for the comparison of conventional and model-based tiling strategies presented in [8].

While those studies are useful for aluminum interconnects, they are no longer applicable to the majority of the CMP steps in 0.22μm or smaller manufacturing technology nodes using copper interconnects. More recent studies on shallow trench isolation (STI) and copper CMP formulated the dummy feature placement problem as a nonlinear problem for the complex situation of polishing multiple materials simultaneously while considering

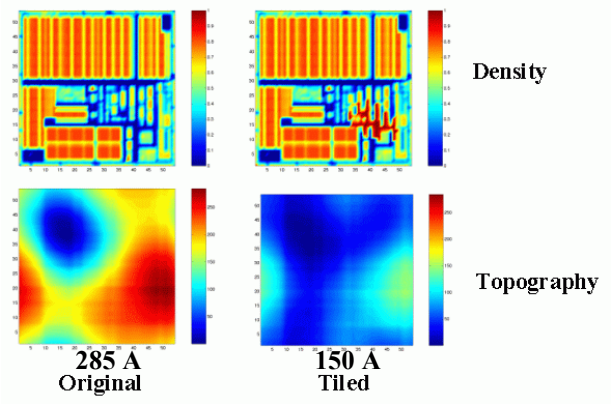

Figure 5: Model-Based Tiling Example for STI

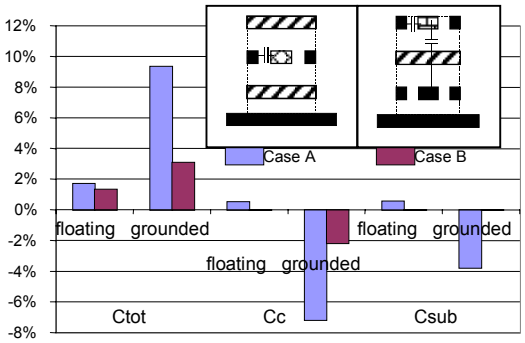

Figure 6 The percent change in capacitances of dense interconnect lines with respect to total capacitance without tiling.

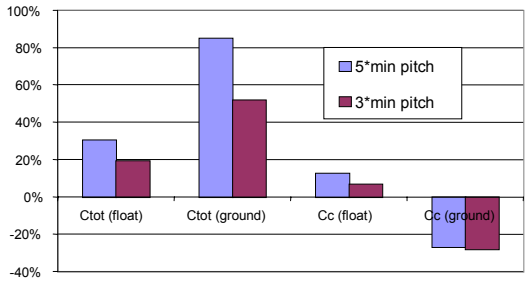

Figure 7 The percent change in capacitances of sparse interconnect lines with respect to total capacitance without tiling.

physical effects of polish pad bending and local polish pad compression [9,10]. The new nonlinear problems are much harder to solve than the linear problem for ILD, but the proposed iterative methods are very promising as solutions. Figure 5 shows the density maps and simulated topography for an example of STI tiling from [10].

Furthermore, dummy feature placement itself is a physical design solution with the objective of enhancing planarity. However, these solutions to the dummy feature placement problem may create new problems for timing and verification. Firstly, although simulations of coupling noise due to dummy features show no significant impact for the current generation of manufacturing technology node (see Section 6), future generations may not be so forgiving. Secondly, the impact on performance due to systematic process and device variations was studied by Mehrotra et al. with hypothetical scenarios in [7]. The study found significant impact due to relatively small amount of post-CMP topography variation. Finally, all dummy feature placement problems are solved for flat design data as a reticle enhancement technique after design tape-out. Design rule checking and parasitic extraction on flat data with dummy features is almost impossible, because the dummy features are not in the original design hierarchy. A recent study of hierarchical dummy feature placement by Chen et al. [4] has found that there is substantial trade-off between solution quality in terms of planarity achieved and the amount of original design hierarchy the inserted dummy features can preserve.

6. TIMING IMPLICATIONS OF TILING

The result of tile placement manifests itself as a source for parasitic electromagnetic effects which are not easily foreseen during layout and design. The metal shapes used for tiling change the interconnect behavior, specifically interconnect capacitance and hence signal delay and cross-talk.

It is well known from classical electromagnetic theory [12] that introducing a new metal object to a group of metal objects will increase their total capacitance. This is certainly true for interconnect lines and metal tiles. Recently, several studies have reported that these effects can be quite significant [13]. However, the exact change in interconnect capacitance will depend on the type of tiling shapes as well as the characteristics of the design layout and silicon process.

The main parameters to influence this change are tile sizes and proximity to interconnect lines. The larger the size of the tile the larger the consequent interaction between interconnect lines. Similarly the closer tiles are to interconnect lines the stronger their interaction will be.

In order to quantify the change in interconnect capacitance, we have considered several structures that are expected to represent the most profound effects. These structures were simulated using an in house 3D model builder RUBY and field solver Raphael [13] for a recent silicon technology developed at Motorola. We have compared the changes in capacitance components when the tiling metal shapes were allowed to float as well as when they are grounded.

The first structure (Figure 6 case A) is intended to characterize the change in intra-layer coupling for lines placed at minimum pitch over the silicon substrate. For simplicity, they are taken to be at the second metal layer while the tiling metal planes were placed above and below the whole array to represent large tiling shapes. The changes in interconnect capacitance are given as a ratio with respect to the total capacitance of the line when there is no tiling, and for floting tiles the effect is negligible (<2%). In contrast, the capacitances are drastically changed (~10%) if the tiles are grounded.

Another structure (Figure 6 case B) was chosen to look at the coupling capacitance between two metal layers. This structure has two parallel line arrays with minimum pitch at the first and third metal layers above the substrate. The metal tile is placed between them on the second layer. Again, in this case the change in capacitance is found to be very small ~1% when the tiles are floating.

We have observed that dense lines effectively do not suffer much from floating tile placement above and below them since their capacitance is mostly dominated by their coupling to neighbors. The other limiting case where interconnect lines are more sparsely separated behaves differently. As an example, the coupling between lines separated at 3 and 5 times the minimum pitch showed considerable change in total capacitance (20% and 30% respectively) in comparison to the dense cases above (See Figure 7). The floating tile above and below provided a much shorter effective distance between the interconnect lines. However, this last case should not be too much cause for alarm since the

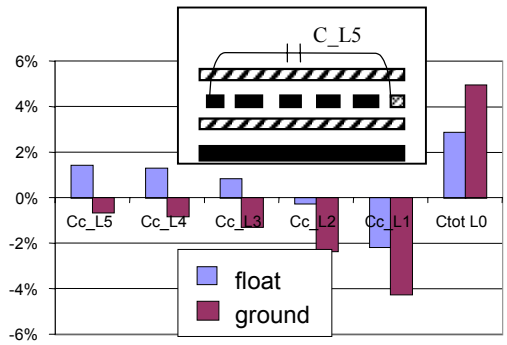

Figure 8 The percent change in neighbor capacitances of dense interconnect lines with respect to total capacitance without tiling. The coupling to next to neighbor lines are increased by floating tiles.

absolute value of the capacitances are much smaller than the dense cases.

The last case also shows the importance of tile size. Had the tile shape been smaller than the separation between lines the effective interaction distance between them would not have been as short and therefore their coupling would not have been increased. In other words large tiling shapes are very effective in carrying local effects to their extent. As another example, consider the dense array of lines shown in Figure 7. It is easily noticed that, next-to-nearest neighbor coupling is increased by tiling. Therefore, if tiling has to be performed over critical paths, using smaller tiles with same tiling density would prevent unnecessarily increasing the interconnect capacitance.

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