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36th Design Automation Conference
June 21 - 25, 1999
New Orleans, LA

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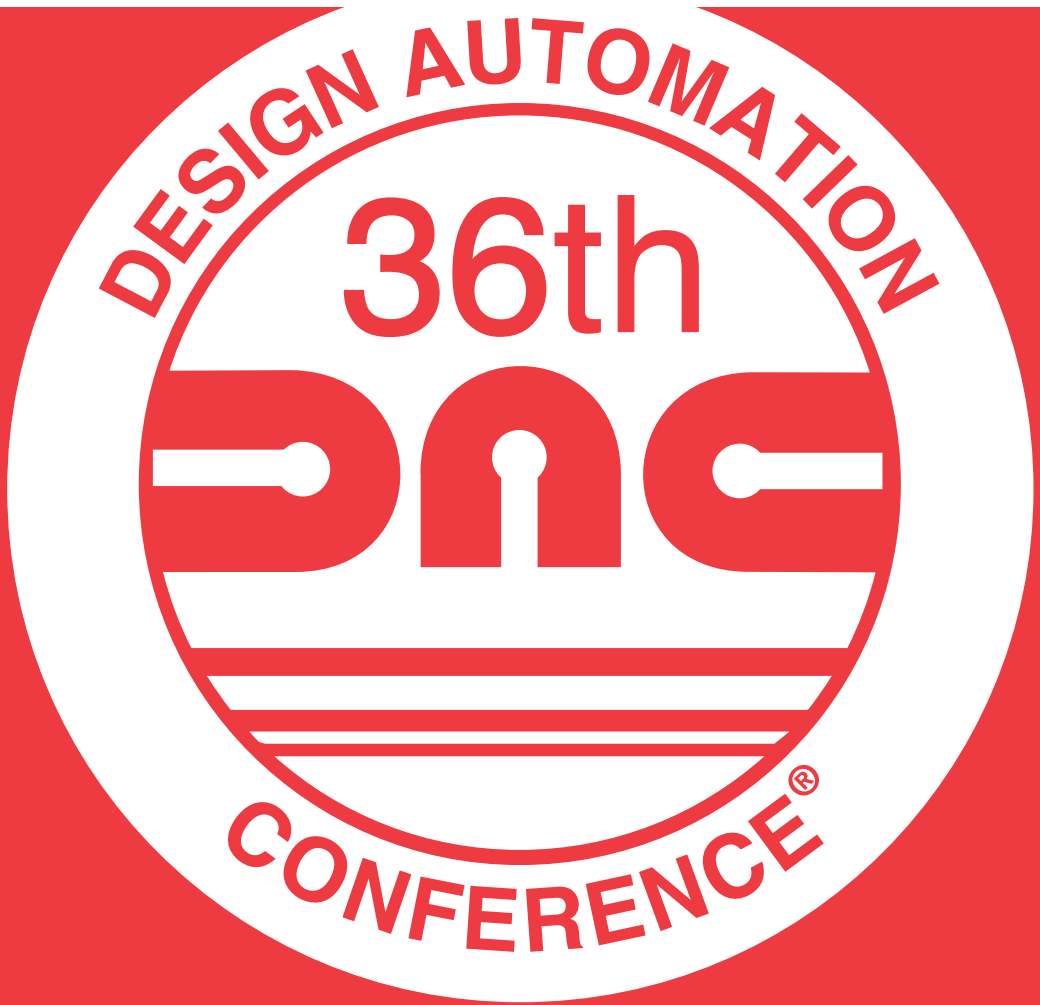
PROCEEDINGS 1999

DESIGN AUTOMATION CONFERENCE®



Ernest N. Morial Convention Center, New Orleans, LA, June 21 - 25, 1999

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General Chair's Welcome

General Chair's Welcome

Welcome to the 36th annual Design Automation Conference (DAC). DAC is organized to facilitate technical interchanges among design automation researchers and developers, the engineers who use DA systems, and the vendors who provide both DA systems and silicon. It has become the premier conference for the presentation of research and development work in electronic design automation (as part of the Design Tools track) and is quickly emerging as the preferred conference for presenting next generation electronic circuits and systems design experiences (as part of the Design Methods track). DAC also continues to be the forum where the EDA industry exhibits leading edge products and makes new product announcements. In its second year, Silicon Village ensures that silicon and IP vendors are also represented at the conference.

These Proceedings, representing an outstanding technical program, were assembled under the leadership of this year's Co-Program Chairs, Randy Bryant and Bryan Ackland, and Panel Chair, Jim Rowson. 451 papers from around the world were submitted to the Design Tools and Design Methods tracks, and were reviewed by over 700 EDA and system design professionals. These reviews, along with a detailed examination by the Technical Program Committee, yielded the 154 papers included in this Proceedings and to be presented at the conference. These papers are complemented by seven panel sessions, sixteen invited papers, four embedded tutorials and three university design contest paper finalist. A special mini-track, consisting of one panel and two sessions of invited papers, will take DAC's first look at how traditional CAD and embedded system software tools will converge to meet the special needs of embedded systems.

I want to thank all of the people who contributed to making DAC *the* premier conference for electronic design automation and design methods: the DAC Executive Committee, the Technical Program Committee, the Exhibitor Liasion Committee, MPAssociates, Inc., and especially the exhibitors, authors, speakers, session organizers and session chairs. DAC is sponsored by ACM/SIGDA, IEEE Circuits and Systems Society, and the EDA Consortium. Their members represent the breadth of DAC's participants and we are thankful for their continued and active support.

Welcome to New Orleans and the 36th Design Automation Conference. We wish you a very productive and fun-filled week in a southern city famous for its old-world charm, creative jazz and fine dining. We trust that you will find these Proceedings to be a valuable resource and reference for many years to come.

Mary Jane Irwin

General Chair, 36th Design Automation Conference

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1999 IEEE Fellows

- **Aart J. de Geus** - Synopsys, Inc., Los Altos, CA
  "For leadership in developing and commercializing logic synthesis technology"
- **Pinaki Mazumder** - Univ. of Michigan, Ann Arbor, MI
  "For contributions to the field of VLSI design"

1998 ACM Kanellakis Award

The 1998 ACM Kanellakis Award for Theory and Practice was awarded to:

Randal E. Bryant - Carnegie Mellon Univ., Pittsburgh, PA

Edmund M. Clarke, Jr. - Carnegie Mellon Univ., Pittsburgh, PA

E. Allen Emerson - Univ. of Texas, Austin, TX

Kenneth L. McMillan - Cadence Design Systems, Inc., Berkeley, CA

for their invention of:

"Symbolic Model Checking"

1999 SIGDA Distinguished Service Awards

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) presents its Distinguished Service Award to Professor C.L. Liu, National Tsing Hua University, Hsinchu, Taiwan, ROC, for contributions to the Design Automation Community and for creating the journal ACM Transactions on Design Automation of Electronic Systems (TODAES).

1999 SIGDA Doctoral Thesis Awards

- Inaugural Winner - **Dirk Stroobandt** - Univ. of Ghent, Ghent, Belgium, for:
  Analytical Methods for a prior Wire Length Estimates in Computer Systems.
- Honorable Mention - **Naresh Maheshwari** - Iowa State Univ., Ames, Iowa, for:
  Fast Algorithms for Retiming Large Digital Circuits.

1999 Best Paper Award

This year, awards were made for the best papers in four categories. Winners were determined from detailed reviews of the accepted papers in the technical sessions. Each award is accompanied by a plaque and a cash award of $400. The awards are given by ACM/SIGDA (Special Interest Group on Design Automation), IEEE/CAS (Institute of Electrical and Electronics Engineers/Circuits and Systems Society) and EDA Consortium (Electronic Design Automation Companies).

PHYSICAL AND ELECTRICAL DESIGN, MODELING, AND ESTIMATION

Paper 6.1: *Area Optimization of VLSI Power/Ground Networks Via Sequence of Linear Programmings*

Authors: Xiangdong Tan, C.J. Richard Shi, Dragos Lungeanu
Affiliation: Univ. of Washington, Seattle, WA

Authors: Jyh-Chwen Frank Lee, Li-Pen Yuan
Affiliation: Avant! Corp., Fremont, CA

LOGIC-LEVELTESTING, SIMULATION, AND SYNTHESIS

Paper 42.2: *Improving the Test Quality for Scan-Based BIST Using a General Test Application Scheme*

Authors: Huan-Chih Tsai, Kwang-Ting Cheng
Affiliation: Univ. of California, Santa Barbara, CA,Bell Labs.

Author: Sudipta Bhawmik
Affiliation: Lucent Technology, Princeton, NJ

HIGH-LEVEL SYNTHESIS, VERIFICATION, AND CO-DESIGN

Paper 18.1: "Coverage Estimation for Symbolic Model Checking"

Authors: Yatin V. Hoskote, Timothy Kam, Xudong Zhao
Affiliation: Intel Corp., Hillsboro, OR

Author: Pei-Hsin Ho
Affiliation: Synopsys, Inc., Beaverton, OR

DESIGN METHODOLOGY

System Level Design Methodology

Paper 4.1: *Common Case Computation: A High Level Power Optimization Technique*

Authors: Ganesh Lakshminarayana, Anand Raghunathan
Affiliation: NEC USA, Princeton, NJ

Authors: Sujit Dey, Kamal S. Khouri
Affiliation: Princeton Univ., Princeton, NJ

Author: Niraj K. Jha
Affiliation: Univ. of California at San Diego, La Jolla, CA

Technology Driven Design Methodology

Paper 28.1: *Reducing Cross Coupling Among Interconnect Wires in Deep Sub-Micron Datapath Design*

Author: Joon-Seo Yim
Affiliation: LG CIT, Seoul, Korea

Author: Chong-Min Kyung
Affiliation: KAIST, Taejon, Korea

Advancement in Computer Science and Electrical Engineering Undergraduate Scholarships

The objective of the ACSEE Scholarship program is to increase the pool of professionals in Electrical Engineering and Computer Science from under-represented groups (Women, African American, Hispanic, Native American, and Physically Challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provides the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two $4000 scholarships renewable up to 5 years to graduating high school seniors. In 1999 the IEEE Circuits and Systems Society also sponsored one scholarship.

The 1999 winners will be announced at the Conference. The 1998 winners were:

1998 DAC ACSEE Undergraduate Scholarships

DAC $4K: Rashadd Hines, Chicago, IL - attending Howard Univ.

DAC $4K: Brian Kevin McCabe, Holbrook, AZ - attending Arizona State Univ.

For more information about the ACSEE Scholarship, please contact Dr. Cherrice Traver, EE/CS Department, Union College, Schenectady, NY 12308 email: traverc@doc.union.edu.

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Information on next year's DAC scholarship award program will be available on the DAC World Wide Web page at: http://www.dac.com, under general information and the 37th DAC scholarship program.

Design Automation Conference Graduate Scholarship Awards

- Prof. John Lillis of the University of Illinois, Chicago, IL, for Sung-Woo Hur and Ashok Jagannathan. Their project is entitled, *New Techniques for Timing-Driven Placement.*
- Prof. Miodrag M. Potkonjak of the University of California, Los Angeles, CA, for Darko Kirovski and Gang Qu. Their project is entitled, *Intellectual Property Protection for VLSI CAD.*
- Prof. Srinivas Katkoori of the University of South Florida, Tampa, FL, for Stelian Alupoaei and Udaykumar Anumalachetty. Their project is entitled, *RT-Level Route-and-Place Design Methodology for Delay and Power Optimization in DSM Regime*.

Design Automation Conference Graduate Scholarship Committee

The 1999 DAC Scholarship Committee was comprised of the following people:

James P. Cohoon, University of Virginia (Chair)
Michael Lightner, University of Colorado
Sylvia Nessan, Synopsys, Inc.

OPENING KEYNOTE ADDRESS

Paul Otellini
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March of Technology

Technology continues to progress at an ever-increasing rate. Semiconductor advancements and computing platforms are being introduced according to Moore's Law and delivering exciting new capabilities for the entire computer and electronics industry. The cornerstone for these platform solutions from basic computing to high performance workstations and servers is rapidly becoming Intel Architecture.

Paul Otellini will provide insight into trends impacting the computing industry and specifically design automation. Mr. Otellini will discuss the challenges facing designers in their quest to stretch the laws of physics, how Intel is taking on that challenge, and demonstrate solutions powered by new and compelling technology.

Paul Otellini is Executive Vice President of the Intel Architecture Business Group. He is responsible for Intel's computing business units, including the Desktop Products Group, Workstation Products Group, the Mobile and Handheld Products Group, the Enterprise Server Group, Home Products Group, and Reseller Products Group. These organizations together represent Intel's product development and marketing activities around the Intel Architecture set of microprocessors.

THURSDAY KEYNOTE ADDRESS

Aart de Geus
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Chief Executive Officer, Synopsys, Inc.
Mountain View, CA

EDA to the Rescue of System on a Chip

Silicon capacity has doubled every 18 months and will continue to do so for some time. While spiraling gate counts allow designers to pack more and more functions onto a single piece of silicon, they also highlight our inability to keep up with such staggering complexity. The good news is that EDA technology will be the enabler for designers who want to take advantage of this increasing silicon capacity. This presentation will outline the specific challenges facing the EDA industry and its customers in the coming years - as well as predictions for the solutions that will be adopted.

Dr. Aart J. de Geus is Chairman and CEO of Synopsys, Inc. Since co-founding Synopsys in 1986, Dr. de Geus has grown the company from a start-up focused on breakthrough synthesis technology to an international EDA market leader with over 2,900 employees. Today, Synopsys is focused on delivering a complete line of best-in-class EDA software, technologies, intellectual property reuse, and consulting services necessary to succeed in the era of deep submicron and system-on-a-chip design.

Dr. de Geus is considered one of the leading experts worldwide in electronic design automation and frequently speaks on the direction of the EDA industry and its technology. In April 1998, Dr. de Geus was elected Chairman of the Board of the EDA Consortium. Dr. de Geus has also served on the Board of Governors of the IEEE Circuits and Systems Group and as Chairman of the Computer and Network Design (CANDE) group. For his many achievements in the field of electronics, Dr. de Geus was made a Fellow of the Institute of Electrical and Electronics Engineers in January 1999. He holds an M.S.E.E. from the Swiss Federal Polytechnical Institute and a Ph.D. in electrical engineering from Southern Methodist University.

REVIEWERS

A total of 390 manuscripts were submitted to the 1999 DAC. The Conference Executive and Technical Program Committees wish to acknowledge the time and effort spent by the following people who reviewed these manuscripts and returned the review forms completed. Our thanks to all of those who participated and contributed to the success of the Conference.

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CALL FOR PAPERS

37th DESIGN AUTOMATION CONFERENCE®

Los Angeles Convention Center, Los Angeles, CA•June 5 - 9, 2000

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Five types of submissions are invited: regular papers, special topic sessions, panels, tutorials, and design contest entries. All types of submissions should be submitted electronically to: www.dac.com **NO later than October 29, 1999**.

TOPICS OF INTEREST

Authors are invited to submit original technical papers describing recent and novel research or engineering developments in all areas of design automation. Topics of interest include, but are not limited to:

DESIGN TOOLS TRACK:

The Design Tools track (T) is devoted to contributions to the research and development of design tools and the supporting algorithms.

T0.1 Fundamental CAD Algorithms, e.g., BDDs, graph coloring, partitioning
T1.1 Electrical-level circuit and timing simulation
T1.2 Discrete simulation
T1.3 Critical path analysis and timing verification
T1.4 Power estimation
T2.1 Testing, fault modeling and simulation, TPG, test validation and DFT
T2.2 Design and implementation verification (excluding layout verification)
T3.1 Floorplanning and placement
T3.2 Global and detailed routing
T3.3 Module generation and compaction, transistor sizing and cell library optimization, layout verification
T4.1 Technology independent, combinational logic synthesis
T4.2 Technology dependent logic synthesis, library mapping, interactions between logic design and layout
T4.3 Sequential and asynchronous logic synthesis and optimization
T4.4 High-level synthesis
T5.1 Interconnect and packaging modeling and extraction
T5.2 Signal integrity and reliability analysis
T5.3 Analog and mixed-signal design tools and RF
T5.4 Microsensor and microactuator design tools
T5.5 Statistical design and yield maximization
T6.1 Frameworks, intertool communication, WWW-based tools and databases

DESIGN METHODS TRACK:

The Design Methods track (M) deals with innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art designs. Submissions for this track will be judged on how effectively they teach new art in the development and application of new tools and techniques to real-world design problems.

Design methodologies and case studies for specific design tasks

M1.1 Design entry and specification
M1.2 Simulation, analysis, modeling and estimation
M1.3 Verification, test and debugging
M1.4 Physical design, module generation, design for manufacturing
M1.5 Logic and high-level synthesis and optimization

Design methodologies and case studies for specific application domains and platforms

M2.1 Configurable computing, FPGA and rapid prototyping
M2.2 Large heterogeneous systems
M2.3 Microprocessor and multiprocessor
M2.4 DSP, data-paths, multimedia and communication
M2.5 Wireless and data networking
M2.6 Other (MCM, optical, consumer)

Performance and technology driven design techniques

M3.1 Deep sub-micron: signal integrity, interconnect and modeling
M3.2 High-performance design: timing, clocking and power distribution
M3.3 Low power design
M3.4 Mixed-signal, analog, and RF
M3.5 Process technology development, extraction, modeling
M3.6 Other (MEMS, sensors, new devices)

Integration and management of DA systems

M4.1 Management of DA systems, design interfaces, standards
M4.2 Distributed, networked, and collaborative design
M4.3 Intellectual property, design re-use and design libraries

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EMBEDDED SYSTEMS TOPICS:

Embedded Systems are characterized by mixed hardware and software components with limited processing, I/O and storage resources. The increasing role played by software components and their associated support introduces a host of new system design issues. To focus on these, the 37th DAC will have embedded systems sessions covering both the "tools" and the "methods" aspects of the following topics:

E1 Embedded Systems Hardware: system-on-a-chip, IP re-use
E2 Embedded Systems Software: run-time schedulers, middleware, compilers
E3 HW/SW Codesign: specification languages, interfaces and integration, partitioning, synthesis
E4 Validation: debug, performance estimation and analysis, co-simulation
E5 Applications: application-architecture interaction, networked and distributed systems, multimedia systems

REQUIREMENTS FOR SUBMISSIONS

New this Year: DAC Submissions must be made electronically. Reference the DAC web page for instructions on electronic submissions.

Be prepared to submit 2 files: 1) a paper abstract of approximately 60 words. 2) the paper itself of no more than 4000 words. Both should be submitted in PDF or Postscript format (preferably PDF)

In addition one hard copy of the manuscript must also be submitted, with a cover page specifying:

- Name, affiliation, and complete address for each author
- A designated contact person including his/her phone #, fax #, and email address
- A designated presenter, should the paper be accepted
- A list of topic numbers preceded by the letter T (Tools Track), M (Methods Track), or E (Embedded Systems Topic) ordered by relevancy, most clearly matching the content of the paper
- The following signed statement: "*All appropriate organizational approvals for the publication of this paper have been obtained. If accepted, the author(s) will prepare the final manuscript in time for inclusion in the Conference Proceedings and will present the paper at the Conference*".

To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript or abstract. The papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Notice of acceptance will be mailed to the contact person by February 18, 2000. Authors of accepted papers must sign a copyright release form.

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PANELS, TUTORIALS, SPECIAL TOPICS

Proposals should not exceed two pages in length and should describe the topic and intended audience. They must include a list of all participants, including the moderator for panels.

Special Topic Sessions may be either independent papers with a common theme or a set of closely related papers describing an overall system. In both cases, independent reviews of each paper and evaluation of the session as a whole will be used to select sessions. Proposals for Special Topic Sessions should be submitted along with the list of papers to be included in the session and should describe the session's theme. **These proposals and paper submissions must be electronically submitted no later than October 29, 1999**.

UNIVERSITY DESIGN CONTEST

Submissions of original electronic designs (circuit or system), developed at universities and research organizations after June 1998 and resulting in operational implementations are invited. Submissions should contain the title of the project, a 60-word abstract and a complete description of the design, not exceeding 4000 words in text. The submission should clarify the originality, distinguishing features, and the measured performance metrics of the design. Proof-of-implementation in the form of die or board photographs and measurement data is a must. Submitted designs should not have received awards in other contests. Submissions will be reviewed by a special committee of experts. Selected designs will be presented and exhibited at the conference.

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