Local Optimality Theory in VLSI Channel Routing: Composite Cyclic Vertical Constraints

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Abstract

Local Optimality paradigm is applicable to all combinatorial optimization problems. Its direct field of application are the constructive solution algorithm; its main advantage is the low computational cost for multiple high quality initial solutions for iterative improvement algorithms. The application of the paradigm to the VLSI channel routing has necessitated the creation of new knowledge represented by the theory of locally optimal breaking (LOB) of directed circuits (DC) in the vertical constraint graph. Existing theory has supported deterministic polynomial time algorithms for LOB of two classes of directed circuits, the classes of vertex disjoint DC's, and of couples of connected DC's. The new LOB theory supports algorithms for more complex classes of any number of DC's sharing a single vertex and of a uniform lattices of DC's. It is significant that the new theory relies on theory for couples of connected DC's for breaking more complex structures of connected DC's

1. Introduction

Channel routing is the most important detailed routing technique in VLSI design. While many researchers consider its algorithmic aspect to be an overworked field, the theoretical aspect is covered by a comparatively modest number of fundamental results, which mainly concern NP-completeness of the problem and the bounds on channel width; some results applicable to routing decisions can be found in [1,2,3]. This paper presents contributions to the theory of locally optimal breaking of cyclic vertical constraints (CVC) [4,5,6,7,8].

Vertical constraints are the main obstacle to achieving optimal results in channel routing. The original Left Edge algorithm of Hashimoto and Stevens was proven conditionally optimal for channels without vertical constraints; while the problem has been proven NP-complete in the presence of vertical constraints. Directed circuits and directed paths in the vertical constraint graph (VCG) may cause an increase in channel width over the channel density bound. Directed circuits, often referred to as cyclic vertical constraints, present a more difficult problem

to channel routers than the directed paths. Altogether, breaking CVC's is the toughest problem in channel routing, for which little theory has been developed, and no deterministic algorithmic techniques have been published that guarantee a degree of optimality.

Due to the NP-completeness of the problem, globally optimal channel routing is not likely to be guaranteed by any algorithm. The local optimality concept has been introduced to support what can be achieved deterministically towards the goal of optimality. The concept relies on theory which is based on a new VCG augmented by geometric concepts[4]. The new VCG has been proven to be a complete description of the vertical constraint structure, as opposed to the classical VCG.

The basic theory of locally optimal breaking of cyclic vertical constraints is the necessary knowledge base for appling the Local Optimality Paradigm. The basic theory of LOB was developed for vertex disjoint DC's [4], and followed by the theory for couples of DC's which share a single common vertex, or a single common path [5]. The LOB theory for sets of n DC's which share a single common path was presented in [6] along with the theory for a class of outer planar DC structures. The contribution of this paper is the LOB theory for sets of n DC's which share a single common vertex, and for a class of outer planar directed circuit structures which was not treated in [6].

2. Definitions

The weighted VCG $G_W(V_W, E_W, W_W)$ has been defined in [4] as an extension of the classical VCG: its edge set E_W contains a distinct edge for every column that induces a vertical constraint, and it includes a set of edge weights W_W which are equal to the order numbers of the channel grid columns that induce the edges. Graphical representations of G_W in this paper have the edge weights indicated next to the edges. *Secondary vertical constraints* were first recognized in [1,3], but were not conceptually differentiated from the commonly known, *primary* vertical constraints. They are induced by the geometry of terminals and the geometry of routing: at a column that contains signal net terminals, but

does not contain a terminal of the net whose vertical wire segment is placed at the column. A *terminal column* of a signal net is a column that contains a terminal of the net. *Terminal column track switching*, often referred to as terminal dogleging, places the switching jog in a terminal column of the switching net; its virtue, that it does not induce secondary vertical constraints, and therefore can not create secondary directed circuits has been recognized in [1,3]. The net set N_{Ci} of a DC $C_i(V_{Ci},E_{Ci},W_{Ci}) \subseteq G_W$ is the set of nets represented by the vertices in V_{Ci}. The *column interval* Q_{Ci} of a DC C_i is the set of columns $Q_{Ci}=\{q_k|$ $minw_j \in W_{Ci} \leq q_k \leq maxw_j \in W_{Ci}\}$. The *tight set of DC's* is a set of DC's whose column interval contains only columns that induce vertical constraints represented by the edges of the DC's. A *tight channel* is one whose every column belongs to the column intervals of tight sets of DC's. The tightness concept for DC's was introduced in [2]. *Breaking a cyclic vertical constraint* is the ensemble of all routing decisions that must be taken in the process of avoiding a violation of a set of CVC's.

3. The Local Optimality Paradigm applied to channel routing

The idea of the Local Optimality Paradigm is to construct global solutions of NP-complete combinatorial optimization problems by combining locally optimal partial solutions which can be in turn constructed and combined in polynomial time. Implementation of the idea puts a collection of design automation tools into the hands of designers of complex technical systems, enabling them to construct in polynomial time near optimal global solutions to NP-complete combinatorial optimization problems. End benefits of the application of the paradigm are shorter time to market and improved quality of designed products.

The paradigm is implemented by first identifying non trivial subsets of design elements for which provably optimal designs can be constructed in polynomial time. Construction of such partial solutions is followed by a final heuristic step, which combines the design solutions for elements which are, with the design solutions for elements which are not included in the locally optimal partial solutions. In particular, in the VLSI channel routing problem the locally optimal partial solutions are complete routings of selected groups of signal nets. The merit of the Local Optimality Paradigm stems from the fact that it is highly unlikely that a globally optimal solution of a problem will be composed entirely of non optimal partial solutions; more likely, locally optimal partial solutions will be essential ingredients of globally optimal solutions.

In the notion of the local optimality paradigm, the word *local* does not apply to the search space. Rather it applies to the collection of elements (features) of the design problem that the algorithm has to manipulate so that they assume some mutual relations which are considered optimal by the definition of the problem. The locality refers to the fact that the optimal mutual relations are local to independently selected individual subsets of features of a problem instance.

For the local optimality paradigm to be effective, the selection of subsets which are treated separately must be tailored to the particular characteristics of each individual combinatorial optimization problem. The mutual relations derived by a locally optimal algorithm are made optimal with respect to a set of problem specific characteristics, which we shall call the *criteria of local optimality*.

Consequently, the application of the local optimality paradigm to a specific combinatorial optimization problem requires that two sets of criteria be derived in a problem specific manner,

- the criteria for selecting the subsets of problem features to which the local optimization will be applied,
- the conditions of local optimality that must be fulfilled by the mutual relations between the problem features of selected subsets.

Those criteria tailor the paradigm to an individual problem by using either already available, or newly created problem specific knowledge in a provably best way. In the case of the VLSI Channel Routing, new problem specific knowledge had to be created, and a part of it is reported in this paper.

The set of features manipulated in the VLSI Channel Routing problem is the set of wire segments of signal nets in the channel. Based on the current state of the research, the best criteria for selecting the subsets of signal nets whose routing will be locally optimized are defined by relying on the vertical and horizontal constraint structures of the channel. In the domain of vertical constraints, the so far identified criteria for selecting the subsets of signal nets are the following two

- the set of nets involved in a set of cyclic vertical constraints,
- the set of nets involved in a long directed path in the vertical constraint graph,

The local optimality conditions need to be defined separately for each of the selection criterions. This is under investigation for the second of the above two selection criteria, and has been completed for the first of them by the following definition of the Locally Optimal Breaking (LOB) of cyclic vertical constraints, which are represented by directed circuits in the vertical constraint graph.

Locally optimal breaking of a set of directed circuits $C_N=\{C_1,C_2,...,C_n\}$, $C_N \subseteq G_v$, is the ensemble of routing decisions that specify the horizontal and vertical routing of

the nets involved in all DC's $C_i \in C_N$ in such a way that:

(a) the total number of track-switching used in the process of breaking all DC's in C_N, and all secondary DC's created in the process is minimized,

(b) the observable negative effect of the routing of the nets in N_{C_N} on the flexibility of routing of the nets not in N_{C_N} is minimized;

(c) all nets involved in C_N are routed without violations of vertical and horizontal constraints.

Conditions (a) and (c) are self explanatory. Condition (b) implies that when two breaking patterns exist that use the same minimum number of track switching, and pattern A creates a secondary vertical constraint, while pattern B does not create a secondary vertical constraint, pattern A is not a LOB pattern. A more detailed explanation follows.

When a breaking of a set of DC's creates a secondary vertical constraint, the increase in the number of vertical constraints makes the routing of the remaining nets less flexible than it was before the breaking. Consequently, such a breaking can not be considered a locally optimal breaking if there exists another breaking which uses the same number of track switching but does not reduce the remaining flexibility by creating additional vertical constraints.

The argument in favor of the condition (b) is illustrated by the example of a channel whose VCG contains a couple of directed circuits which share a single vertex. Figure 1(a) shows a routing of the channel obtained by applying the double switching breaking pattern to the couple of DC's. In that routing, the common net $N_s=3$ has been switched twice in its terminal columns 2 and 5, having not created any secondary vertical constraints. Figure 1(c) shows a routing of the channel in which the single switching breaking pattern has been applied. The placement of the switching jog at column 7 has induced a secondary vertical constraint which in turn closes a secondary directed circuit. The secondary directed circuit had to be broken by an additional switching of the net $N_s=3$, whereby the total number of track switching has been brought up to two, equalling eventually the number of track switching in the routing of Figure 1(a).

In the routing of Figure 1(a), where a secondary vertical constraint has not been induced, the horizontal wire segment of net 6 could have been placed on any track above the track which carries the segment of net 2. In the routing of Figure 1(c), where a secondary vertical constraint has been created, the horizontal wire segment of net 6 is additionally restricted to being placed on a track located below the track which carries the lower placed segment of the switching net; which leaves no options - net 6 must be placed on a track between the tracks which carry nets 2 and 3. In the latter case, the flexibility in placing net 6 has been completely lost.

With regard to the total number of track switching both routings in Figure 1 are equal. The crucial disadvantage of
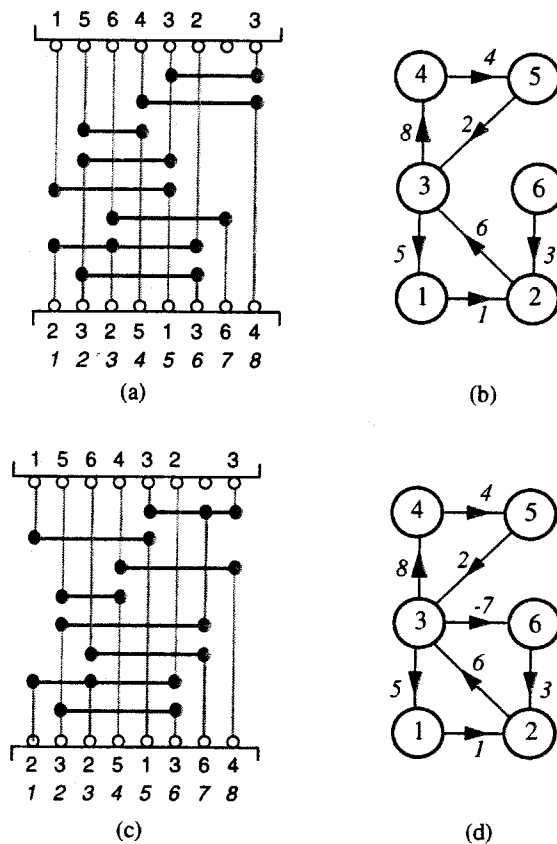
Figure 1 Illustration in support of the condition (b) of the definition of LOB of a set of directed circuits (a)The double switching breaking pattern applies two track switchings and does not create a secondary vertical constraint. (b)G_W of the channel. (c)The single switching breaking pattern applies one track switchings and creates a secondary directed circuit which must be broken by a second track switching (d)G_{WS} of the channel as routed in (c).

the routing in Figure 1(c) is that the induced secondary vertical constraint forces net 6 to be placed on a track located below the track which carries the lower horizontal segment of the switching net 3. In the channel of Figure 1 that loss of flexibility has not made a difference because there do not exist other nets with which net 6 is horizontally or vertically constrained. But in the case of a channel which contains more nets, and whose VCG contains the VCG of Figure 1(b) as a subgraph, the secondary vertical constraint between the nets 3 and 6 could prevent a globally optimal placement of net 6, which would be otherwise possible if the routing pattern of Figure 1(a) had been applied.

Deterministic, polynomial time methods for locally optimal breaking of DC's allow a shift in the level of heuristic decision making, from the low level routing decisions concerning a single signal net, or a geometrically not clearly related group of nets, to a higher level where

groups of locally optimally routed nets involved in composite vertical constraints are combined. The deterministic nature of the LOB procedures provides the important low cost quality to the locally optimal partial solutions.

LOB of directed circuits and long directed paths in the VCG has potential in automatic and interactive DA systems. In interactive systems, designers can be presented with graphical representations of available locally optimal routings, allowing them to use human intuition for selecting the most promising combinations. For automatic routers, a bounded search space of available alternative locally optimal partial routings lends itself to efficient search using parallel computer architecture. As a demonstration of that kind of application, LOB theory has already been successfully implemented in the first of their kind Genetic, and Neural Network channel routers which allow the existence of directed circuits in the VCG of the channel [7,8]. All iterative improvement algorithms for solving combinatorial optimization problems shoud benefit from initial solutions created by the application of the local optimality paradigm. This includes the inherently sequential simulated annealing, which produces good quality solutions but critically depends on high quality initial solutions for shortening its long run times.

4. New LOB theory

To demonstrate that a locally optimal breaking of sets of connected DC's always exists, we consider in the sequel the worst case scenarios characterized by channels being tight, which requires application of the double switching breaking pattern. In non tight channels, the single switching breaking pattern may require one track switching less than the double switching pattern.

4.1 Breaking any number of directed circuits which share a single common vertex

It will be shown that LOB of a set of n DC's which share a common vertex relies on already developed results for couples of connected DC's, and that it does so in such a way that the corresponding DA tools are reusable.

Theorem 1 establishes the rules for LOB of a set of n DC's which share a common vertex.

Theorem 1: When the vertical constraint graph G_W of a tight channel contains a set of n DC's $C_N=\{C_1,C_2,...,C_n\}$ which share a single common vertex v_s, $C_1 \cap C_2 \cap ... \cap C_n = (\{v_s\},\varnothing,\varnothing)$, all n DC's will be locally optimally broken if:

- the algorithm for LOB of two DC's with a single common vertex is applied to an arbitrary couple of DC's $C_j,C_k \in C_N$,

- nets belonging to the remaining n-2 DC's in C_N are placed on tracks observing horizontal constraints, and following the order of their vertices within the paths which are left when vertex v_s is deleted from those DC's; they must be placed on any of the existing tracks in the track set T_{jk} which carries the nets in C_j and C_k, or on tracks additionally inserted into T_{jk} anywhere between its outermost tracks.

Proof: For $n \leq 2$ the proof is given in [4,5]; for $n>2$, the application of rules of Theorem 1 results in:

(a) C_j and C_k have been broken in a locally optimal way by routing the common net N_s on the topmost and the bottom most track in T_{jk}; this breaks any DC $C_i \in C_N$ whose nets are placed on tracks between the outermost tracks of T_{jk}; so no more switching is needed for breaking the rest of the DC's in C_N;

(b) breaking C_j and C_k has not placed a switching jog into any of the columns that induce the rest of n-2 DC's of C_N, so no secondary vertical constraints could have been created between the nets in C_j and C_k and the nets in other DC's of C_N;

(c) except for the common net N_s, nets involved in any DC $C_i \in C_N$ are not in a vertical constraint relation with the nets in other DC's of C_N;

(d) by the virtue of (b) and (c) no vertical constraint violations are possible between two nets from two different DC's of C_N, ergo the freedom in selecting the tracks for placing the nets involved in remaining n-2 DC's.QED

The problem of minimizing the number of tracks used for placing the nets in the remaining n-2 DC's is likely to stay NP-complete due to the freedom referred to under (d), although a part of their routing has already been decided by the LOB procedure: the ordering of nets on tracks is determined within DC's, and the nets in all DC's must be routed within the contiguous set of tracks T_{jk}.
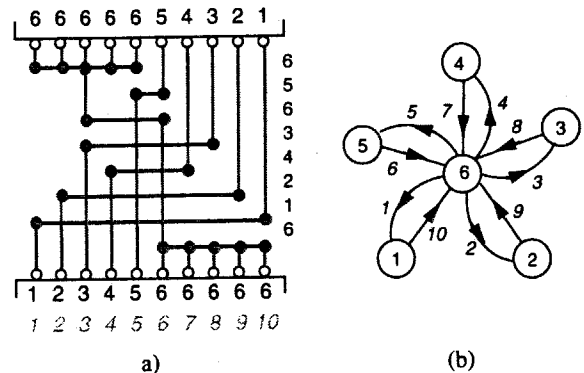
Figure 2: Tight channel with five DC's sharing a common vertex. (a)One of LOB's. (b)G_W of the channel.

Application of the LOB procedure of Theorem 1 is illustrated in Figure 2 on a case of a tight channel with five DC's in its VCG G_w, which share a common vertex $v_s=6$. The LOB algorithm for a couple of DC's sharing a common vertex [5] has been applied to DC's containing vertices $v_j=3$ and $v_k=5$. It should be observed that horizontal routing of nets 1,2, and 4 could have been alternatively placed onto any of the tracks located between the two outermost tracks that carry the horizontal segments of the switching net 6.

4.2 Breaking directed circuits of a uniform ladder VCG

We call a *uniform ladder graph* a digraph G characterized by the following:

(a) the underlying undirected graph of G is an outer planar graph,

(b) in the planar embedding of G in which the longest face is represented by the external contour, all faces of G, except the longest one, are of the same length.

The faces of the planar imbedding defined under (b), except for the longest face, will be called *internal faces*.

Ladder graphs are partitioned into two classes by the property that they do, or do not, contain a DC whose edges coincide with the longest face. We call the former *l-class* and the latter *n-class* ladder graphs. The theory of LOB of *l-class* ladder graphs has been presented in [6]; we consider here the *i-class* to which those n-class ladder graphs belong in which the edges of every internal face form a DC.

A maximal i-class subgraph of a ladder graph G is one which:

- is not a proper subgraph of another i-class subgraph of G, and

- does not contain a face which belongs to a maximal l-class subgraph of G,

where a *maximal l-class subgraph* of G is an l-class ladder subgraph which is not a proper subgraph of another l-class subgraph of G.

Since maximal l- and i-class subgraphs consist of sequences of adjacent internal faces they are ladder graphs themselves. A ladder graph G isomorphic with its maximal l-class/i-class subgraph, will be called L-ladder/I-ladder graph. Precedence of the l-class over the i-class maximality property, established by the second property of the maximal i-class subgraphs, is arbitrary but seems to be justified by the greater power of LOB procedures for L-ladder DC's. For an I-ladder graph with n_f internal faces LOB can at best reduce the number of necessary track switching to one half of n_f, while for L-ladder graphs one half of n_f is the worst case [6].

It is obvious that every DC of a ladder graph G belongs to a single L-class or I-class subgraph of G, and that all

edges of those subgraphs belong to a DC. It, therefore, follows that all DC's of a ladder VCG can be broken by breaking separately DC's of each of its L-ladder and I-ladder subgraphs. Consequently, what is needed for LOB of DC's in a ladder subgraph of a VCG G_w is, to know how to break all DC's of L-ladder and I-ladder subgraphs of G_w. The theory of LOB of DC's of L-ladder subgraphs of G_w has been presented in [6]; this paper completes the theory of LOB of DC's of uniform ladder subgraphs of G_w by discussing the I-ladder subgraphs.

Consistent with Section 4.1, we consider tight channels whose VCG is a uniform I-ladder graph with internal faces of length three.

Theorem 2 details how all DC's of an I-ladder VCG containing four or three DC's can be broken by an extension of the LOB theory for a couple of connected DC's. When an I-ladder block of a VCG contains more than four DC's, it requires separate treatment of I-ladder subgraphs which contain four or less DC's. When such a procedure results in a subgraph with less than three DC's, the existing LOB theory for those cases applies [4,5].

Theorem 2 In a tight channel whose I-ladder VCG G_w contains four DC's of length-three, C_i,C_j,C_k,C_l in that order of adjacency, all four DC's will be LO broken by only two nets switching tracks, each net one time, if:

(a) two directed Euler trails, E_1 and E_2, of $C_j \cup C_k$ are determined by the procedure for LOB of a couple of DC's which share a common path [5];

(b) that one of E_1 and E_2 becomes the selected trail E_S whose second vertex has in its incidence set an out-directed edge that belongs to C_i or C_l but does not belong to C_j or C_k [in Fig.2(b), vertex 2 has edge (2,1) in C_i, so the selected Euler trail's vertex sequence is $V_{ES}=(3,2,4,3,5,4)$];

(c) a new vertex sequence V_{EA} is constructed by augmenting V_{ES} by the two vertices of G_w which are not covered by the trail E_S, as follows:

- the vertex that belongs to that one of C_i and C_l which contains the first edge of the trail is inserted after the second vertex of the trail and before the second occurrence of the first vertex of the trail [in Fig.2, vertex 1 is inserted after vertex 2 and before the second occurrence of vertex 3],

- the other vertex is inserted between the third and the fifth vertex of the trail;

(d) nets are placed on a contiguous set of tracks T_{jk} in the order of appearance of their vertices in the sequence V_{EA} [vertex sequence V_{EA} is shown next to the routing of Fig.2(a)].

Proof: Two centrally located DC's of a four-DC ladder VCG, C_j and C_k, are locally optimally broken because

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application of the LOB procedure for a couple of DC's produces the vertex sequence V_{ES} whose mutual order of vertices is kept unchanged in V_{EA}. The nets switched to break C_j and C_k belong to both C_i and C_l, so their switching provides for breaking of C_i and C_l. Part (c) determines the placement of two remaining nets on tracks so that violation of vertical constraints is avoided. In the case of a three-DC I-ladder block, steps involving the DC C_l do not apply.

<div align="right">QED</div>

Figure 3 illustrates Theorem 2. All four DC's are broken by only two nets switching tracks. Applying the LOB for a couple of DC's with a single common path produces the selected Euler trail $E_S=(3,2,4,3,5,4)$ [5]. Nets 1 and 6 must be inserted on tracks between the nets 2 and 3, and 4 and 5 respectively. The lower segment of net 3 and the upper segment of net 4 can swap tracks with nets 6 and 1 respectively; so a total of four different LOB's exist for the four-DC I-ladder VCG.
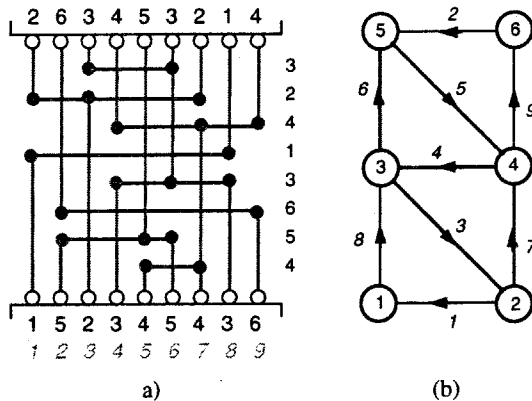
Figure 3: Tight channel with a four-DC I-ladder VCG. (a) One of the channel's LOB routing solutions. (b) G_W of the channel showing in bold lines two DC's to which the two directed circuits with a common path LOB has been applied.

5. Conclusion

The theory of locally optimal breaking of directed circuits in the vertical constraint graph has been developed to provide new knowledge requited for the application of the local optimality paradigm to the channel routing problem. Other results of the theory of locally optimal breaking have been previously published, but the local optimality paradigm is first time described in this paper. The paradigm is applicable to all combinatorial optimization problems. Its direct field of application is in the constructive solution algorithms, which are used to provide initial solutions for iterative improvement algorithms. Its main advantage is in the low computational cost for high quality initial solutions.

Applying known results of the theory of locally optimal breaking of directed circuits in the vertical constraint graph, extensions of the theory have been developed which cover two new general classes of sets C_N of directed circuits in the vertical constraint graph. The class of single-row lattice connected sets is a breakthrough result into sets of connected directed circuits which greatly increases the versatility of the cyclic vertical constraint structures to which the LOB theory has been successfully applied. The low computational cost, and the high quality of the locally optimal partial solutions make them attractive ingredients of the initial solutions for all iterative improvement approaches to VLSI channel routing.

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