A Continuous-Time Switched-Current ΣΔ Modulator with Reduced Loop Delay

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Abstract

A novel architecture for a second-order continuous-time switched-current ΣΔ modulator is presented. The loop delay is reduced by predicting the states of the second integrator and feeding the predicted states to the comparator. The predicted states are generated by summing three scaled current mode signals. A Gain-Manager is used to accurately control the integrator gain to generate the predicted states and stabilize the system. A newly designed high-speed current-mode comparator is capable of summing the three scaled current inputs and comparing them. With a 50 MHz sampling rate, it has achieved 60 dB dynamic range (10-bit) at 1 MHz. The modulator has been fabricated in a 2um CMOS process with an active area of 0.37 mm^2. The power dissipation is 16.6 mW from a 5V single power supply.

1 Introduction

Current research on high-speed low-power A-to-D conversion is mostly focused on high-speed high-order multi-bit switched-capacitor ΣΔ modulators. However, the speed of the switched-capacitor ΣΔ modulator is limited by the settling time of the OPAMP. To reduce the settling time of the OPAMP, the cost of higher power dissipation and larger size must be paid. A multi-bit ΣΔ modulator requires the use of a flash A-to-D converter resulting in increased power dissipation and size of the modulator.

A continuous-time switched-current ΣΔ modulator can operate at high sampling speeds with a lower power consumption. It directly integrates the current on capacitors as shown in figure 1, which eliminates the need of high speed OPAMPs. It also has the advantage of smaller size due to a simplified circuit structure and fewer capacitors. However, continuous-time switched-current ΣΔ modulators suffer from scaling, clock feed-through, and clock jitter problems, which limit their use to lower speed or lower resolution applications[1, 2].

In the past, the integrator gain of a continuous-time switched-current ΣΔ modulator has been determined by the RC time constant of the on-chip resistors and capacitors[2, 3]. This RC time constant is not well controlled due to processing variations of the resistance and capacitance, and therefore leads to gain error of the integrator. This gain error can cause a stability problem and a scaling problem which must be counterbalanced by external compensation [3], otherwise the modulator can only be realized for first-order modulation[2].

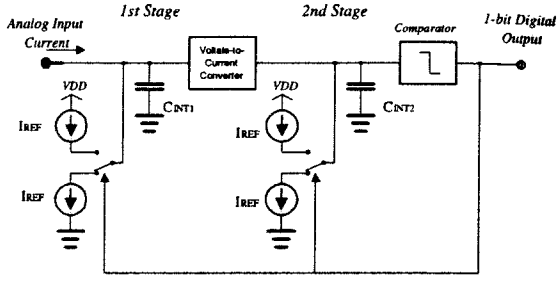

Figure 1: The simplified scheme of a second-order continuous-time switched-current ΣΔ modulator.

In our previous work [4], the clock feed-through problem was successfully solved by newly designed current switches as shown in figure 2. The scaling problem was solved by using a Reference-Current Generator for the second stage. This circuit, implemented in a standard 2um double-metal double-poly CMOS technology, achieved 50dB dynamic range at 1 MHz with a 50MHz clock.

However, this modulator contains an extra loop delay. This delay may cause a stability problem and must be compensated by reducing the loop gain, which degrades the performance of the modulator. The improved design presented in this paper eliminates the delay by new circuit architecture. With predicted "next states" fed to the comparator, the loop delay is compensated without degrading the performance. In the following sections, we will discuss how the delay can be reduced and how the circuit is implemented to achieve this goal.

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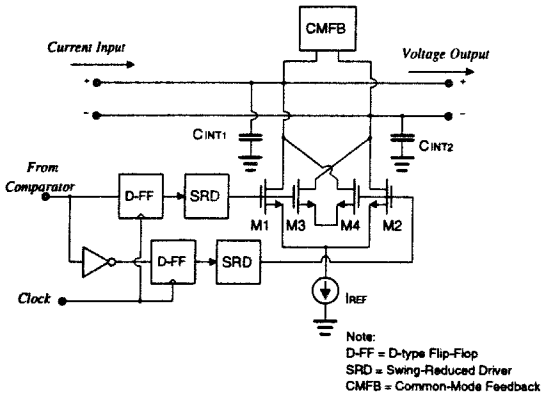

Figure 2: The simplified scheme of the high-speed current switch.

2 Loop Delay in Continuous-Time Switched-Current ΣΔ Modulator

In a switched-current ΣΔ modulator, the comparator (or the A-to-D converter for a multi-bit modulator) does not require extra delay. If the comparator (ADC) can settle into a result within the first half of the clock cycle, the reference voltage will be integrated on the integrator within the second half of the clock. In most SC ΣΔ modulators, the clock speed is limited by the settling time of the OPAMPs, not the comparator, and therefore the extra loop delay does not exist in switched-capacitor ΣΔ modulators.

In continuous-time switched-current ΣΔ modulators, extra loop delay is required for the comparator to settle to a result and for the D-type flip-flops to synchronize the current switches. The synchronization of the current switches is very important since the integration relies on the time interval. This extra delay can cause a stability problem. The integrators tend to be overloaded and cause the modulator to settle into a long period of limit cycle. The stability problem can be solved by reducing the loop gain. However, this will deteriorate the noise-transfer function (NTF) to have less dynamic range and more in-band noise. The extra loop delay also increases the time period of the noise pattern and causes the pattern noise to enter the lower frequency band.

In the previous design [4], the scaling factor between the first and second stage (the integrator gain of the first stage) had to be smaller than 0.5 to avoid the stability problem and even smaller to avoid overload on the integrators and to have a reasonable input range. The scaling factor was set to be 0.25, resulting in an input range within $\pm 0.5 I_{REF}$ and an idle channel (no input) peak output noise of -20dB at 5MHz, which is 1/10 of the clock frequency.

Without the extra loop delay, the upper bound of the scaling factor is 1 (compared with 0.5 for the modulator with extra delay as stated above). The noise transfer function (NTF) is improved by moving the energy of noise toward the higher frequency band, and hence the in-band noise is reduced. A modulator with only one clock cycle loop delay (first-order modulator) should have an idle channel peak output noise at 1/2 of the clock frequency. For an ideal second-order ΣΔ modulator, two delays are required by the two integrators (assuming each integrator requires one clock delay), and accordingly, the idle channel peak output noise should be around 1/4 of the clock frequency.

3 System Architecture

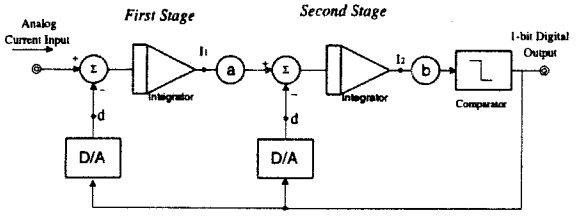

Figure 3: The block diagram of a second-order ΣΔ modulator.

The loop delay can be reduced by feeding the comparator with a predicted "next state". Figure 3 shows the block diagram of a second-order ΣΔ modulator, where **I1**, **I2**, and **d** represent the output of the first integrator, the second integrator, and the D/A respectively, and **a** and **b** represent the scaling factors. Set **b** to be 1 and the next state of the second integrator is

$$I2_{N+1} = I2_N + a \times I1_N - d_N \qquad (1)$$

By feeding this to the comparator, the comparator performs analog-to-digital conversion according to the "next state" of the second integrator. This method reduces the loop delay by 1 clock cycle and hence compensates the delay introduced by the comparator and the D-type flip-flops. The new circuit architecture is shown on figure 4.

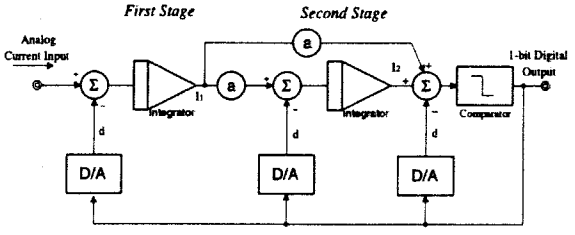

Figure 4: The block diagram of a second-order ΣΔ modulator with reduced delay.

Equation (1) holds true if the first integrator is a discrete-time integrator. However, as the integrator is a continuous-time integrator, the output value is

changing continuously. If the modulator input current, I_{IN}, is a slowly changing signal, as is normally true for $\Sigma\Delta$ modulators, the change at the output of the first integrator within one clock cycle is

$$\Delta I1 = I_{IN} - d \quad (2)$$

The next state of the second integrator should be

$$I2_{N+1} = I2_N + a \times I1_N - d_N + \frac{a}{2} \times \Delta I1 \quad (3)$$

$$I2_{N+1} = I2_N + a \times I1_N - (1 + \frac{a}{2})d_N + \frac{a}{2} \times I_{IN} \quad (4)$$

To achieve the architecture in figure 4, the integrator gains of both the first stage and second stage have to be accurately controlled. In contrast, in the previous work [4], only the integrator gain of the first stage needed to be well controlled, while the gain of the second stage was arbitrary, as it only affected the resolution of the comparator.

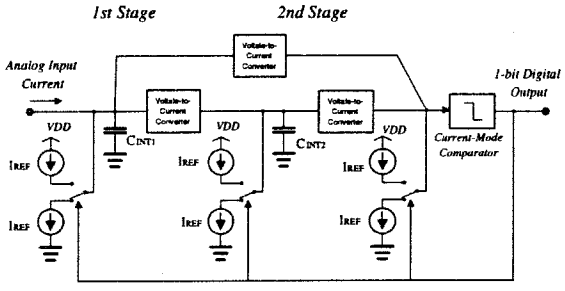

Figure 5: The circuit implementation of a second-order $\Sigma\Delta$ modulator with predicted "next state".

The new architecture can be implemented by introducing two voltage-to-current converters and one D-to-A (current switch) as shown in figure 5. Different scales of the voltage-to-current converter are achieved by sizing the transistors and current sources in the voltage-to-current converter. In this design, the scaling factor a is set to be 0.5 for optimizing the loop stability, the available modulator input range, and the ratios of transistor sizes of the voltage-to-current converters.

The higher order correction terms, $\frac{a}{2} \times d_N$ and $\frac{a}{2} \times I_{IN}$ as shown in equation (4), are not implemented due to the availability of the duplicate of the input current, I_{IN}. The noise transfer function (NTF) is degraded less than 3dB due to the lack of higher order correction terms. However, the system is stabilized with the lack of the correction terms when large input is applied ($I_{IN} \approx \pm I_{REF}$).

To generate the predicted "next state" and the scaling factor correctly, the transconductance gains of the voltage-to-current converters need to be accurately controlled. A Gain-Manager is introduced to control the transconductance gains of all the voltage-to-current converters. The detailed design of each block is presented in the next section.

4 Circuit Design

The proposed new architecture uses a fully differential design to minimize the injected noise from VDD and the environment. Instead of switching between the current source and current sink as shown in figure 5, the current switch architecture switches only one current sink between two capacitors as shown in figure 6. This architecture eliminates the switching time mismatch problem and the parasitic capacitance problem [4, 2, 3]. The details of each building block are described in the following paragraphs.

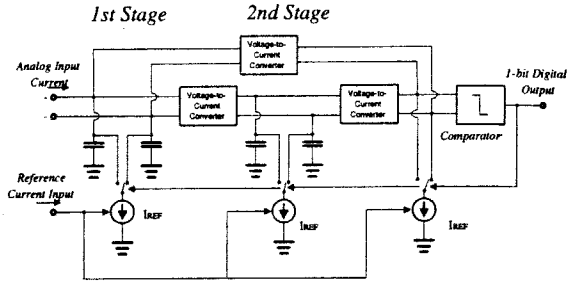

Figure 6: The architecture of the new second-order continuous-time switched-current $\Sigma\Delta$ modulator.

4.1 The Current Switch

The current switch is realized by an NMOS differential pair (M1, M2) as shown in figure 2. D-type flip-flops are used to synchronize the switching with the clock to guarantee each integration is exactly one clock cycle. The Common-Mode Feedback (CMFB) block is a continuous-time common-mode feedback used to stabilize the common-mode voltage.

The Swing-Reduced Drivers are used to reduce the voltage swing on the gates of M1 – M4. This minimizes the clock feedthrough problem and also reduces the charges which are moved into and removed from the gates during the switching. M3 and M4 are two dummy transistors with the same sizes as M1 and M2, and are used to cancel out the feedthrough charges from the gates. From the experiment of the previous work [4], all these blocks have very excellent performance as expected.

4.2 The Voltage-Controlled Voltage-to-Current Converter (VCVCC)

The Voltage-Controlled Voltage-to-Current Converter (VCVCC) is realized by the cross-coupled quad cell [5] shown in figure 7a. The cross-coupled quad cell composed by M1 – M4 is a traditional NMOS cross-coupled quad cell. However, the different common-mode output currents caused by different differential input voltages will cause a stability problem of the common-mode voltages of the integrators. M5 and

M6 are added to solve this problem. Figure 8b shows the complete circuit diagram of the VCVCC. The controlling voltage input ($V_{CONTROL}$) is used to control the transconductance gain of the VCVCC. As the controlling voltage increases, the transconductance gain of VCVCC increases.

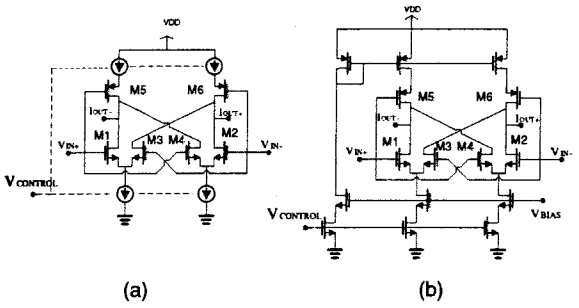

Figure 7: (a) The simplified circuit diagram of the Voltage-Controlled Voltage-to-Current Converter which utilizes the cross-coupled quad cell. (b) The complete circuit diagram of the VCVCC.

To minimize the nonlinear error and gain error of the transconductance gain, the aspect ratio (W/L) is set to M3 = M4 = 5 M1 = 5 M2. From simulation, the nonlinear error and gain error are less than 5% within the whole input range. From system level simulation, a 10% error is tolerable without degrading the performance or introducing any stability problem.

4.3 The Gain Manager

The Gain Manager controls the transconductance gain by integrating the input reference current (I_{REF}) for two clock cycles, holding the current level, comparing the current level with the reference current input, I_{REF}, and then adjusting the transconductance gain. As shown in figure 8, the Voltage-controlled Voltage-to-Current Converter (VCVCC) is identical to all the other VCVCCs in the system. A capacitor is used to memorize (hold) the controlling voltage of the VCVCC. The Gain Manager uses four successive clocked states to complete the task and operates repeatedly. The four states operate in the order S_1, S_2, S_3, S_3, and then back to S_1. Each state is two clock periods long (40ns), and hence, the transconductance gains of the VCVCCs are updated every 160ns.

The function of each state is:

- S_1 : Reset the integrator by shorting C_{INT1} and C_{INT2}.
- S_2: Integrate the input reference current on C_{INT1} and C_{INT2}.
- S_3: Precharge. If point **A** is not precharged, charge sharing will affect the voltage of C_{HOLD}, which may cause an error voltage and increase the time needed for the Gain Manager to converge to the final value. During the precharge state, point **A** is precharged to the voltage level of the last convergence point.
- S_4: Adjust the controlling voltage. During this state, the Gain Manager becomes a closed loop. The Gain Manager adjusts the controlling voltage of VCVCC so that the output current of VCVCC is exactly equal to the input reference current, IREF. After this state, the holding capacitor, C_{HOLD}, will hold this controlling voltage until the next S_4 state.

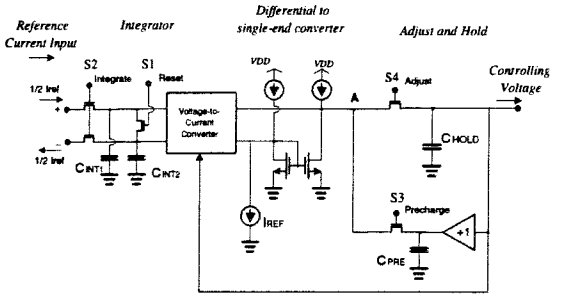

Figure 8: The simplified circuit scheme of the Gain Manager.

4.4 The High-Speed Current-Mode Comparator

The high-speed Current-Mode Comparator is a two stage regenerative comparator [6, 7] as shown in figure 9. The input stage composed by M1 - M8 is a current gain stage. The first regenerative stage is composed by M9 - M12. The second stage is composed by M13 - M16. M17 and M18 are used to precharge points **c** and **d**. M19 is used to reset points **a** and **b**. Φ_1 and Φ_2 are two non-overlapping clocks.

During the clock phase Φ_2 , the comparator is being reset. Point **a** and point **b** are shorted. When Φ_2 drops from VDD to ground, the first stage begins the first regeneration process. When Φ_1 turns high, the second stage starts the second regeneration process. Either point **c** or point **d** will drop to low voltage and trigger the RS latch.

The input stage serves the following purposes,

- Decouples the charge feedback effect caused by the regeneration process (charges feedback from points **a** and **b** to the inputs).
- Guarantees voltages of the two input nodes are within the output range of the VCVCC to have the VCVCCs operate properly.
- Offers a current gain for the two current inputs.

By carefully designing the layout and sizes of transistors, the Current-Mode Comparator has a resolution of 0.05uA with a 50 MHz clock by SPICE simulation. The charge feedback effect has been successfully eliminated. Together with the D-type flip-flops, only one clock delay is required.

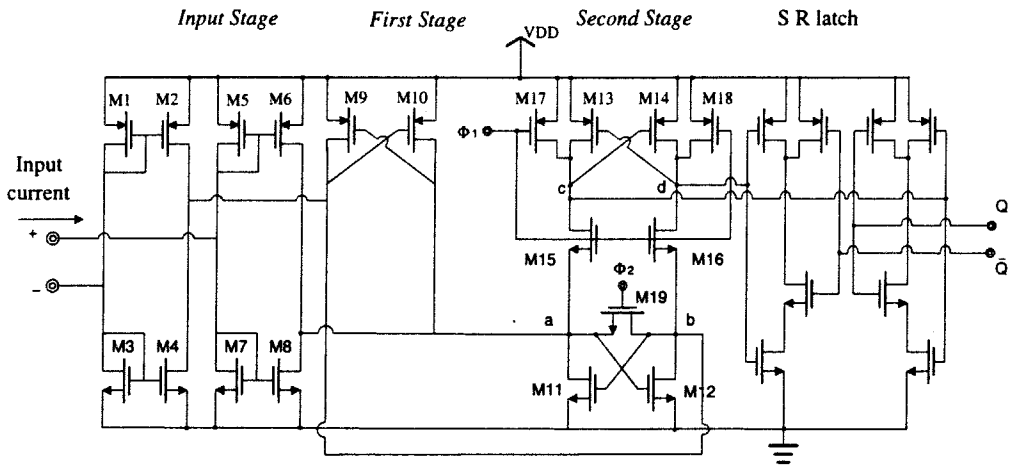

Figure 9: The circuit diagram of the high speed current-mode comparator.

5 Experimental Results

The continuous-time switched-current ΣΔ modulator has been implemented in a standard 2-um N-well double-metal double-poly CMOS technology. Figures 10 shows the microphotograph of the modulator. The size of the active area is $620 \times 600mm^2$. With a single 5 V power supply, a 50 MHz clock, and a 10 uA reference current input, it achieves 60 dB dynamic range in 1 MHz bandwidth. It has achieved 10dB improvement in dynamic range compared to the previous work[4]. The total power dissipation is 16.6 mW and more than 10 mW is dissipated by the digital circuitry. With the use of a more advanced process, the power dissipation of the digital circuitry can be reduced resulting in a much lower power consumption.

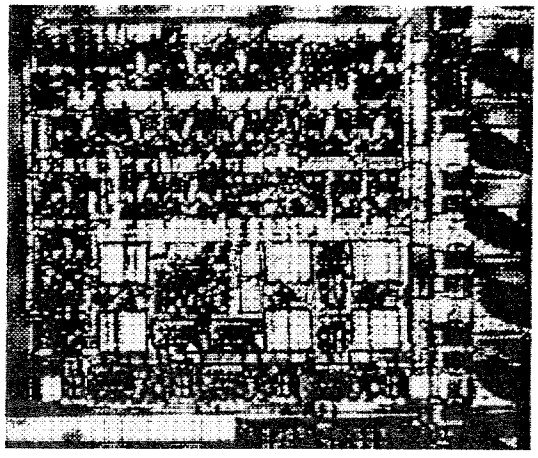

Figure 10: The microphotograph of the second-order continuous-time switched-current ΣΔ modulator.

Figure 11 shows the output spectrum with a 100 KHz input. Compared to the previous work [4], the peak noise moves from 5MHz to 8.3 MHz (from 1/10 of the clock frequency to 1/6 of the clock frequency). The energy of noise is moved to a higher frequency band, reducing the in-band noise in this design.

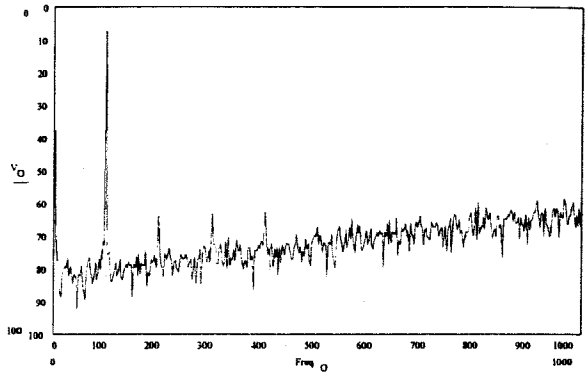

Figure 11: The modulator output spectrum with a 100 KHz sinusoid input.

6 Conclusions

A new architecture of continuous-time switched-current ΣΔ modulator has successfully reduced the loop delay and attained 10dB improvement on the dynamic range compared to previous work. The novel Gain Manager, Voltage-Controlled Voltage-to-Current Converter, and the Current-Mode Comparator allow the continuous-time switched-current ΣΔ modulator to have complex feedback and feed-forward signal

Table 1: The experimental result

	Previous Work [4]	$\Sigma\Delta$ modulator w/ reduced delay
Power supply voltage	5V	5V
Clock frequency	50MHz	50MHz
Signal Bandwidth	1MHz	1MHz
Dynamic range	50 dB	60 dB
Input reference current	10 μA	10 μA
Input current range	$\pm 5\mu$A	$\pm 5\mu$A
Power dissipation	15 mW	16.6 mW
Active area	0.37 mm^2 ($620 \times 600\mu$m)	0.37 mm^2 ($620 \times 600\mu$m)
Technology	2μm CMOS	2μm CMOS

paths, which cannot be achieved in traditional approaches. This new architecture offers a low cost way to realize a high-speed, low-power, and small-sized A-to-D converter. Furthermore, it provides the foundation for building higher-order $\Sigma\Delta$ modulators.

Acknowledgements

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