

Low Voltage Low Power CMOS AGC Circuit for Wireless Communication

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Abstract

This paper describes a new technique for realizing CMOS digitally controlled, dB-linear variable gain amplifier (VGA) circuit. The circuit is developed taking into account system level issues for a direct conversion receiver. Besides being effective and simple to use from a system point of view, the developed VGA offers precise gain control, high linearity and low power consumption. The circuit can operate in a current domain or a voltage domain mode with single ended or fully differential signal handling capability. The proposed VGA circuit is implemented using a novel class AB operational transconductance amplifier and current division networks. Simulation results are included.

1 Introduction

Variable gain amplifier circuits are employed in many applications such as hearing aids [1], disk drives [2] and imaging circuitry in order to maximize the dynamic range of the overall system. A VGA is essentially important in virtually all wireless communication systems [3]. The demand of an automatic gain control (AGC) loop in wireless systems comes from the fact that all communication systems have an unpredictable received power. To buffer receiver electronics from change in input signal strength by producing a known output voltage magnitude, a VGA is typically used in a feedback loop to realize the AGC circuit. To maintain AGC loop settling time which is independent from the signal levels, an exponential gain control characteristic is required [4]. Furthermore, with the recent trend in digital communication, most transceivers employ digital circuitry. Usually the digital part collects and processes data then sends control information to the VGA which adjusts the signal power level prior to A/D conversion. Thus, a digitally controlled VGA circuit will simplify the interface between the analog and digital part of the transceiver. In this paper a digitally controlled CMOS VGA circuit is

described. The presented circuit has a dB-linear gain control characteristic of approximately 25 dBs. This function is realized using a novel pseudo exponential gain implementation. The VGA circuit is designed for use in direct conversion receivers. In section 2, system level design issues for the VGA are presented. The VGA implementation based on a new OTA is given in section 3. Section 4 discusses the simulation results for the proposed VGA circuit.

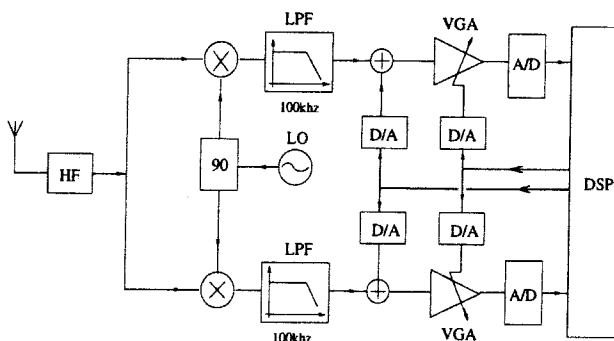


Figure 1: Direct conversion receiver.

2 VGA circuit for direct conversion receivers

Recently, direct conversion receivers have been receiving considerable attention [5]. The advantage of having a zero-IF receiver is obvious; there is no need for high Q HF or IF bandpass filters. Fig.1 shows a block diagram of a zero-IF receiver with dynamic suppression of DC offset. It is clear that the VGA gain is set by the DSP. Where the digital word is converted to an analog voltage which is used to control the dB-linear gain of the VGA. The receiver also employs other D/A converters for DC offset control. The DC offset is one of the major problems in direct conversion receivers. The reason behind this is the fact that the

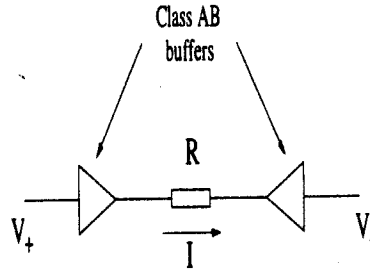


Figure 2: Class-AB OTA operating principle.

DC offset is superimposed on the desired signal in the baseband. It can only be removed by means of a very long time constant control loop. However, with the presence of a DSP in the receiver complex non-linear algorithms which determines the DC level dynamically can be realized. The DC level is converted to an analog quantity then fed back to the baseband circuit. It is clear that a digitally controlled VGA would eliminate the need for one of the D/A converters. The other D/A converter and adder can be removed if the VGA circuit allows digital offset trimming. Another design aspect for the digitally controlled VGA is the resolution of gain control. In communication systems where digital decision thresholds are fixed, the input amplitude to the A/D converter must be set accurately to within one least significant bit. Therefore, high resolution gain control is important for those applications. From yield and silicon area point of view, the precise gain control would be best implemented without component spreading. Therefore, the VGA is required to provide high resolution gain control with minimum component spreading. An advantage of having a zero IF receiver is that the input and output signal to the VGA circuit is at the baseband frequency. The bandwidth requirement of the circuit is thus somewhat relaxed. A circuit with small bandwidth will offer better noise performance as well. Finally, the circuit is required to operate from low supply voltage with a small standby current.

3 The VGA CMOS realization

The proposed VGA circuit is based on an operational transconductance amplifier and current division networks [6]. A new CMOS realization for a class AB OTA is used. The proposed OTA circuit operates in class AB mode for low standby power dissipation and high current driving capability. The circuit operation is illustrated in Fig.2. Two class AB buffers are connected across the two terminals of a resistor. The current flowing through the resistor is given by:

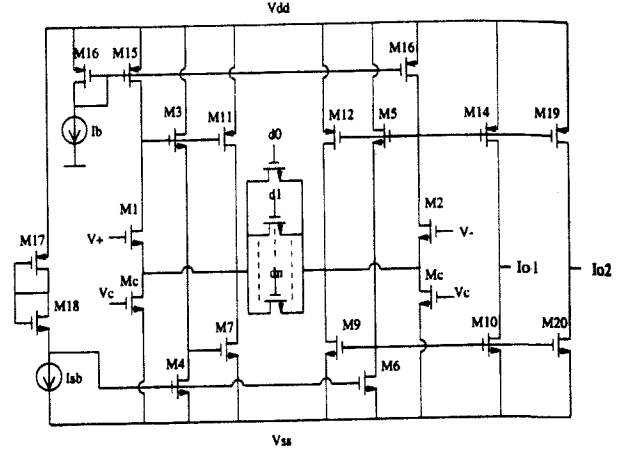


Figure 3: New class-AB OTA circuit realization.

$$I = \frac{V_+ - V_-}{R + 2r_x} \quad (1)$$

where r_x is the output resistance of the buffer. To obtain a high transconductance, the resistor value can be reduced to zero. Using current mirrors two copies of the current is mirrored to the output terminals of the OTA. The CMOS realization of the OTA is shown in Fig.3 where two class AB CMOS buffers are used and the resistor is replaced with a binary weighted MOS array. By changing the control word, the transconductance of the OTA can be digitally programmed. For a fixed transconductance, the digital terminals can be hard wired to the supply rails. The current is mirrored to the output terminals of the OTA by the mirroring action of transistors M10, M14 and M19, M20. The two biasing transistors M15 and M16 force an equal current through transistors M1 and M2, resulting in equal gate-source voltages for transistors these transistors. Therefore, the source of transistor M1 will trace the input V_+ and the source of transistor M2 will trace the voltage V_- . The low output resistance of the buffer is provided by the action of the class AB negative feedback loop formed by transistors M3, M4, M7 and M11. The feedback loop operates in a class AB mode to minimize the standby power dissipation. The operation of the class AB input stage can be described as follows: If a current is withdrawn from the output terminal the gate voltage of M11 is lowered. By the action of the level shift transistors M3 and M4 the gate voltage of M7 is lowered as well. Thus, the current through M11 increases and the current through M7 decreases. The result is that the feedback network provides the necessary extra current flowing out of the output terminal. Similarly, if the output

terminal sinks current, the gate voltage of M11 and M7 increases, this decreases the current through M11

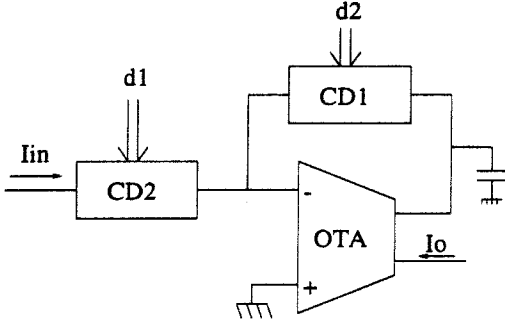


Figure 4: The variable gain amplifier circuit.

and increases the current through M7. The level shift voltage is used to adjust the standby current of the loop. Assuming all transistors to be in the saturation region and M3 and M4 are matched, it follows that:

$$V_{SG11} + V_{GS8} + V_{GS7} = V_{dd} - V_{ss} \quad (2)$$

$$V_{SG17} + V_{GS18} + V_{GS4} = V_{dd} - V_{ss} \quad (3)$$

In standby mode no current is withdrawn from the output terminal and the current I_b is equal to the current flowing through Mc (which can be used for common mode feedback as well). Hence, M7 and M11 have equal currents. Therefore :

$$I_{M7} = I_{M11} = I_{sb} \quad (4)$$

To realize a digital control exponential function, the approximation $e^x \simeq (1+x)/(1-x)$ is used [2] where the linear in dB relation can be achieved by dividing a linearly increasing function by a linearly decreasing one:

$$e^x \simeq \frac{1+x}{1-x} \rightarrow \frac{d_1}{d_2} \quad (5)$$

$$d_1 = 2^0 a_0 + 2^1 a_1 + \dots + 2^n a_n \quad (6)$$

$$d_2 = 2^0 \bar{a}_0 + 2^1 \bar{a}_1 + \dots + 2^n \bar{a}_n \quad (7)$$

The resolution n in equation (6) and equation (7) determines the number of gain steps of the AGC circuit. The proposed digital VGA is shown in Fig. 4, where the OTA is realized using the circuit shown in Fig.3. The current division network shown in Fig.5 is used to realize the digitally controlled dB-linear gain function. The relation between the output current and input current of such a network is given by:

$$I_{o1} = I_{in1} \sum_{i=1}^n d_i 2^{-i} \quad (8)$$

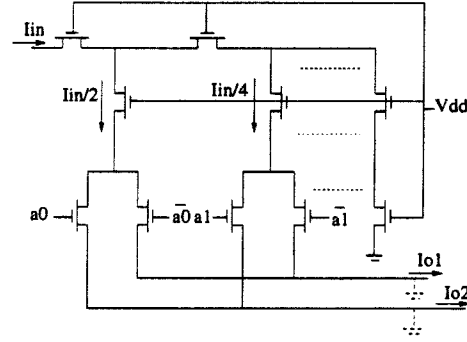


Figure 5: Current division network.

By equating the two currents at the virtual ground terminal of the OTA, one gets:

$$\frac{I_o}{I_{in}} = \frac{d_1}{d_2} \quad (9)$$

The current gain of the circuit is thus digitally controlled in an exponential manner. The current division network provides precise digital trimming without any spread in the transistor aspect ratios, which helps to maintain a compact layout area [7]. The capacitor connected to the VGA output is used for compensation and bandwidth limiting. The OTA current division loop has a variable gain. This will result in a gain bandwidth tradeoff where the bandwidth of the VGA circuit decreases as the gain is increased. For direct conversion receivers, there is no demand for high bandwidth and the trade-off between gain and bandwidth is acceptable. It is worth noting that it is possible to maintain constant loop bandwidth by using the gain control word to control both the current division networks and the OTA gain. Fig.4 shows a fully differential version of the VGA circuit. where two balanced currents are applied to the input and two balanced output currents are produced at the output. The circuit can be used for balanced input voltages as well [8]. In this mode two balanced input voltages are applied to the input terminal. The input current division networks will then convert the voltage to a digitally controlled current output. The VGA transconductance gain is then given by:

$$\frac{I_o}{V_{in}} = K_{cd}(V_{DD} - V_T) \frac{d_1}{d_2} \quad (10)$$

where K_{cd} is the current division transistor transconductance and V_T is the threshold voltage. To provide digital offset control, the two current dividers CD3 and CD4 are used. The inputs of CD3 and CD4 are connected to a constant bias current source. The digital

DC offset word is converted to an offset current that is added to the input current signals of the OTA.

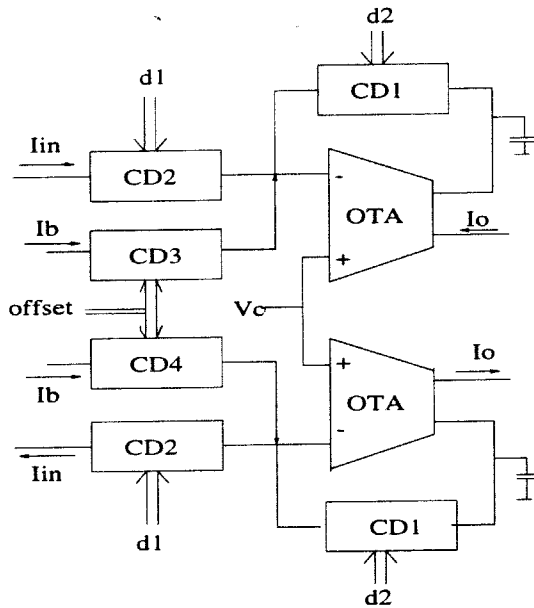


Figure 6: Fully differential digitally controlled VGA circuit.

4 Simulation results

The OTA circuit and the current divider networks were laid out and extracted. The extracted circuits were simulated using level 2 parameters of the ORBIT $2\mu\text{m}$ nwell CMOS process available through MO-SIS. The supply voltage used in the simulation is 3.3V and the non-inverting input terminal of the OTA is held at 2V. The biasing current is adjusted to $22\mu\text{A}$ and the standby current I_{sb} is set to $4\mu\text{A}$. Fig.7 shows the output current of the OTA versus the input voltage indicating a transconductance gain of 22mA/V . Fig.8 shows the supply current of the OTA versus the input voltage. The standby current of the OTA is less than $155\mu\text{A}$. It is clear that the class AB operation of the OTA provides high transconductance and high current drive capability with low standby current consumption. The phase margin of the OTA is more than 45° , and a unity gain frequency of 5MHz . Fig.9 shows the linear in dB gain control simulation results for the VGA circuit of Fig.6 with 6 bits of resolution. The digital control bits were swept linearly with time. The THD of the VGA was less than 0.1 percent for a $400\mu\text{A}$ peak to peak 100kHz sinusoidal output swing.

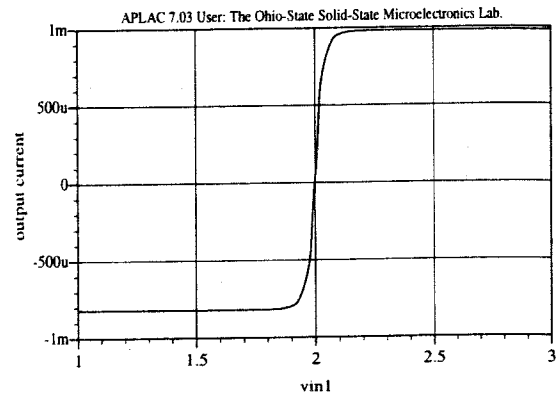


Figure 7: The output current of the OTA versus input voltage.

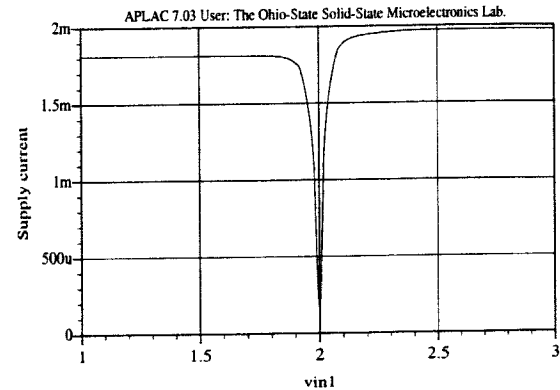
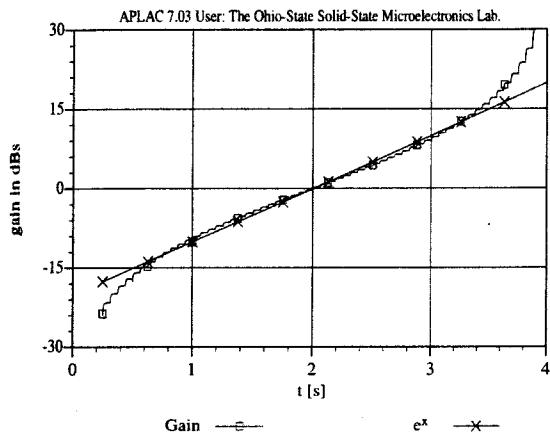


Figure 8: OTA supply current versus input voltage.

5 Conclusion

A novel digitally controlled VGA amplifier circuit is presented. The proposed circuit was optimized for use with direct conversion receivers. The circuit achieves a 25 dB gain control using a novel digital implementation of the exponential function. CMOS realization of the proposed circuit using a new class AB OTA and current division networks is discussed. Simulation results using level 2 parameters of the ORBIT $2\mu\text{m}$ nwell CMOS process confirms the attractive properties of the proposed VGA circuit. (Experimental results from a $2\mu\text{m}$ test chip is expected to be available at the conference)



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Figure 9: The fully differential VGA gain versus digital control word.

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