Next Generation Narrowband RF Front-Ends in Silicon IC Technology

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Abstract

It is anticipated that the next generation of wireless systems will deliver voice and data services at carrier frequencies extending up to 6GHz. The front-end circuits for these radios must be aggressively designed in order to deal with issues such as analog and digital compatibility, higher linearity imposed by broadband signal processing at IF, low supply voltage to minimize size, weight and power consumption, as well as operation in multiple frequency bands. The challenges and opportunities facing the designer of these radio frequency (RF) front-end IC's in silicon will be addressed in this paper from both the technological and circuit perspectives.

1. Introduction

It is expected that wireless systems to deliver voice (i.e., telephony), messaging and data will emerge and evolve rapidly over the next decade[1,2]. New standards are being proposed and adopted, however, some level of compatibility must be maintained with the previous generations of systems. For example, a system based on spread-spectrum modulation (e.g., CDMA) may be an appropriate design for urban areas, but older analog cellular technology may not disappear in many sparsely populated regions for a variety of economic reasons. Consequently, the next generation of wireless handsets and base stations will likely be required to deal with a number of additional constraints: mixed analog and digital standards, higher linearity imposed by broadband signal processing at IF, low-power and low-voltage restrictions to minimize size and weight, and operation in multiple frequency bands (e.g., 900MHz and 1800MHz bands), to name only a few.

The signal processing elements in a radio transceiver front-end are illustrated in the block diagram of Fig. 1. The elements shown in the figure could (potentially) be integrated onto a single RF IC, as indicated by the pins placed around a hypothetical chip boundary. However, the stringent performance requirements of "first tier" wireless systems[3], such as IS-54, IS-95 and GSM, has limited the level of integration seen in today's handsets. The transceiver functions in these radios are often implemented with a mixture of technologies, combining discrete components and RF ICs with a low level of integration (i.e., only one or two functions from Fig. 1 on each chip)[4]. The receive path

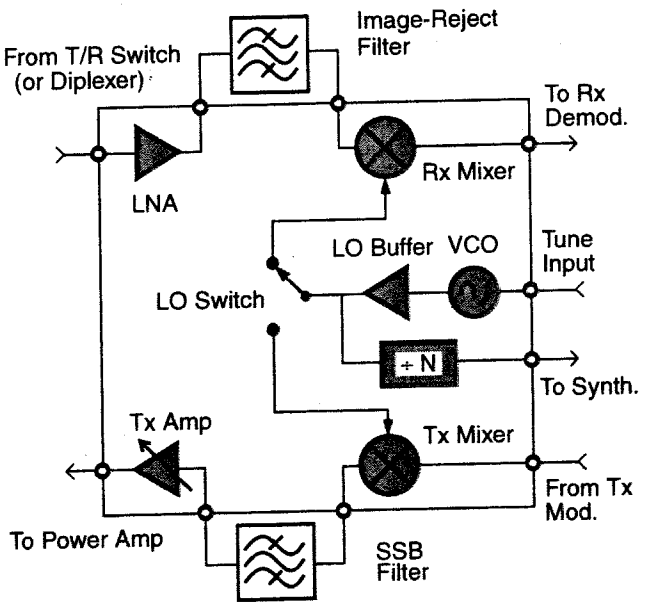

Figure 1: Typical RF IC front-end functions.

components have very demanding specifications, where an overall noise figure of 6-7dB is typically required. To achieve this, a preamplifier noise figure on the order to 2dB with a gain of 20dB is needed. The receiver linearity is usually determined by the first downconverting mixer, where an input third-order intercept greater than +5dBm is required. Oscillator phase noise has an effect on the signal-to-noise ratio of the demodulated signal and hence it must be less than -100dBc/Hz at a 100kHz offset from the centre frequency.

For products sold to the mass market in large quantities, cost and power consumption are important design considerations that favour IC implementations. Hence, "second tier" (e.g., PCS) systems and cordless telephones have depended upon RF ICs to a greater extent. Extending the performance of RF ICs will require advances in both passive and active components in silicon IC technology.

2. Active Device Performance

Sub-micron silicon IC technology is already capable of producing digital integrated circuits that can operate in the millimeter-wave band of frequencies (i.e., above

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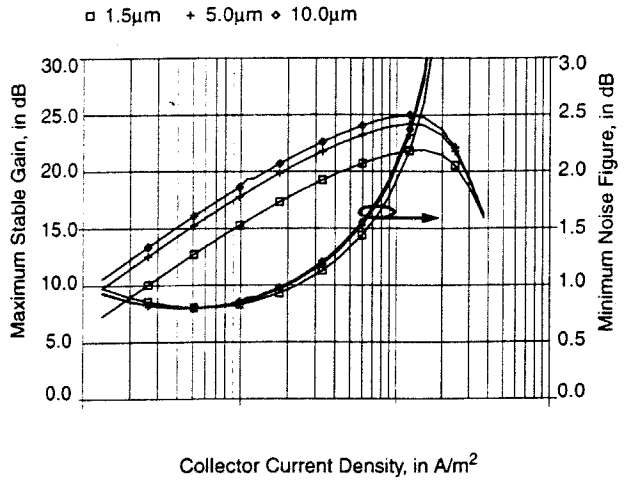


Figure 2: BJT performance for V_{CE} = 2V, f = 2GHz.

~30GHz)[5]. It is also on the verge of becoming a viable technology for analog monolithic microwave integrated circuits (MMICs)[6,7]. The technological limitations of silicon as an MMIC technology for the design of high performance RF front-ends are often expressed in terms of active device speed or bandwidth, and normally specified by parameters such as the transistor unity gain bandwidth, f_T. Of course, a sufficient margin between the desired band of operation and the f_T/f_{MAX} limitations of device technology is an absolute necessity, and typically one order of magnitude is considered adequate for a production design. This margin is required because the performance of the active elements has a significant impact on the receiver noise figure, gain, operation at low bias voltage and impedance matching.

The minimum noise figure and maximum stable gain of a common-emitter bipolar transistor amplifier for three different emitter lengths (1.5, 5.0 and 10.0μm emitter lengths) are plotted as a function of collector current density in Fig. 2. The performance illustrated here is representative of a state-of-the-art bipolar RF IC technology based on 0.5μm design rules, of which there are many examples[8]. It should be noted that the minimum noise figure is well below 1dB and it is almost independent of the emitter area selected, and that there is a broad range of bias points over which the noise figure of a typical common-emitter amplifier can be minimized[9]. Comparison of the two groups of curves shown in Fig. 2 illustrates the trade-off between noise and gain in the selection of bias point. The current density for minimum noise does not coincide with the peak gain for the transistors. However, a single-stage gain greater than 20dB and a sub-2dB noise figure is feasible with a bias current in the low mA range at 2GHz.

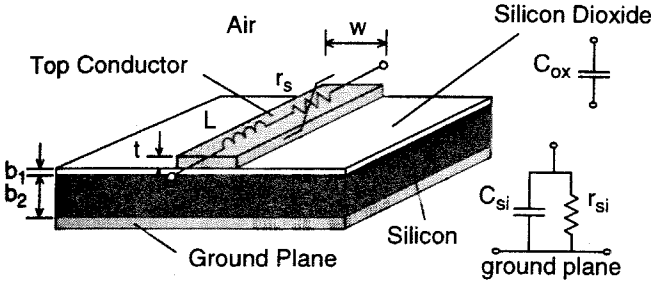
Aside from gain and noise, harmonic and intermodulation distortion of the transistor amplifier also depends upon the bias current. The third-order intercept point can be estimated from the small-signal linear power limit of a narrowband amplifier stage[10]. Of course the linear power range at the output is influenced by the bias current, load impedance, supply voltage and a variety of other factors. Implementation in a monolithic context offers some flexibility to the designer in this regard, if the 50 Ohm interface between preamplifier and image reject filter is eliminated (e.g., using an image-reject receive mixer). Feedback (such as emitter degeneration) modifies the input compression and intermodulation intercept points through a change in the amplifier gain.

An output third-order intercept point of +19dBm is theoretically achievable for a narrowband amplifier biased at 5mA operating from a 2V supply. However, the compromises between gain, linearity and noise figure reduces the output intercept by over 10dB in a practical implementation[4].

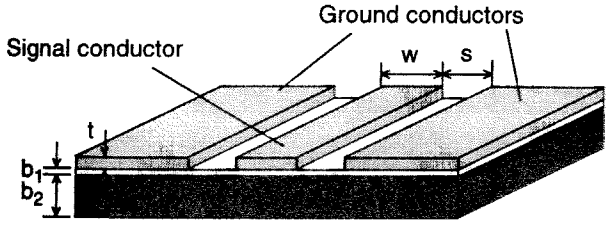
3. Passive Component Performance

From a technological perspective, the circuit elements which limit the dynamic range in a typical RF IC receiver implementation involve far more than simply active devices alone. The performance constraints on the front-end imposed by passive elements in silicon IC technology and low-cost (i.e., plastic) IC packages are becoming more of a challenge to the designer than the active devices. For example, the highest performance production silicon bipolar technologies today offer transistors with f_T/f_{MAX} on the order of 50GHz[7]. A microstrip transmission line fabricated in the same technology, which has an acceptably low loss of 0.5dB/cm at 1GHz, has a extraordinarily high loss of 10dB/cm at 10GHz[11]. In addition, the constraints imposed by these elements are not well understood by designers, or captured in modern CAD tools. Additional margin must be built into a typical design in order to account for some degradation in performance. This leads to non-optimal designs, and often, numerous redesigns of a circuit in order to meet product specifications.

The two most commonly used transmission line structures available to the IC designer are the microstrip and coplanar strip waveguides (see Fig. 3). The microstrip (Fig. 3a) is the simplest and most popular configuration because an adjacent ground conductor is not required on the top side of the substrate. However, a connection from the top to the back of the IC is required in order to properly couple signals to a microstrip transmission line. In III-V MMIC technologies, a low inductance connection between the top and back sides of the wafer is realized using via holes that are milled through the substrate by chemical etching. This technology is not readily available in most silicon IC processes. As an alternative, two layers of metal could be used to define the top conductor and ground plane. For example, a 10μm wide line in topmetal separated from a metal (i.e., ground) plane by 5μm of oxide would have a characteristic impedance close to 50 Ohms. However, ohmic losses in the



(a) Microstrip transmission line



(b) Coplanar waveguide transmission line

Figure 3: Transmission lines on silicon RF ICs.

relatively narrow conductors at microwave frequencies cause high attenuation in such a structure. Coplanar waveguide (Fig. 3b) does not require via hole technology, but ground conductors adjacent to the signal line are needed, which restricts signal routing. It is often used at frequencies above 10 GHz because of its low dispersion compared to microstrip.

Attenuation in on-chip transmission lines is a primary concern for silicon MMIC designs. The drive to reduce ohmic losses in IC wiring for high-speed digital circuits through the use of lower resistivity metals such as copper will benefit the MMIC designer as well[12]. Other techniques of reducing losses caused by the semiconducting substrate are: very thick intermetal dielectrics (~20μm) using polyimides and gold metallization[11], lower ε_r intermetal dielectrics, partial or complete removal of the semi-conducting substrate beneath the interconnecting metal[13,14,15], and fabrication of devices on semi-insulating substrates using technologies such as silicon-on-sapphire (SOS) or bonded silicon-on-insulator (bonded SOI)[16,17,18].

Accurate models for interconnect and all passive devices on-chip (i.e., inductor, cap, resistor, etc.) up to a factor of 5 greater than the intended operating frequency are necessary for high performance RF designs. Full-wave electromagnetic (EM) simulators have been widely available since the late 1980's[19], however, their use by RF IC designers has been limited by the computational time and skill required to successfully apply these sophisticated simulation tools. Over time, improvements in computer processing power will make full-wave EM analysis fast enough for the optimization of

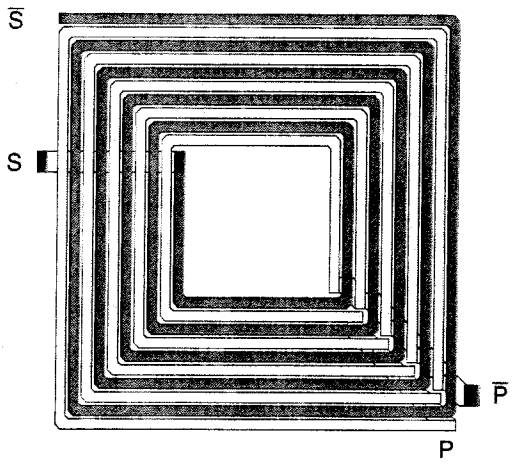


Figure 4: 1:5 square spiral transformer.

circuits, but unfortunately that capability is still unavailable today. A bridge between the complete solution of Maxwell's equations in three dimensions and many of the very rudimentary engineering approaches being used by RF IC designers is needed. Scalable compact models for passive components, such as inductors and transformers fabricated on semi-conducting silicon substrates, have been developed and can be applied to the design of narrowband circuits in microwave bipolar processes for many commercial applications[20,21]. Accuracy of this modeling technique has been verified for circuits fabricated in production silicon VLSI processes using medium resistivity substrates.

The limitations of monolithic inductors and transformers as circuit components must be clearly understood in order to make intelligent design compromises. Consider the sample layout for a monolithic transformer illustrated in Fig. 4. The secondary winding is a continuous square spiral of topmetal with a total of 5 turns. The remaining 5 turns of topmetal form the primary winding, where the end terminal of each turn are connected in parallel, forming a 1:5 turns ratio transformer. The path for magnetic flux that is produced by current flow in the windings is highly linear. However, only 80% of the flux produced by a current flow in one winding is coupled to the other because of leakage inherent in the planar design[22,23]. Imperfect coupling leads to attenuation and constrains the bandwidth of the device, but it is not a source of noise. Source of dissipation such a ohmic losses in the metal and semiconducting substrate are sources of noise which must be accounted for in the design. Parasitic capacitance between windings, and from the metal windings to the substrate, limits the high frequency bandwidth. Resonant tuning of the transformer is achieved by adding shunt capacitance at the transformer's ports. Tuning can be used to reduce losses in-band to below 1dB in most cases, but the operating bandwidth is reduced to approximately one octave for a tuned transformer.

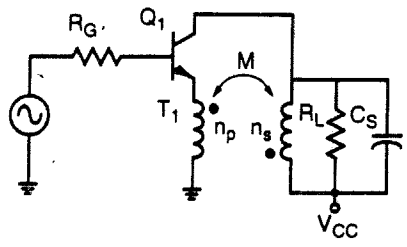


Figure 5: A transformer-coupled RF preamplifier.

4. Narrowband Front-End Circuits in Silicon

Narrowband LC circuits, which are constrained to work over a frequency range of a few octaves at most, can realize better performance than traditional broadband circuits based on resistor-capacitor (RC) topologies[24]. This improvement comes from establishing a resonance at the desired frequency of operation using an on-chip inductance, thereby absorbing the parasitic capacitance of another element (e.g., a transistor). The L-C combination can form resonators and tuned loads for narrowband amplifiers, oscillators and filters, as well as tuned networks for feedback, matching and interstage coupling in RF front-ends. In order to achieve high linearity and sensitivity in practical RF circuit topologies, a passive inductance is required. Technological refinement of inductive elements for silicon ICs is still in the early stages of development. However, circuit techniques that exploit the benefits of a monolithic inductors and transformers have been manufactured in production III-V technologies for more than a decade[25,26], and many of these design principles can be applied to RF front-ends in silicon IC technologies. A narrowband low-noise amplifier and receive mixer in silicon IC technology will be used here as illustrative examples.

4.1 The Low-Noise Preamplifier

The benefits of negative feedback in amplifier design are well-known, however, a broadband feedback amplifier cannot meet the sub-3dB noise figure required for many wireless applications. The transformer is an almost ideal feedback element for an RF amplifier, and can be used as a narrowband alternative to a broadband, resistive network. Feedback via mutual magnetic coupling, as shown in Fig. 5, allows for control of the amplifier gain and linearity without introducing excessive noise. A lower supply voltage is also possible, since ohmic drops in the signal path are nearly eliminated. For example, a 1dB noise figure RF preamplifier with a input third-order intercept point of -4dBm, with 12dB of gain, and draws only 2mA from a 1V supply, has been realized using transformer feedback[27,28]. This level of performance was achieved using a production silicon IC process flow that was not optimized for RF performance from the passive components.

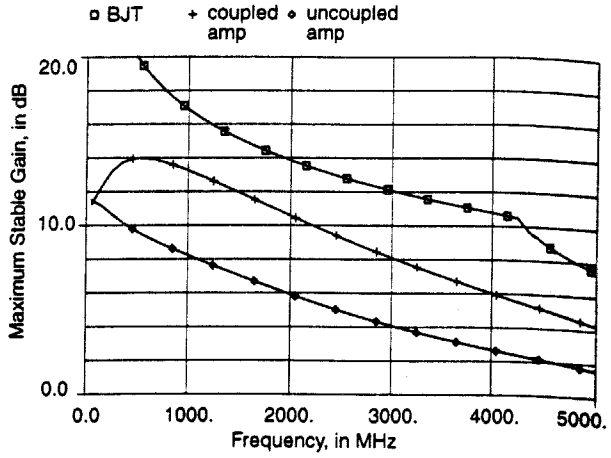


Figure 6: Feedback amplifier comparison.

It is useful to compare the performance of the transformer-coupled amplifier (or simply "coupled amplifier") to a single stage preamplifier with emitter degeneration and collector load inductors (an "uncoupled" amplifier). The uncoupled amplifier is a special case of the feedback amplifier shown in Fig. 5, where M = 0. The simulated maximum stable gain (MSG) that can be realized for a common-emitter bjt, and for the same transistor connected in both coupled and uncoupled amplifier configurations is compared in Fig. 6. The transistor (0.8μm BiCMOS technology, f_T=12GHz[29]) is biased at I_C = 2mA and V_{CE} = 1.9V in each case. A Q-factor of 5 was assumed for both emitter and collector inductors in the uncoupled amplifier. An emitter inductance that resulted in an intercept point comparable to the coupled amplifier design was used for the comparison.

As seen from Fig. 6, there is a clear advantage in power gain at a given linearity when the collector and emitter loops are coupled with a monolithic transformer. The transformer-coupled preamplifier produces over 4 dB more gain than an two-inductor (uncoupled) amplifier with comparable noise figure, power dissipation and linearity.

4.2 The Receive Mixer

Improvement in the overall dynamic range of RF IC mixers (i.e., increasing the linearity while preserving the sensitivity) is necessary if silicon designs are to be competitive with III-V and discrete implementations in next generation of wireless applications.

The conventional IC double-balanced demodulator, which is based on the Gilbert multiplier topology[30], can be viewed as a linear preamplifier stage followed by a differential downconverting mixer, as illustrated in Fig. 7. The function of the input stage is to convert a single-ended RF input signal into a differential signal that drives the RF inputs of a four transistor mixing quad. This is analogous to the function of a

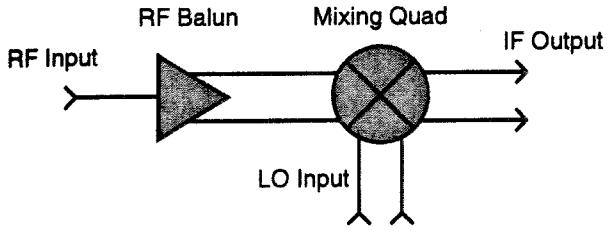


Figure 7: IC double-balanced modulator.

balun in RF and microwave mixer circuits[31].

Gain in the input stage can be used to suppress noise introduced by the mixing stage, but this gain also reduces the upper limit on the mixer's dynamic range. However, distortion in the receive mixer usually defines the input intercept point for the receive chain in a modern transceiver. Hence, the input stage in the Gilbert mixer is normally designed with little gain in order to maximize the linear range at the mixer's RF input.

Three realizations for the input balun in a receive mixer are illustrated in Fig. 8. The conventional Gilbert multiplier uses a differential pair of transistors to perform the single-ended to differential signal conversion (Fig. 8a). Degeneration of the differential pair to reduce the input stage gain is realized using impedance Z_{EE} as shown in the figure. A degeneration resistance (i.e., R_{EE}) degrades the mixer noise figure and so inductive degeneration (L_{EE}) is preferred. The real part of the input impedance in such cases is typically on the order of a few hundred Ohms, which makes impedance matching to a 50 Ohm source difficult. The Class-AB input stage[32] uses a low impedance common-base stage and a current mirror to form the RF input balun (Fig. 8b). The low impedance of the common-base stage simplifies matching of the mixer input to a low impedance source. The input stage is degenerated by the source impedance, which extend the linear range at the RF input without degrading the noise figure. The active devices in the RF signal path still affect the signal-to-noise ratio, however, and there can be a substantial phase error between RF signals at the balun outputs, unless there is sufficient operating margin in the active devices used in its realization.

Interstage coupling using on-chip magnetic elements such as the transformer balun shown in Fig. 8c) is an alternative technique of aggressively improving a mixer's performance, which has a different set of design trade-offs from the better-known RC mixer topologies[28]. With a passive transformer balun, the RF input can be effectively matched to the mixing quad through the appropriate choice of transformer turns ratio. The passive balun introduces virtually no distortion to the RF signal, thereby preserving linearity. Resonant tuning must be used to ensure that the signal-to-noise ratio is not excessively degraded in the transformation.

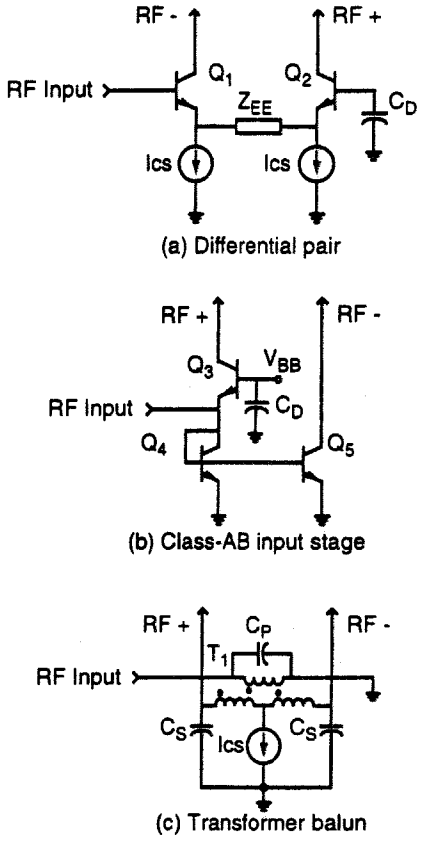


Figure 8: Input stages for the receive mixer.

Mixers with high linearity and noise figures in the 6-7dB range can be implemented on-chip using balun-coupled diode ring topologies[31]. Input intercept points on the order of +10dBm, or more, are possible for such mixers based on a quad of Schottky diodes. The LO power required to drive the diode mixer is a disadvantage when 50 Ohm interfaces are required. However, in a completely monolithic implementation, the port impedances can be defined on-chip in order to reduce power consumption. The transformer-coupled approach has the potential to realize a variety of proven mixer topologies, including image-reject designs. If implemented monolithically, these components would offer a significant advance in transceiver performance and integration level compared to the current state-of-the-art.

5. Conclusions

Narrowband RF IC circuits offer the potential to realize substantial gains in the performance of wireless transceiver components fabricated in silicon IC technologies. In order to make silicon a viable MMIC technology, losses introduced by the semi-conducting substrate must be reduced significantly. In addition, improvements in modeling and simulation techniques are required to optimize circuit designs fabricated

on silicon substrates. Two circuit examples were used to illustrate the performance benefits that are possible when narrowband design techniques are combined with circuit topologies in common use on silicon ICs.

6. Acknowledgements

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