A Unified Approach for a Time-Domain Built-In Self-Test Technique and Fault Detection

B. Provost[1], A.M. Brosa[2] and E. Sánchez-Sinencio[1]

[1] Department of Electrical Engineering, Texas A&M University, TX (US), provost,sanchez@amesp01.tamu.edu
[2] Departament d'Enginyeria Electrònica, Universitat Politècnica de Catalunya, Barcelona (SPAIN), brosa@eel.upc.es

Abstract

Being able to fully test a circuit is an important issue for quality manufacturing. Unlike fault analysis for digital circuits, analog fault analysis has been comparatively slow to evolve. The purpose of this paper is to study the feasibility of the time domain response analysis as a test method for analog circuits[1]. The approach was to first study the fault coverage obtained by testing the main parameters of the new NGCC amplifier, which shows the feasibility of built-in self test in time-domain. A circuit macromodel to implement a time-domain built-in self-test circuit was then proposed.

1: Introduction

Testability analysis in analog circuits is an important task and a desirable approach for producing testable complex systems. Because of the density of analog circuits which continues to increase and of the nature of analog faults, the detection and isolation of faults in these circuits becomes more difficult.

Owing to the non-binary nature of their operation, analog circuits are influenced by process defects in a different manner compared to digital circuits. This calls for a careful investigation [1]-[11] into the occurrence of defects in analog circuits, their modeling related aspects and their detection strategies. Thus, analog testing is a difficult and expensive task. Analog circuits have been traditionally tested by verifying their functionality (functional test), which is known to be costly [3]. The difficult stems from the fact that, unlike digital circuits, the physical quantities of analog circuits, like voltages and currents, vary over time in a continuous range. This implies a continuum of possible defects. In consequence, there is a lack of adequate fault models, since the output values of analog circuits cannot be considered as either high or low level as in the digital world, where a large class of defects can be modeled by *stuck-at-0/1* faults.

In this paper, preliminary results of a unified approach to tackle the fault detection problem and a built-in self-test strategy in the time domain are introduced. By considering the main physical and parametric defects determined from manufacturers of analog IC's, the results of the test circuit macromodel are satisfactory and provide a 100% fault coverage. The rest of the paper is organized as follows: in section 2 the targeted analog amplifier is designed and analyzed. Section 3 describes the tests (AC, DC and time response) applied to the mentioned cell. The different fault coverages are presented and compared in section 4, and a proposal for a built-in test circuit is given in section 5. Finally, the conclusion is given in section 6.

2: The NGCC Amplifier

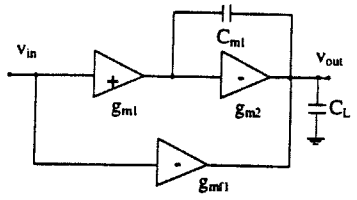
As the power supply voltage for integrated circuits continues to scale down, the analog design in mixed signal environments is becoming more difficult and challenging. The main reason is that the threshold voltage is not expected to scale down proportional to the supply voltage. The operational amplifier, which is a core building block for analog systems, is a perfect example to demonstrate how difficult it is to design in a low voltage environment. The conventional vertical gain enhancement technique (cascoding) is no longer suitable for low voltage applications because it does not allow enough head room for voltage swing anymore. Instead, horizontal gain enhancement techniques (cascading) must be used [12-15].

In designing a multistage op amp with multiple feedback loops, special precaution in the compensation must be taken to ensure stability . In [15] a very good discussion on what is known as Nested Miller Compensation (NMC) technique is given in terms of its stability. In [20] a new topology, the Nested Transconductance (G_m) Capacitance Compensation (NGCC) is proposed. The NGCC topology has a simple and regular function, which yields to a very simple stability

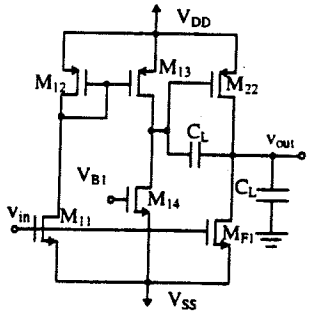
[1] This work is partially supported by Texas Instruments Inc., Dallas, TX.

0-8186-8409-7/98 $10.00 © 1998 IEEE

condition. In this paper, as shown in Figure 1a, we use the basic module (2-stage) NGCC topology, whose transistor level realization is presented in Figure 1b.



a)



b)

Figure 1: a) The NGCC Amplifier topology
b) Transistor level realization

In table 1 its typical characteristics are depicted. Assuming that $g_{m1}=g_{m2}$, the transfer function of the amplifier can be given as:

$$\frac{V_{out}(s)}{V_{in}(s)} \cong -\frac{\frac{g_{m1}g_{m2}}{g_{o1}g_{o2}}}{1+s\frac{g_{m2}C_{m1}}{g_{o1}g_{o2}}+s^2\frac{C_{m1}C_L}{g_{o1}g_{o2}}} \qquad (1)$$

where $g_{o1}=g_{ds13}+g_{ds14}$
$g_{o2}=g_{dsf1}+g_{ds22}$ (2)

If the denominator of (1) can be written as

$$D(s)=\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right) \qquad (3)$$

and assuming that p_1 is the dominant pole, i.e. $|p_1| << |p_2|$, then (3) can be approximated by

$$D(s) \approx 1-\frac{s}{p_1}+\frac{s^2}{p_1 p_2} \qquad (4)$$

then equating the denominator of (1) to (4), the expressions of the dominant pole and the second pole can be obtained as follows

$$p_1 \approx -\frac{g_{o1}g_{o2}}{g_{m22}C_{m1}} \quad p_2 \approx -\frac{g_{m22}}{C_L} \qquad (5)$$

From (1) it is also easy to obtain the expression of the open-loop gain

$$A_o = -\frac{g_{m11}g_{m22}}{g_{o1}g_{o2}} \qquad (6)$$

Combining (5) and (6), and using (1), it can be easily shown that the expressions of the unity-gain frequency bandwidth and the phase margin are the following

$$GB = |A_o p_1| \approx \frac{g_{m11}}{C_{m1}} \text{ [Hz]} \qquad (7)$$

$$\Phi_m = arctg\left(\frac{A_o}{1-A_o^2\frac{p_1}{p_2}}\right) \qquad (8)$$

DC Gain	A_0	84dB
Unity-Gain Bandwidth	GB	202kHz
Phase Margin	Φ_m	82°
Input Resistance	r_{in}	∞
Output resistance	r_{out}	12MΩ
Output voltage at 0 input	v_{out} (v_{in}=0)	14mV
Power Consumption	P	7μW

Table 1: NGCC characteristics

3: Test of the NGCC Amplifiers

3.1: Types of test

The multitude of response parameters in analog circuits makes testing difficult and expensive. The tendency is oriented towards functional testing (spec-based tests). For testing complex analog systems, a circuit partitioning is done and each sub-block is tested separately. For linear circuits the tested parameters could include DC specifications; AC specifications, and transient specifications [23]. For the NGCC circuit, three kinds of test have been considered :

1) AC Test, where the low-frequency gain (A_o), the phase margin (Φ_m), and the unity-gain bandwidth (GB) have been observed.
2) DC Test, where the observables are the i_{DD} current and the output voltage (v_{out}).
3) Transient test, where a 1μs-t_{rise} step has been applied to the circuit, and the fall time (90%-10%) of the voltage at the output and the delay time have been measured for small signal (50μV amplitude) at the input.

3.2 Types of defects

In general, faults in analog circuits can be classified into hard (or catastrophic) and soft (parametric) faults. *Hard* faults are caused by catastrophic variations in the structure of the circuit such as shorts and opens [10], and usually induce a complete loss of functionality. *Parametric* faults are caused by abnormal deviation of parameter values and result in altered performance. Both types of fault have to be detected by a set of tests.

From the wide spectrum of possible defects reported in CMOS circuits, two kinds of catastrophic defect have been chosen, both of them external to the devices of the circuit: bridges (shorts) among conducting lines, and opens of the conducting lines of the circuit. These catastrophic defects have been widely described in [16] for the digital domain.

Two kinds of parametric defects considered in this study deserve a special mention: β shifts and V_T shifts. These parametric defects may be introduced in some of the process steps, as well as can be induced by the field environmental conditions during the circuit operation. Assuming that the simplest form of the current in the saturation region can be represented by

$$i_{D\,Sat} = \frac{\beta}{2}\left(V_{GS} - V_T\right)^2\left(1+\lambda V_{DS}\right) \qquad (9)$$

where β depends on the aspect ratio (W/L), the channel mobility (μ) and the oxide capacitance (C_{ox}). In order to group all the possible deviations of (W/L), μ and C_{ox} , the first parametric defects considered are the shifts in β. The second type of parametric defects are the deviations on the threshold voltage of the MOS devices. In fact, during the life of MOS transistors, different reasons may cause a permanent or temporary shift in their threshold voltage, V_T. Also, experimental results have shown that several process manipulations going from first steps up to the dicing and packaging steps, may cause threshold voltage shifts [17]-[19]. If we define a certain variability ΔV_T, the threshold voltage can be written as

$$V_T = V_{T0} + \Delta V_T \qquad (10)$$

Simultaneous shifts of the nMOS' threshold voltage (V_{TN}) and the pMOS' threshold voltage (V_{TP}) will be applied to the NGCC circuit, considering four cases: 1) $\Delta V_{TN} < 0$, $\Delta V_{TP} < 0$; 2) $\Delta V_{TN} < 0$, $\Delta V_{TP} > 0$; 3) $\Delta V_{TN} > 0$, $\Delta V_{TP} < 0$; 4)$\Delta V_{TN} > 0$, $\Delta V_{TP} > 0$, ΔV_T being the concerning deviation of V_T in every case.

To consider catastrophic faults in the NGCC circuit, the hard fault model at the transistor level in Figure 2 is adopted. It is based on the fault model described in [21] and implements drain to gate, source to gate and drain to source shorts, together with opens on drain and source contacts.

Applying this fault model and taking into account the drain to gate shorts already realized for transistor M_{12} , a total of 45 catastrophic faults (worst case) can be listed for this circuit: 21 possible shorts node-to-node, and 24 opens. For the parametric set, β deviations of $\pm 5\%$ and $\pm 10\%$ over the nominal value have been considered, and 10mV, 100mV, and 200mV V_T shifts have been applied. Next section will present the results obtained from every type of defect for every kind of the mentioned tests.

4: Results

The acceptance or rejection of a circuit under test is required to be reliable: testing errors like rejecting a circuit actually good or accepting a really faulty one should not occur. The adoption of DfT and BIST schemes aims at increasing test efficiency by improving controllability and observability indexes affected by higher integration levels and compactness. The extra circuitry introduced by these schemes is not always well accepted due to the area and cost overhead which they may represent. However, this situation is changing as the improvements due to testing are recognized [24]-[26].

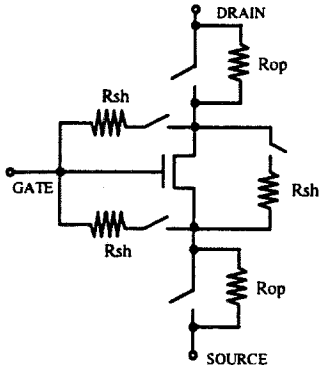


Figure 2: Hard faults at the transistor level

For the NGCC amplifier, once the catastrophic and parametric defects are modeled and HSPICE simulated, and the AC, DC and transient tests have been applied, two selection criterias have been taken into account, in order to decide whether a fault is detected or not: 1) *Rule of 10* criterion / 2) *Rule of 5* criterion, which considers that a fault is detected if the error measurement is greater or equal to 10%/5% for the GB, i_{DD} , v_{OUT} , and fall and delay time measurements, and 10dB/5dB for the A_o measurements, and 10°/5° when measuring the phase margin. Plots of the percentage of detections for every criterion and case appear in Figures 3. From these graphics, the following points can be observed:

- Catastrophic defects such as shorts and opens in the NGCC amplifier are mostly detected by transient (around 80%) and AC metrics (achieving a 100% coverage). This

is due to the strong deterioration of the performance in most of the cases. DC test offers very poor fault coverage. On the other hand, the parametric defects considered in this analysis are mostly detected by the DC metric, more precisely by the observation of the i_{DD} current. This is due to the direct influence of β and V_T on the current expression. AC metrics offer poor percentage of detection (the transistors remain in saturation and the performance is scarcely penalized), but the transient response allows to achieve around 100% of detected cases, thus justifying the goodness of the transient response test method.

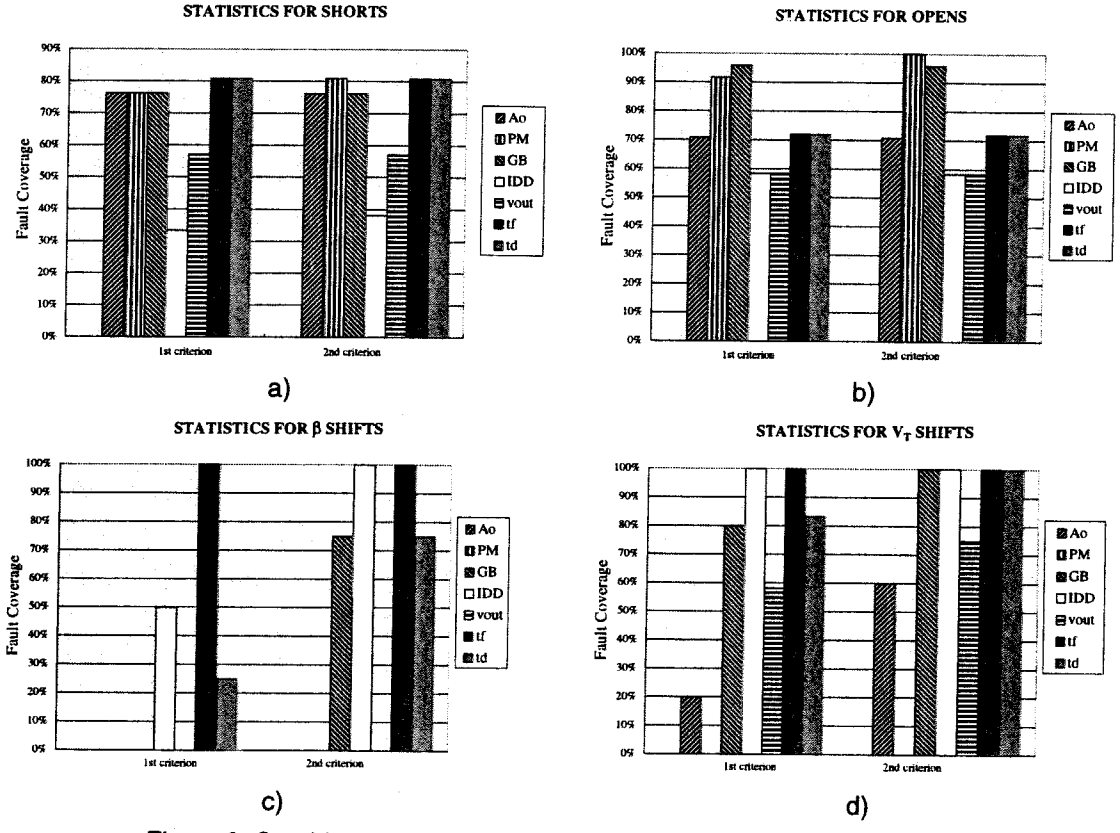


Figure 3: Graphical representation of the percentage of detection achieved with the different test methods.

- Good detections are obtained for the catastrophic defects when measuring the phase margin. If the time response is used, this can be translated into the delay time measurement.
- The power supply current of an analog circuit results from the sum of the individual currents of a number of circuits, each of which may present widely differing amplitudes and waveforms [24]. This can constitute a drawback to fault detection in subcircuits whose power supply current is much smaller than the others. As the NGCC amplifier has been designed in such a way that all the subcircuits (inverters) present the same power supply current, good detections are obtained for the parametric defects when measuring the i_{DD} current. But it also detects the $i_{DD}(t)$ variations for a large amount of time. If our purpose is to focus on the detection by the use of the time response, the possibility of an i_{DDQ} measuring structure should be studied. This is matter of our future work.

5: Built-In Test Circuit Proposal

We have seen from the previous section that some of the most important parameters for full test coverage are the time-domain parameters (fall time and delay). Moreover, these parameters are well suited for analog built-in self-test since they are relatively easy to measure with simple (hence easily integrated) timing circuits. They can also be used for characterization of the filter in time-domain or in frequency domain. Some simple relations (especially if the first pole is much smaller than the other poles) can be used to relate the time-domain and frequency domain characteristics. In this section, we will set the needs for a built-in self-test circuit based on time-domain parameters. Then we will

describe the macromodel of this circuit and give some preliminary results. The goal is to measure the two delays that represents the fall-time and the delay between the input and the output of the op-amp. Figure 4 shows the timing diagram of the different signals involved in that process.

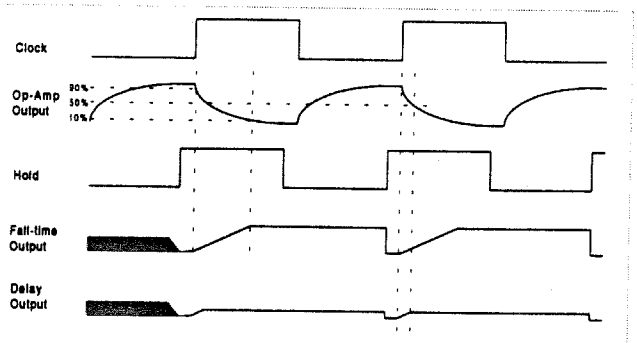


Figure 4: Timing diagram for the measurement of time domain parameters.

The "Clock" signal is sent to the input of the op-amp, which is configured in inverter-amplifier. The output of the op-amp is acting like a low-pass and the timing measurements have to be made between 90% and 10% of the settled output value (for the fall-time) and between the start and 50% of the signal (for the delay). The "Hold" signal is used to hold the output signal of the op-amp while making comparisons between the steady-state value and the actual value. These delays will be measured by analog timers. The expected results are also shown ("Fall-time Output" and "Delay Output"). We can see that the Fall-time output starts rising at the 90% detection and stops at the 10% detection, while the Delay output starts rising at the beginning of the Clock cycle and stops at the 50% detection. The steady-state level of the timer is the final timing result.

Figure 5 shows the block-diagram of the macromodel used to implement this test circuit. The op-amp block has been modeled by an overdamped second order low-pass filter. The Clock signal is sent to the op-amp under test and the result is sent to the test circuit. The steady-state value is held by the Sample/Hold block. From this value, we derive the three reference values (90%, 10% and 50%). The input signal is compared to these reference voltages. Timer 2 is started when the signal starts to decrease, i.e. when the clock signal goes high again. As soon as the input signal becomes lower than 90% of the steady-state value, Timer 1 is started. When the signal drops to 50% of the steady-state value, Timer 2 is stopped and the delay value between the input and output is available at the output of Timer 2. When the input signal drops to 10% of the steady-state value, Timer 1 is stopped and then the fall-time is available at the output of Timer 1. The two timers are reset by the "Hold" signal, i.e. just before the output of the op-amp starts to increase again. Finally, the results from the timers are compared to reference voltages and a "Fault-Free" signal is sent if the delays are within predefined windows of acceptability.

This macromodel has been simulated using Spectre-HDL. The simulation result is shown on figure 6. The error on the timer final output voltages is lower than 1%. This error is due to the component non-idealities necessary to assure convergence. Most of the blocks in this system are very simple to implement, with the exception of the timers. The timers must be as linear as possible, and must not be subject to charge injection from the digital control signals. Charge injection is a systematic error, but the error value is difficult to predict. One way to overcome these problems and get a very high resolution on the timing measurement is to use a digital counter. This would also eliminate the problem of generating the reference timing voltages for comparison, since the comparison would be a simple digital comparison with a pre-defined digital word. Also, this would allow a precise and easily modified result analysis.

Each of these design options should be considered in relation with the kind of system under test. Even if the complexity of the building blocks to be used in the design of the test circuit is kept as low as possible, the test overall complexity will definitely be higher than the complexity of the op-amp under test. However, in large mixed-signal systems, the number of op-amps under test is usually large. By using the same test macrocell to test all op-amps, the overhead complexity is much more acceptable. Moreover, the mixed-signal system may provide digital counters and comparators which can be used in the test circuit without increasing the overhead complexity.

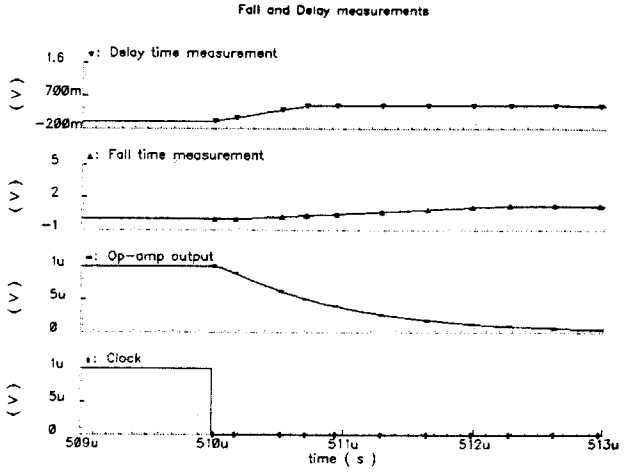


Figure 6: Simulation result of the macromodel

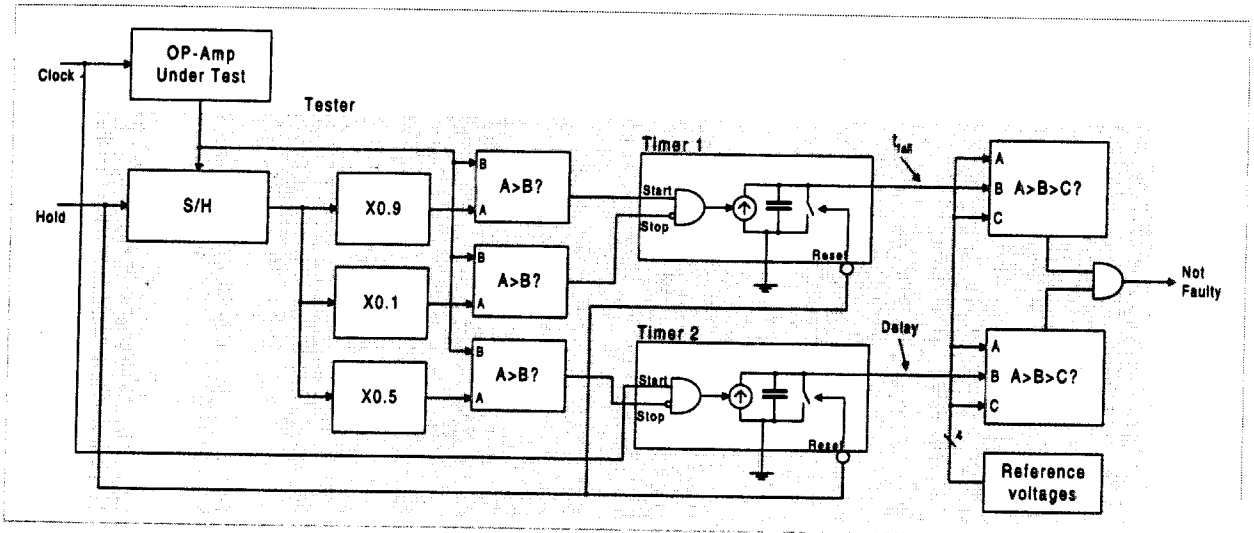


Figure 5: Block-diagram of the built-in test macromodel.

The main limitations of the test circuit are the delays to be measured. These delays are defined by the pole locations and the amplitude of the input step signal. The delays should not be too small so that the follower delays and the errors in the test circuits (for example, the clock feedtrough) are negligible. Also, in the case where analog timers are used, the delays should not be too large so that the sizes of the charging capacitors are acceptable.

Since the detected information (time domain behavior) defines the characteristics of the op-amp, we can use these measurements as a signature in order to localize the possible faults. In the situation where digital counters are used, a single serial output can send all the characterization results for external analysis. If analog timers are used, the characteristics can be made accessible one after the other on the single output pin through the use of an analog multiplexor.

6: Conclusion and Future Work

In this paper, the feasibility for a time-domain built-in self-test technique has been shown. The main parameters of the NGCC amplifier have been tested for fault coverage in the three domains (DC, AC and transcient) and the validity of time-domain testing has been observed. Based on these results, a circuit prototype has been designed and simulated to perform the built-in test of the amplifier. The precision of the simulation results prove that time-domain testing is an efficient method for analog built-in self test. The frequency-domain characteristics can be related to the time-domain parameters by non-linear equations with the use of some digital signal processing. Immediate future work includes device level design of the built-in test circuit and chip implementation.

References

[1] M. Slamani and B. Kaminska, "Fault Observability Analysis of Analog Circuits in Frequency Domain", *IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing*, 43(2):134-139, February, 1996.

[2] I. Baturone, J.L. Huertas, S. Sanchez-Solano, and A.M. Richardson, "Supply Current Monitoring for Testing CMOS Analog Circuits", *Xth Conference on Design of Integrated Circuits and Systems, DCIS'96*, Barcelona-Sitges, 20-22 November 1996, pp. 231-236.

[3] J. van Spaandok and T.A.M. Kevenaar, "Selecting Measurements to Test the Functional Behavior of Analog Circuits", *Journal of Electronic Testing:Theory and Applications (JETTA)*, 9 (1/2), August/October 1996, pp. 9-18.

[4] A. Abderrahman, E. Cerny, and B. Kaminska, "Optimization-Based Multifrequency Test Generation for Analog Circuits", *Journal of Electronic Testing:Theory and Applications (JETTA)*, 9 (1/2), August/October 1996, pp. 59-73.

[5] M. Lubaszewski, S. Mir, and B. Courtois, "Unified Built-In Self-Test For Fully Differential Analog Circuits", *Journal of Electronic Testing:Theory and Applications (JETTA)*, 9 (1/2), August/October 1996, pp. 135-151.

[6] M. Sachdev, "A Realistic Defect-Oriented Testability Methodology for Analog Circuits", *Journal of Electronic Testing:Theory and Applications (JETTA)*, 6 (3), June 1995, pp. 265-275

[7] P. Caunegre and C. Abraham, "Fault Simulation of Mixed-Signal Systems", *Journal of Electronic Testing:Theory and Applications (JETTA)*, 8 (2), April 1996, pp. 143-152.

[8] L. Whetsel, "Proposal to Simplify Development of a Mixed-Signal Test Standard", *Proceedings of the International Test Conference*, October 20-25, 1996, pp. 400-409.

[9] M. Renovell *et al.*, "Analog Output Response Compaction", *Proceedings of the European Design and Test Conference*, Paris, France, March 17-20 1997, pp. 568-572.

[10]T. Olbrich *et al.*, "A New Quality Estimation Methodology for Mixed Signal and Analogue Ics", *Proceedings of the European Design and Test Conference*, Paris, France, March 17-20, 1997, pp. 573-580.

[11]V. Kaal and H. Kerkhoff, "Compact Structural Test Generation for Analog Macros", Proceedings of the European Design and Test Conference, Paris, France, March 17-20 1997, pp. 581-587.

[12]R. Eschauzier and J. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*, Kluwer Academic Publishers, 1995.

[13]R. Eschauzier, L. Kerklaan , and J. Huijsing, "A 100 MHz 100 Db Operational Amplifier with Multipath Nested Miller Compensation Structure", *IEEE Journal of Solid State Circuits*, vol. 27, no. 12, December, 1992.

[14]R. Eschauzier and J. Huijsing, "An Operational Amplifier with Multipath Miller Zero Cancelation for RHP zero Removal", *Proceedings ESSCIRC*, pp. 122-125, 1993.

[15]R. Hogerwost, R. Wiegerink, P. Jong, J. Fonderie, R. Wassenaar, J. Huijsing, "CMOS Low-Voltage Operational Amplifier with Constant-Gm Rail-to-Rail Input Stage", *Proceedings of ISCAS'92*, pp. 2876-2879, 1992.

[16]R. Rodriguez, J.A. Segura, V.H. Champac, J. Figueras, and J.A. Rubio, "Current vs. Logic Testing of Gate Oxide Short, Floating Gate and Bridging Failures in CMOS", *Proceedings of the International Test Conference*, 1991, pp. 510-519.

[17]D. Vuillaume, A. Bravaix, D. Goguenheim, J.-C. Marchetaux, and A. Boudou, "Comment on 'Hot-Hole-Induced Negative Oxide Charges In n-MOSFET's' ", *IEEE Transactions on Electron Devices*, vol. 43, no. 9, September, 1996, pp. 1473-1477.

[18]T. Shibata and T. Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", *IEEE Transactions on Electron Devices*, vol. 39, no. 6, June 1992, pp. 1444-1455.

[19]T.L. Tewksbury III and H.-S. Lee, "Characterization, Modeling and Minimization of Transient Threshold Voltage Shifts in MOSFETs", *Proceedings of the IEEE 1993 Custom Integrated Circuits Conference*, 1993, pp. 14.4.1-14.4.4.

[20]F. You, S.H.K. Embabi and E. Sanchez-Sinencio, "Multistage Amplifier Topologies with Nested Gm-C Compensation", 1996.

[21]M. Renovell, F. Azais and Y. Bertrand, "A Design-For-Test Technique for Multi-Stage Analog Circuits", *The Fourth IEEE Asian Symposium*, 1995, pp. 113-119.

[22]J. Galiay, Y. Crouzet and M. Verginault, "Physical Versus Logical Fault Models for MOS LSI Circuits: Impact on their Testability", *IEEE Transactions on Computers*, vol. C-29, no. 6, pp. 527-533, June 1980.

[23]A. Balivada, J. Chen, and J.A. Abraham, "Analog Testing with Time Response Parameters", *IEE Design and Test of Computers*, Summer 1996, pp. 18-25.

[24]R.G. Bennets, "Progress in Design for Test: A Personal View", *IEEE Design and Test of Computers*, Spring, 1994.

[25]R.H. Williams and C.F. Hawkins, "The Economics of Guardband Placement", *Proceedings of the IEEE International Test Conference*, Oct. 1993, pp. 218-225.

[26]J. Machado da Silva, J. Silva Matos, Ian M. Bell, and Gaynor E. Taylor, "Mixed Current/Voltage Observation Towards Effective Testing of Analog and Mixed-Signal Circuits", *Journal of Electronic Testing: Theory and Applications (JETTA)*, vol. 9, no. 1/2, August/October, 1996, pp.75-88.