Analysis of Adaptive CMOS Down Conversion Mixers

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Abstract— **Analysis of CMOS direct conversion architecture with adaptive DC offset compensation is presented. Due to process mismatches and local oscillator (LO) crosstalk, DC offsets up to 30mV are observed at the mixer output. For a practical direct conversion or zero-if downconversion system, the incoming RF signal can be as low as -100dBm or few microvolts at this stage and any LO coupling will cause a DC offset orders of magnitude larger than the received signal. The DC offset needs to be effectively reduced to prevent the consecutive gain stages from entering saturation and destroying the RF signal. To achieve this, an adaptive DC shifting circuit is presented. Adding a tunable DC offset on the LO signal can effectively counteract the output DC offset by exploiting the quadratic LO dependence of the process mismatch induced offsets. In addition to that, DSP approaches for adaptively generating the control signals for the DC shifting circuitry are investigated.**

Keywords— **Zero-IF, Direct Conversion, Mixer, DC offset**

I. Introduction

THE increasing demand for low-cost, power efficient and small radio-frequency transceivers requires circuit and architectural breakthroughs. With the continuing developments in the integrated circuit technology, transceiver architectures such as direct conversion is feasible.

The main challenge in the design of single chip superheterodyne receiver is the need for high quality image-rejection filters. These filters are usually off chip discrete components increasing the power consumption and the size of the receiver. In direct conversion architectures, since the IF frequency is zero, there is no need for image-rejection filters. However, as the downconverted band extends to zero frequency, extraneous offset voltages can corrupt the downconverted signal and saturate the following stages [1].

The linearity of an RF mixer such as the Gilbert topology, commonly used in bipolar technology [5] is based on the use of the exponential voltage to current conversion of the bipolar transistors. To obtain reasonable linearity, techniques like predistortion and emitter degeneration are necessary. Imperfections combined with a limited matching will render a third-order intercept point (IM3) which can be slightly larger than 0 dBm. In CMOS, a double balanced structure operating in saturation region can be used for low frequency applications. A better approach [3] is to use the transistors in the linear region where the $V_{GS} - V_T$ can be relatively large. This way a small R_{on} can be realized with small transistors, allowing a high input bandwidth.

II. DC Offset Problem

There are three main cases which result in DC offset voltages at the mixer output. The isolation between the LO port and RF port of the mixer can cause LO-leakage. The coupling between the mixer LO port and the next stage LNA can cause LO leakage. In general, any amount of coupling such as capacitive coupling, substrate coupling and bond-wire coupling from the LO port to the signal path can also cause LO-Leakage. The leaked LO signal is then mixed with itself and produces a DC offset at the output of the mixer. A similar effect occurs when a large interfere leaks from the LNA input and RF port of the mixer to the LO port and it can be time varying. This occurs when the LO signal leaks to the antenna and is radiated and subsequently reflected from moving objects back to the receiver. Apart from self-mixing and interfere leakage, IC imperfections such as process-mismatch can introduce serious amounts of DC at the output of the mixer. While the self-mixing and interfere leakage related DC offset can exhibit a rapid changing nature, process-mismatch related DC offset changes only with temperature variations and aging.

For example, if the LO signal has a peak to peak swing of 0.63V (0 dBm on a 50Ω system) and there is 60 dB of isolation between LO and RFD-input port and the LNA, with LNA/mixer gain of 30 dB, the resulting offset will be on the order of 5 mV while the RF signal level at this point can be as low as $30\mu V_{rms}$ [1].

One way to eliminate the DC offset is to AC couple (high-pass filter) the RF port with corner frequency of lower than 0.1% of the bit rate to avoid corrupting the received signal. This, in turn, yields a slow response to changes in the offset and requires large capacitor and resistors. Using high-pass filter wrong initial conditions can cause a temporary loss of data as well. Methods other than high-pass filtering the mixer output needs to be developed for a realizable direct conversion receiver design.

III. CMOS Mixer Parameters

Consider the high-frequency double balanced CMOS downconversion mixer architecture presented by [3] in Figure 1.

The CMOS mixer shown consists of two blocks. The first block is a double balanced structure which consists of four NMOS transistors that are biased in the triode region.

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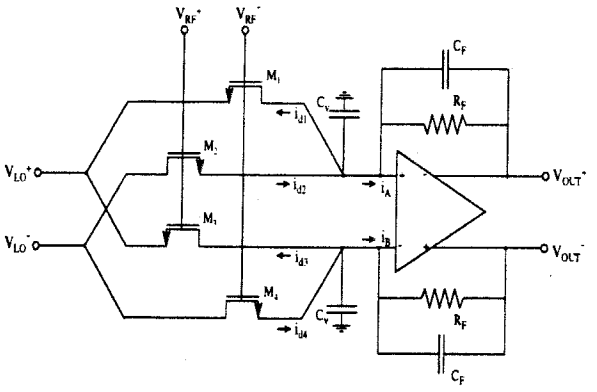


Fig. 1. The mixer architecture.

The output of this block is multiplication of the two differential inputs in terms of differential currents. The second block is the operational amplifier in a $R_F - C_F$ negative feedback configuration which serves as a current difference to voltage difference converter and a lowpass filter. The capacitors connected to the inputs of the operational amplifier establish virtual ground nodes at the input which has a limited bandwidth. In fact, the bandwidth of the operational amplifier has to be larger than the baseband signal. The currents flowing through the triode biased NMOS transistors can be formulated as:

$$i_{d1} = -\beta_1(V_{RF}^- - V_{LO}^+ - V_{tn1} + \frac{V_{LO}^+}{2})V_{LO}^+, \quad (1)$$

$$i_{d2} = \beta_2(V_{RF}^+ - V_{tn2} - \frac{V_{LO}^-}{2})V_{LO}^-, \quad (2)$$

$$i_{d3} = -\beta_3(V_{RF}^+ - V_{LO}^+ - V_{tn3} + \frac{V_{LO}^+}{2})V_{LO}^+, \quad (3)$$

$$i_{d4} = \beta_4(V_{RF}^- - V_{tn4} - \frac{V_{LO}^-}{2})V_{LO}^-, \quad (4)$$

where β is equal to $\mu_n C_{ox}(W/L)$. The mixer output neglecting the finite bandwidth of the operational amplifier structure is given as,

$$V_{OUT}^+ - V_{OUT}^- = R_F[\,(\beta_3 V_{RF}^+ - \beta_1 V_{RF}^-)V_{LO}^+ - (\beta_2 V_{RF}^+ - \beta_4 V_{RF}^-)V_{LO}^- + (\beta_3 V_{tn3} - \beta_1 V_{tn1})V_{LO}^+ + (\beta_2 V_{tn2} - \beta_4 V_{tn4})V_{LO}^- + (\beta_3 - \beta_1)(V_{LO}^+)^2/2 - (\beta_2 - \beta_4)(V_{LO}^-)^2/2\,]. \quad (5)$$

After lowpass filtering, the output of the mixer reduces to

$$V_{OUT}^+ - V_{OUT}^- = \beta R_F(V_{LO}^+ - V_{LO}^-)(V_{RF}^+ - V_{RF}^-) + \Delta\beta R_F(V_{LO}^+ - V_{LO}^-)^2, \quad (6)$$

where β and $\Delta\beta$ can be defined as,

$$\beta = \frac{1}{4}(\beta_1 + \beta_2 + \beta_3 + \beta_4) \quad (7)$$

$$\Delta\beta = \frac{1}{4}(\beta_3 + \beta_4 - \beta_1 - \beta_2). \quad (8)$$

The process mismatch indicated here with the parameter $\Delta\beta$ gives rise to a quadratic LO signal at the output of the mixer. The effect of the process mismatch for this architecture is very similar to the self-mixing phenomenon.

To achieve stable operation, the NMOS transistors need to be biased in triode region and the dc biasing levels must be chosen carefully [3].

IV. Process Mismatch

The process mismatch can introduce a quadratic LO dependence at the output of the mixer. To be able to quantitatively analyze this effect, the order of the possible process mismatch needs to be determined [4].

The mismatch that occurs among the parameters of equally designed CMOS transistors is the result of several random variables. For a given parameter P it's mismatch is usually assumed to have a normal distribution as ΔP. For small variations, the mismatch of the transistors β's can be modeled as [4]:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_W^2}{WL} + \frac{A_L^2}{WL^2} + \frac{A_\mu^2}{WL} + \frac{A_{C_{ox}}^2}{WL} + S_\beta^2 D_2 \simeq \frac{A_\beta^2}{WL} + S_\beta^2 D_2, \quad (9)$$

where $A_W, A_L, A_\mu, A_{C_{ox}}$, and S_β are process-related constants. The relative mismatch in the current factor β is inversely proportional to the area of the transistors as expected. For sub-micron process, the mismatches (i.e., $\sigma(\beta)/\beta$) can range from 0.2% to 0.8% [4].

V. Compensation Methods

In this section two DC offset removing approaches are proposed, a DC level shifting circuit is investigated and DSP approaches for sensing the DC offset are investigated.

A. Feed-forward DC offset compensation

The system level description of the feed-forward approach is presented in Figure 2. The RF signal at the output of the mixer is fed to an A/D converter and the DC value of the signal is measured. When the received signal strength is high enough, signal variations are partially represented at the output of the A/D block. Using this method, the mean of the signal is traced in the DSP domain. Different approaches for effectively extracting the mean of the noisy signal will be discussed later in this section. The estimated DC offset which is the error signal is fed through a control algorithm which can be as simple as a look-up table. The output of the control unit is fed to a latch and is updated periodically. Choosing the update period as large as the DC offset variations, the noise contribution due to the DC level shifter becomes limited.

The aim of this approach is not to completely remove the DC offset, but reducing it's magnitude to a level where it does not saturate the following stages. The same compensation technique should be applied in the following stages until the A/D converter right before the detector is reached.

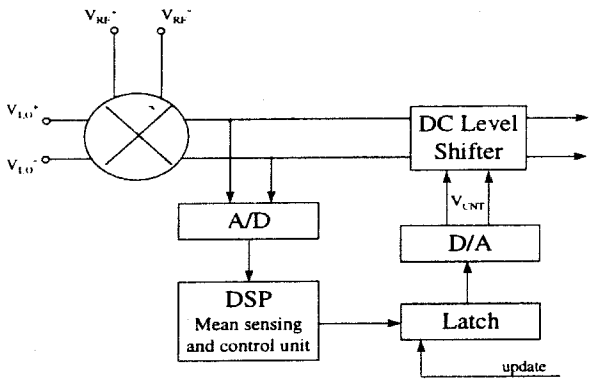


Fig. 2. Feed-forward DC offset compensation.

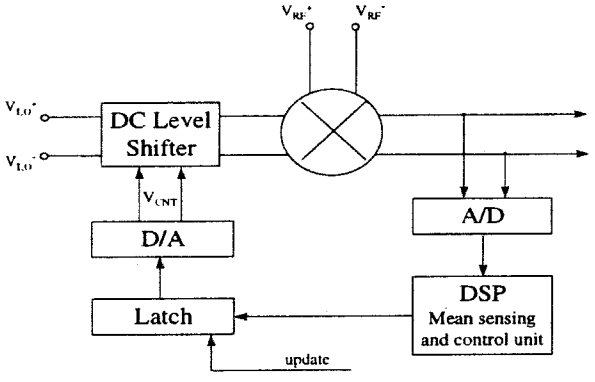


Fig. 3. Feed-back DC offset compensation.

This way, although the DC offset is not completely removed, it's effect is suppressed to avoid saturation.

B. Feed-back DC offset compensation

As shown in Section 3, the process mismatch induces a quadratic LO component at the output of the mixer. Hence, if a proper DC offset on the LO signal is induced, this quadratic dependence can be exploited for compensation. The system level diagram of the feed-back DC offset compensation is shown in Figure 3.

As in the feed-forward compensation approach, the DC offset is sensed through an A/D converter and its mean is computed. The control block produces the corresponding control signal which can have high frequency noise contributions as the mean estimate of the signal may not be exact. Thus a latch with periodical update signal is necessary and the update period should be chosen as large as the DC offset variations permit.

C. The Level Shifting Circuit

A wide-band unity gain level shifter is introduced in Figure 4. It is composed of two common source amplifiers with adaptively biased NMOS loads [9]. By changing the load bias voltages, the differential DC component of the output can be modified. The mismatch in the NMOS transistors, as well as the threshold voltage difference resulting from the body bias change manifests itself in form of a gain deviation between the branches. Due to this gain deviation, the differential mode gain of the circuit can deviate from unity and a common mode DC offset is introduced at the output. Although the gain deviation may pose a problem for the operation of the receiver, the common mode portion of the offset is immediately rejected by the common mode r ejection ratio (CMRR) of the following differential stage.

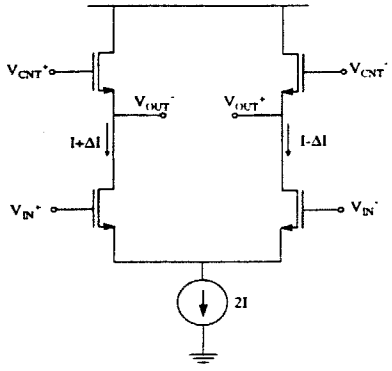


Fig. 4. The unity gain, wide-band level shifter circuit.

D. Removing the High Frequency Terms of the DC Offset

The LO leakage and the interferer leakage induced DC offset is rapidly changing where the process mismatch related offsets are temperature and aging dependent and do not exhibit rapid variations. For the previously discussed compensation schemes to be effective, the DC offset at the output of the mixer needs to be as slowly changing as possible. To achieve this goal the circuit configuration in Figure 5 is proposed.

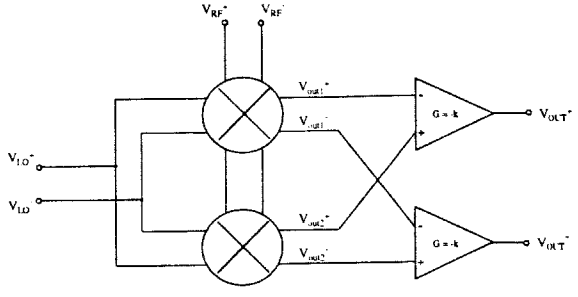


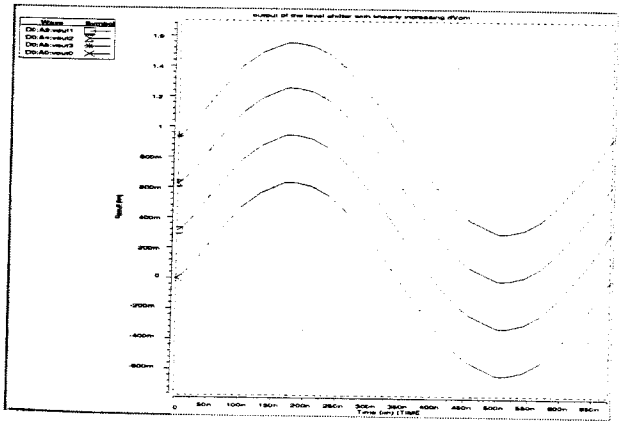
Fig. 5. Differential mixing configuration.

With careful symmetrical layout, the distance between the LO port of the first mixer to RF and the LO port of the second mixer to RF can be matched. This way if LO leaks to RF, negative LO signal will leak to the opposite port effectively canceling the LO leakage related DC offset.

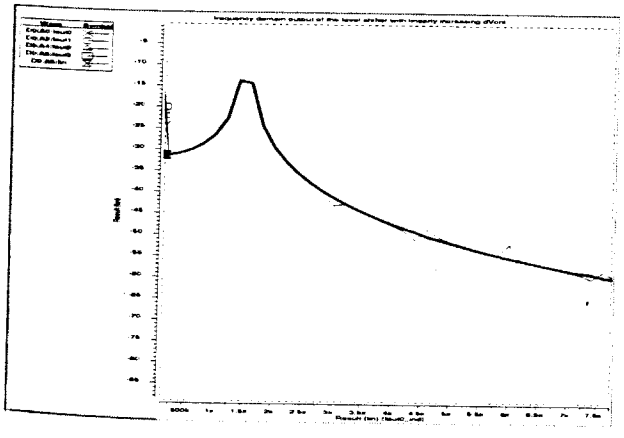
At the same time, if an interfere leaks to the LO port of the first mixer, it also leaks to the LO port of the second mixer. By subtracting the output of the second mixer from the first mixer this interfere leakage dependent term is canceled out. The price for this approach is the doubled variance of the random but low frequency DC offset at the output of the mixer.

VI. Results and Discussion

In this section simulation results for the DC level shifter circuit and the LO controlled DC offset compensation are presented. A level shifter circuit to be used with the feed-forward approach is designed and simulated via HSPICE. The time and frequency domain behavior of the circuit is presented in Figure 6. The bold curve in Figure 6b represents the input signal which is chosen to be a pure sinusoid. Note that the output of the circuit does not have a significant additional distortion for shifts up to 1 Volt. The input signal is chosen to be a 1.5MHz, 0dBm with 50Ω termination.



(a)



(b)

Fig. 6. The HSPICE simulation plots for the unity gain level shifter circuit presented in Section 3. (a) Time domain output, (b) Frequency domain behavior (bold is the input signal).

For the feed-back DC offset compensation, the effect of changing the DC offset of the LO signal is demonstrated in Figure 7. The DC offset induced by the process mismatch is effectively canceled out by applying a differential DC shift of approximately 0.324V on the LO signal.

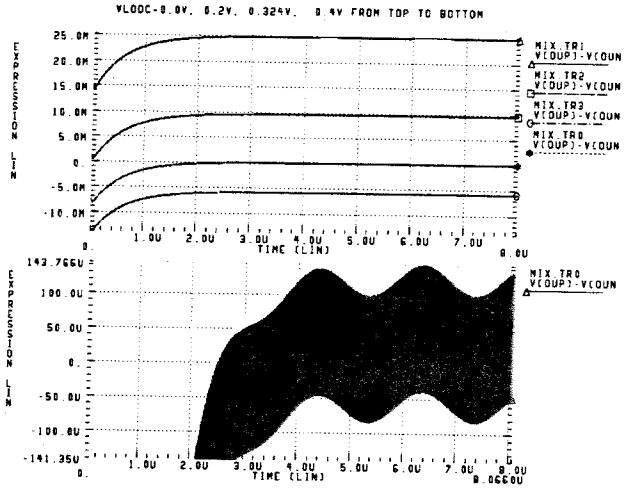


Fig. 7. DC offset compensation by adding a DC offset on the LO signal, V_{LODC} is changed from 0V to 0.4V.

In this paper, the DC offset problem for zero-IF receivers are investigated. The reasons, drawbacks and expected magnitudes are analyzed and two different compensation techniques with an additional system level configurations are proposed. The results presented here demonstrate a potential alleviation to the DC offset problem.

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