Issues in the Design of Domino Logic Circuits

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***Abstract** - Domino logic circuits have become extremely popular in the design of today's high performance processors because they offer fast switching speeds and reduced areas. However, the use of domino logic introduces many design risks because it is very sensitive to noise, circuit and layout topologies. This paper identifies issues that might cause domino logic circuits to fail, and discusses some possible solutions to alleviate these problems.*

I. Introduction

As frequencies of processors increase, domino logic is becoming the circuit style of choice to implement critical paths because it offers significantly faster switching speeds than other circuit styles. Domino logic circuits also occupy smaller areas which makes their use all the more attractive. However, these advantages do not come without drawbacks. Domino logic is very sensitive to noise, circuit, and layout topologies. Therefore its use introduces many design risks and increases the effort needed to verify its functionality and performance.

To better understand the noise sensitivity of a domino logic gate, a brief introduction to this circuit style is provided.

A. Single-rail domino logic

A simple single-rail class I domino gate is shown in Fig. 1(a). A domino gate consists of an Nfet dynamic logic circuit cascaded into a static inverter. The output of this domino stage is Y = A · B.

The circuit operation is synchronized by the clock signal CLK. Precharge occurs when the clock is at CLK = 0. During the precharge phase, P0 conducts to charge the internal node capacitance CX0 to a voltage $V_{X0} = V_{DD}$. The output of the inverter, which is also the output of the domino gate, is therefore at 0V. Evaluation takes place when CLK = 1. During the evaluate phase P0 turns off and N0 is driven into a conducting state and the node X0 undergoes a conditional discharge. If A and B are high, V_{X0} falls to 0V, and the output Y rises. But, if either one of the inputs is low, there is no conduction path to ground and V_{X0} must be maintained at a voltage level greater than V_{IH}. This is when the node X0 becomes dynamic, and this domino gate is susceptible to noise on its input signals (A, B), internal dynamic node (X0), and power rails. These noise events might corrupt the state stored on the dynamic node and result in the incorrect evaluation of this gate.

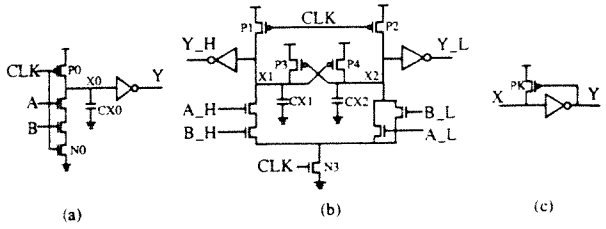

Fig. 1. (a) Single-rail class I domino gate (b) Dual-rail class I domino gate (c) Keeper.

B. Dual-rail domino logic

A dual-rail class I domino gate is shown in Fig. 1(b). This gate implements a 2-input AND (Y_H = A_H · B_H) and NAND (Y_L = A_L + B_L) function. The dual-rail domino gate allows for the implementation of active rising edge inverting signals and overcomes the non-inverting characteristic of single-rail domino gates. This circuit also has cross-coupled Pfets (P3, P4) that help improve its noise margin.

The operation of this gate is similar to that of a single-rail domino gate. In the precharge phase (CLK = 0), both precharge transistors P1 and P2 conduct and charge the internal node capacitances CX1 and CX2 to V_{DD}. Therefore the cross-coupled Pfets are off. Both the outputs, Y_H and Y_L are at 0V. During the evaluate phase (CLK = 1), both P1 and P2 turn off and N3 is driven into a conducting state and based on the inputs (A_H, A_L, B_H, B_L), one of the precharged nodes (X1, X2) is discharged. If A_H and B_H are high, V_{X1} falls to 0V. The cross-coupled Pfet P3 does not fight this discharge because it is off. The other cross-coupled Pfet, P4 turns on and helps attenuate any noise events

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that might disturb the voltage level on node X2. The output Y_H rises, and the output Y_L stays low.

The cross-coupled Pfets do not allow the precharged nodes to be undriven for any significant period of time and do not degrade the performance of the dual-rail domino gate by fighting the discharge current. Therefore their use improves the noise margin of the dual-rail domino gate without significantly effecting its switching speed.

In the following sections of this paper a few issues that might cause domino logic circuits to fail are identified, and some possible solutions to alleviate these problems are discussed.

II. Charge leakage

During the evaluate phase if the dynamic node is storing a logic 1 state, leakage currents will alter the value of the voltage stored. Therefore the dynamic node may not be able to hold this state for a long time. If a feedback Pfet PK (as shown in Fig. 1(c) is added, it will replenish the charge lost to leakage and help the domino gate operate at slow clock frequencies. However, if the output is true during the evaluate phase, the feedback Pfet fights the discharge current and slows down the evaluation of this domino stage. For this reason, PK is made weak.

Another method to reduce leakage is to increase the channel length of the Nfets in the dynamic logic circuit. Increasing the channel lengths of these devices reduces subthreshold leakage but unfortunately, reduces the current drive of the Nfets and therefore results in a decrease in performance. This method is especially attractive for process technologies in which LV_t devices are used [1].

III. Crosstalk

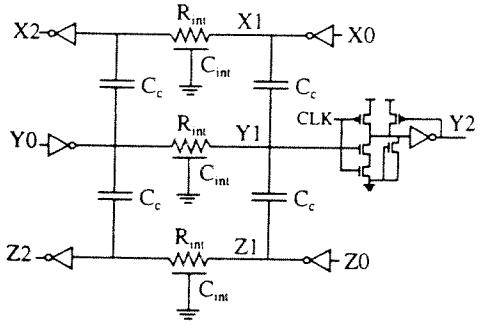

Fig. 2. Simplified model for crosstalk simulations.

A domino gate is susceptible to noise on its inactive low input signals if the precharged node is storing charge during the evaluate phase. Noise on the input signals can be generated as a result of crosstalk. The mechanism of generation of this noise event is illustrated in Fig. 2. When the aggressor nets X1 and Z1 switch, capacitive coupling between them and the victim net Y1 can result in the degradation of the logic state of this net. If Y1 is the input of a domino gate as shown in Fig 2, there might be a conduction path from the precharged node to ground which can result in a loss of the state stored, and a logic failure of this domino stage. This logic failure cannot be recovered from by slowing down the clock because domino circuits do not have a regenerative mechanism that can help restore the state of the precharged node. Fig. 3 shows the magnitude of the crosstalk induced (Vc) on the far end of the inactive low victim net Y1 when both aggressor nets X1 and Z1 rise simultaneously for a set of different net lengths. Both aggressor drivers have an input slew rate of 200 ps, and the victim to aggressor gate width ratio is 1. The peak of Vc is very large, and in most cases, is much larger than the V_t of an Nfet. Also, the pulse width of this noise event can be a very significant fraction of the clock cycle of a high performance processor. Glitches of this amplitude and duration on input signals can lead to functional failures in domino logic circuits [2].

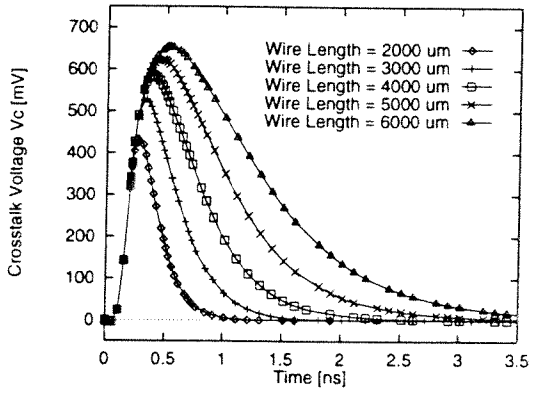

Fig. 3. Crosstalk voltage dependence on wire length.

The domino gate is also susceptible to noise on the precharged node if it is storing charge during the evaluate phase. Just like noise on the input signals, noise on this node can be generated by crosstalk. Potential aggressors could be nets that are running parallel to the precharged node, or on top of it on a higher level of metal. The aggressors can couple to and remove charge from the precharged node. This can result in the voltage level on this node falling below the V_{IH} of the static inverter and cause a logic failure in this domino stage. This logic failure too cannot be recovered from by slowing down the clock.

As Fig. 4 illustrates, coupling also effects delay. If the victim net Y1 rises and the aggressor nets X1 and Z1 fall simultaneously, the effective coupling capacitance is doubled. Also as the victim to aggressor gate width ratio reduces, coupling increases. This results in an increase of the normalized propagation delay which is a ratio of delay that comprehends coupling ($T_{d,crosstalk}$), delay that does not (T_d). For a

victim to aggressor gate width ration of 1, $T_{d,crosstalk} \sim 2 \cdot T_d$. Therefore, the performance of a domino pipeline can be severely degraded if there is adverse coupling. Similarly, if all the nets X1, Y1, and Z1 rise simultaneously, there can be a significant decrease in delay. Depending on clocking and latching schemes, this can lead to short circuit power dissipation, hold-time, or race-through problems. Therefore coupling can result in timing related failures in domino logic circuits as well.

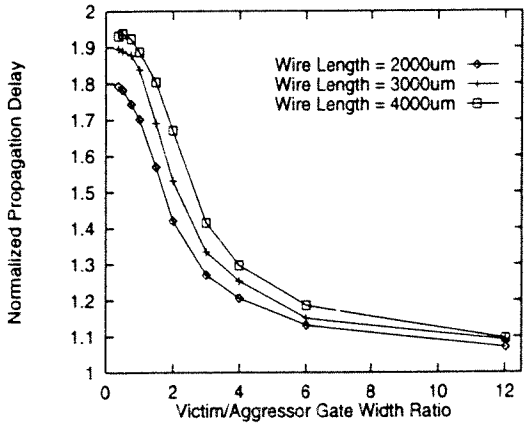

Fig. 4. Delay ratio $T_{d,crosstalk}/T_d$ vs. victim/aggressor gate width ratio.

As a result of technology scaling and higher operating frequencies, coupling and coupling induced noise is increasing [3]. Therefore it becomes all the more important to reduce coupling when designing a domino pipeline for one of today's high performance processors. Coupling is a function of the length of victim and aggressor net adjacency, victim to aggressor net spacing, victim driver impedance, and the aggressor slew rate. Therefore crosstalk can be reduced by manipulating any one of these variables.

A. Reducing the length of adjacency

As Fig. 3 shows, reducing the length of victim and aggressor net adjacency reduces the peak crosstalk voltage and the pulse width of the induced noise significantly. Therefore limiting the length of the input signal into a domino gate will ensure that the crosstalk on this net does not exceed the design constraint.

Similarly, reducing the length of the precharged node to the minimum required will reduce the coupling to this node. Also, an effort should be made to isolate this node from other signals so that there can be no potential aggressors. This includes eliminating crossovers in higher levels of metal. If routing tracks are not available and signals need to be run over the precharged node, the impact of these signals on crosstalk to this node should be assessed and the number of signals allowed to run over the precharged node should be limited accordingly. For example, if a certain precharged node of a domino gate can have only one crossover, then a set of mutually exclusive signals can be run over it. This will help with the efficient use of routing tracks while ensuring that only one of these signals could possibly couple to the precharged node.

B. Increasing the victim to aggressor net spacing

As Fig. 5 illustrates, increasing the victim to aggressor net spacing is another method of reducing crosstalk. Increasing the spacing from 0.49 μm to 0.98 μm reduces the crosstalk significantly. Any further increase in spacing results in diminishing returns.

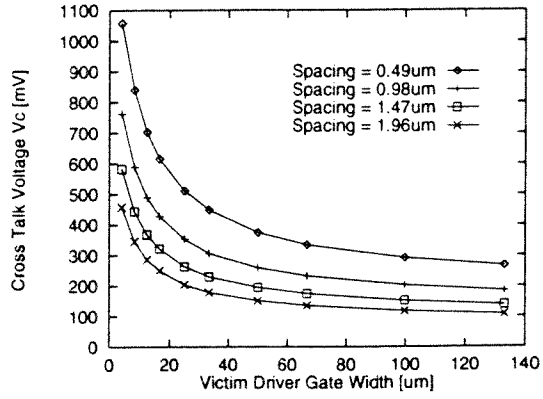

Fig. 5. Crosstalk vs. wire spacing and victim driver size.

C. Decreasing the victim driver impedance

Fig. 6 shows how crosstalk on the input signals of a domino gate can be reduced by reducing the victim driver impedance. However, the neighboring wires of the victim driver could be inputs of other domino gate. Therefore care should be taken when using this method to reduce crosstalk because increasing the victim driver size could result in it becoming an aggressor when it switches.

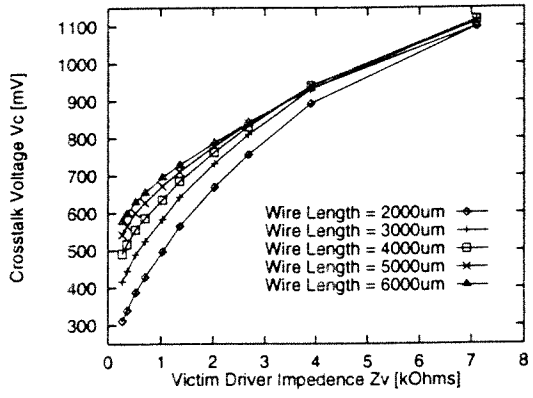

Fig. 6. Crosstalk vs. wire length and driver impedance.

D. Shielding

If none of the solutions discussed above help, then another solution to reducing crosstalk is to shield the victim net. Shielding is by far the most effective method to reduce crosstalk but it results in an inefficient use of the tracks available for routing. With careful planning a scheme can be devised to distribute power while using the power supply rails to shield sensitive nets from potential aggressors like the clock. Also, mutually exclusive signals (like propagate, generate, and kill in a carry-lookahead adder) can be run parallel to each other, albeit for a limited length. In the evaluate phase only one of these signals can rise and therefore the inactive low signals can have only one aggressor which will reduce crosstalk significantly. The mutually exclusive signals should not be run adjacent to each other for long lengths because the net that is switching may couple to one of the inactive low nets, and because of resistive shielding the victim driver may not be able to hold down that net at the far end.

Any of the solutions described above, or a combination of them can be used to reduce crosstalk.

E. The effect of aggressor slew rate on crosstalk

Fig. 7 is a plot of victim driver gate width versus crosstalk voltage on the victim net for a set of different aggressor slew rates. As this figure illustrates, crosstalk reduces as the slew rate of the aggressor nets reduce. However, reducing the slew-rate of the aggressor nets may not be a practical solution to reducing crosstalk.

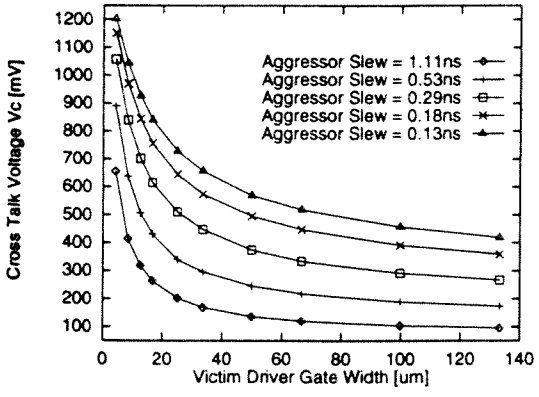

Fig. 7. Crosstalk vs. aggressor slew and victim driver size.

The feedback Pfet PK described in section II assists the recovery of the precharged node from noise events, but this recovery is very slow. Therefore the feedback Pfet cannot attenuate any noise events that have a large pulse width.

In a stacked structure, the lower Nfets have a larger V_{GS} and a smaller V_t than the higher Nfets. Therefore AND domino gates are more susceptible to noise on the inputs that are closer to ground. For similar reasons, OR domino gates are more sensitive to noise on their inputs than AND domino gates. Also, single-rail domino gates are more susceptible to noise than dual-rail domino gates. These are some issues that should be kept in mind when designing domino logic circuits.

IV. Charge Sharing

Fig. 8 (a) shows a single-rail class I domino gate that implements a 4-input AND function (Y = A · B · C · D). If the input pattern is A = B = C= 1, and D = 0 during the evaluate phase, this gate has to maintain a logic 1 voltage ($V_{X0} > V_{IH}$) on the capacitor CX0. But, the value of this voltage can be degraded, and can fall below V_{IH} due to charge sharing between CX0 and the internal parasitic capacitances CX1, CX2, and CX3. This can result in a logic failure of this gate.

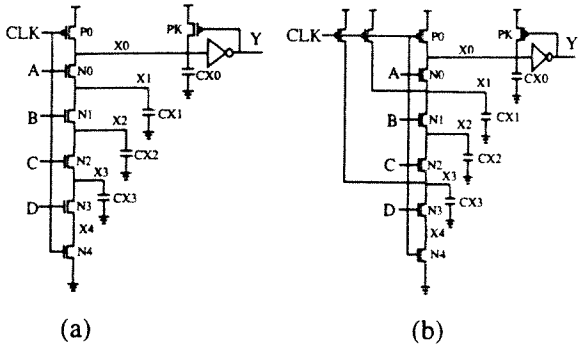

Fig. 8. (a) 4-input class I domino AND gate without precharge Pfets (b) with precharge Pfets.

If the number of stacked Nfets is increased, charge sharing becomes a bigger problem because the number of internal parasitic capacitances that can potentially share charge with CX0 increases. Therefore charge sharing is one of the factors that limits stack height.

The feedback Pfet PK described in section II assists the recovery of the precharged node by supplying charge lost to charge sharing, but this recovery is very slow. Therefore using the feedback Pfet alone does not provide a very effective solution to reducing charge sharing. Noise problems due to charge sharing can be almost eliminated by precharging internal nodes with the use of minimum size Pfets as shown in Fig. 8 (b). Since CX1 and CX3 are precharged to V_{DD}, CX0 does not have to share charge with any of the internal capacitances. Therefore V_{X0} is not degraded and can be held at a logic 1 voltage. This method of reducing charge sharing though results in an increase in gate delay because more capacitances have to be discharged if the output is true.

For the domino gate shown in Fig. 8, precharging an internal node closer to the precharged node results in a larger gate delay but lesser charge sharing problems; precharging an

internal node closer to ground results in a smaller gate delay but more charge sharing.

Another method to reduce charge sharing is to increase the size of the static inverter. This increases CX0 and because the ratio of this capacitance to the internal parasitic capacitances increases, charge lost to charge sharing reduces.

From a layout perspective, charge sharing can be alleviated by reducing the capacitance of all internal nodes. If a scheme for precharging internal nodes has already been chosen, special attention should be given to reducing the capacitance of the non-precharged nodes.

V. β ratio of static inverter

In domino logic circuits, the evaluation transition is more critical. Therefore, the static inverter is usually skewed so that it produces a very fast rising transition in response to a falling transition on the precharged node. This helps reduce the gate delay of domino circuits significantly. However, making β_p much larger than βn results in the reduction of the high noise margin, NMH = V_{DD} - V_{IH}. As we have already discussed in previous sections, if the precharged node is storing a logic 1 voltage, this voltage should be always greater than V_{IH}. Therefore, skewing the static inverter makes the domino gate more susceptible to all noise events.

Skewing the static inverter results in a very slow precharged transition. If class I domino stages are cascaded into class II domino stages (class II domino circuits are class I domino gates shown in Fig. 1 without the clocked Nfets N0, and N3) to reduce clock loading, very slow precharge times will result in a lot of short-circuit power dissipation in the class II domino circuits because the evaluate Nfets may not be turned off when precharge begins. Short-circuit power dissipation can be reduced by making the precharge Pfets larger to reduce the precharge times. But, this will result in an increase in clock loading. Another solution could be to delay match the clock and data inputs for each class II domino stage by adding clock buffers. But, this can result in the duty cycle reduction which reduces the time available for precharge. To compensate for this, the precharge Pfets downstream in a domino pipeline will have to be made larger. This will again result in an increase in clock loading.

Therefore, when choosing a β ratio, its implications on NMH, short-circuit power dissipation, clock loading, and clock duty cycle should be examined.

VI. Power supply variations

Fig. 9 illustrates how power supply variations due to IR drops, instantaneous voltage, or ground bounce present yet another problem to the design of domino logic circuits. If during the evaluate phase signal X1 is low, the domino gate is storing a logic 1 voltage on its precharged node Z1. Now if Gnd0 were to bounce, V_{X1} would be offset by the magnitude of the bounce. Therefore V_{X1} - V_{Gnd1} would not be equal to 0V. If V_{X1} - V_{Gnd1} were large enough (greater than, or equal to V_{tn}), there could be a conduction path from the precharged node to ground which would result in a loss of the state store, and a logic failure of this domino stage. This problem can be solved by making the power rails stiffer by the use of decoupling capacitors. Another method to solve this problem is to have the driver and the domino gate it drives, share the same power rails. Also, staggering the switching of different domino stages within a domino pipeline reduces the peak current at any instant of time, and therefore reduces the peak value of the ground bounce.

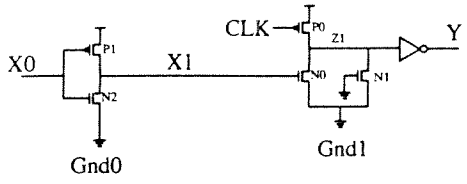

Fig. 9. Circuit schematic used to illustrate the effect of power supply variations on domino logic circuits.

VII. Substrate charge injection

If nodes make excursions outside the power supply rails, they can inject charge into the common substrate. Fig. 10 (a) and (b) show the mechanism of generation of this noise. If Y1 is low, and is coupled to by X1 and Z1 making falling transitions, Y1 can be coupled below ground. This results in the pn junction formed by the drain of the Nfet in INV1 and the substrate becoming forward biased and injecting electrons into the common substrate. These electrons can then be easily picked up by the reverse biased pn junction formed by the drain of the Nfet N0 and the substrate and result in the discharge of the charge stored on CD.

If there are no precharged nodes within a certain radius of a minority carrier injector, there is no need for any fixes. However, if there happens to be a precharged node in the vicinity of a minority carrier injector, an attempt should be made to fix the problem that causes the node to make excursions outside the power supply rails. In this case reducing the crosstalk should alleviate the problem. However, if such a fix cannot be made and nodes still make excursions outside the power supply rails, then a guard band should be placed between the injector and the precharged node (as shown in Fig. 10 (c)).

VIII. α - particles

Flip-chip technologies make use of solder balls. These solder balls contain traces of unstable lead isotopes that emit α-particles. Fig 10 (d) illustrates how α-particles could upset