# MULTIPLE-VALUED LOGIC VOLTAGE-MODE STORAGE CIRCUITS BASED ON TRUE-SINGLE-PHASE CLOCKED LOGIC

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## ABSTRACT

A number of novel voltage-mode multiple-valued logic circuits are introduced. Adopting the main features of the true single-phase clocked logic, efficient quaternary logic dynamic and pseudo-static latches, dynamic and static master-slave storage units, and uni-signal controlled pass gates are proposed. These circuits use two kinds of MOS transistors, i.e., enhancement and depletion mode, each of which has two threshold voltages. The proposed circuits exhibit regular, modular, and iterative structure, which means that the MVL circuits are VLSI implementable and can be easily re-designed for any radix of an arithmetic system. Since we use only clock signal, the derived circuits have low power dissipation. Comparisons with existing circuits prove substantial improvements in terms of speed, power consumption, and transistor count.

## 1. INTRODUCTION

Multiple-valued Logic (MVL) circuits have been attracting researchers in recent years, the reason stems from the fact that some critical features related to the reduction of the number of the interconnections and the increased information content per unit area [1-3]. The current VLSI technology can support the fabrication of MVL circuits. Two kinds of MVL circuits based on MOS technology have been developed, namely the current-mode MVL circuits and the voltage-mode MVL circuits. Although many efficient current-mode circuits have been presented [4], the critical problem of the power dissipation, due to the continuous current flow, puts these circuits under consideration. A number of research papers have been published for implementing voltage-mode MVL circuits [5-8]. In particular, some voltage-mode circuits with many threshold voltages for each transistor type, whose number depends on the radix, were presented [5, 6]. However, these circuits required increased number of the manufacturing processes to achieve the multiple thresholds and thus, increased design cost. In [7, 8] a set of dynamic circuits with multi-phase clock schemes have been proposed. However, they had the known problems of the dynamic circuits, such clock race, charge redistribution, etc.

In this paper, a set of novel voltage-mode MVL circuits, namely the dynamic and pseudo-static latches, the dynamic and static master-slave storage units, and the uni-signal controlled pass gate are introduced. Although the proposed circuits are designed and simulated for quaternary logic, they can easily re-designed for any arithmetic base (or radix), since the corresponding architectures exhibit regular, modular, and iterative structure. The proposed circuits are characterized by two threshold voltages for each type of MOS transistor and can function with only one control signal (usually a clock), i.e., its complementary form is not needed. Exploiting the latter useful feature, one can avoid clock race problems, designing MVL data paths similar to the True Single-Phase Clocked Logic (TSPCL) [9] approach of the binary logic. The existence of TSPCL design style ensures that the proposed circuits exhibit low power consumption.

Comparing the introduced pseudo-static MVL latch with an existing circuit [11], it is concluded that the proposed circuits exhibit substantially-improved features such as small number of transistors (i.e., small area), low power consumption, only one clock signal, and high performance (i.e., speed).



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## 2. THE PROPOSED VOLTAGE-MODE MVL CIRCUITS

As it has already been mentioned, a quaternary arithmetic system is chosen. The relations between the used logical values and voltage values are shown in Table 1. For simplicity reasons, the voltage values coincide with the corresponding logical values.

Using both enhancement-mode and depletion-mode MOSFETs of 0.7 μm technology, the introduced voltage MVL circuits can be constructed. These circuits are designed by Cadence CAD tool and their operation is verified by SPICE (Level 2). The specified device parameters of the used transistors are shown in Table 2.

| **Logical values** | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| **Voltage (Volts)** | 0.0 | 1.0 | 2.0 | 3.0 |

**Table 1:** Correspondence between the logical values and voltages.

| **Transistor type** | $V_{TH,0}$ **(Volts)** | $V_{TH}$ **($V_{BS}$=0) (volts)** | $V_{TH}$ **($V_{BS}$=±3) (Volts)** |
|---|---|---|---|
| enhancement -mode n-MOS | 0.307 (calculated ) | 0.262 | 0.737 |
| enhancement -mode p-MOS | -0.307 (calculated ) | -0.267 | -0.733 |
| depletion-mode n-MOS | -0.697 (defined) | -0.733 | -0.267 |
| depletion-mode p-MOS | 0.694 (defined) | 0.732 | 0.268 |

TOX = 170 Å (Oxide thickness)
NSUB: Substrate doping, NSUB=3.1 ×10[16]  $V_{TH,0}$: Zero-bias threshold voltage

**Table 2:** The 0.7 μm technology parameters of MOS transistors

## 2.1 QUATERNARY VOLTAGE-MODE LATCHES

The proposed MVL latches consist of three introduced basic building units, namely the *inverter-based unit*, the *TSPCL-based output unit*, and the *uni-signal controlled pass gate*. The main features of the building blocks of the proposed latches as well as the function of the proposed latches are presented in the next paragraphs.

### 2.1.1 Inverter-based unit

The architecture of the inverter-based unit for quaternary logic is shown in Fig. 1. This circuit is similar to the level corrector circuit presented by Watanabe *et al* [10]. The proposed circuit exhibits regularity and modularity, design properties which make the inverter-based units VLSI implementable. Also, the iterative structure of the proposed circuit ensures the derivation of similar structures for any radix ($k \geq 2$). The proposed circuit performs voltage level correction, i.e., it produces the exact logic level voltage, when the input voltage value has small difference from the precise voltage value of the associated logic level.

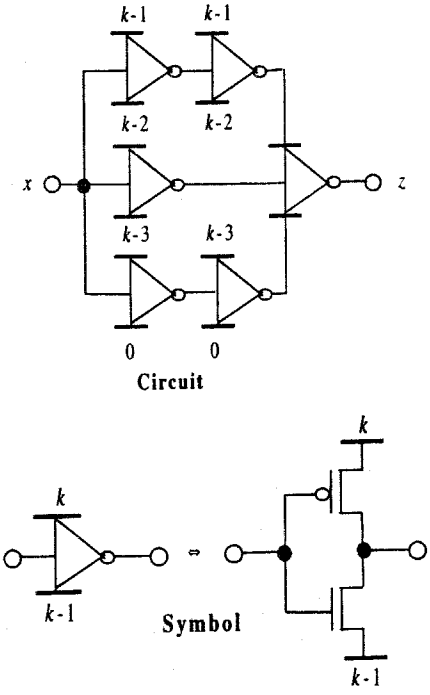



**Figure 1:** The Inverter-based unit for quaternary logic voltage-mode latches.

### 2.1.2 MVL uni-signal controlled pass gate

The circuit implementations of the proposed uni-signal controlled pass gates are depicted in Fig. 2. More specifically, the pass gate shown in Fig. 2(a) allows the propagation of a signal from input $x$ to the output $y$ when the control voltage is in high level (logic level 3), while the second pass gate when the control signal is in logic level 0. Each pass gate circuit consists of three enhancement and one depletion transistor. The proposed pass gates use only one control signal (and not its complementary form), which means smaller switching activity of the MOS transistors and therefore, less power

dissipation. Furthermore, the proposed gates can function at any radix, $k$, of an arithmetic system.

Assuming a quaternary system ($k$=4), the detail description of the function of the pass gate shown in Fig. 2(a) follows. When the control signal is in high level (logic level 3) the transistor $M_1$ conducts. If the input signal is in logic level 3, the output voltage, $y$, of the node $x$ reduces to the voltage 3-$V_{TH}$ volts, since the nMOS transistor $M_1$ does not conduct under its threshold voltage ($V_{TH}$ denotes the threshold voltage). In contrast, the signal $x$=3 passes through the transistors chain $M_2$-$M_3$-$M_4$ without any modification. If $x$=0, the signal through $M_1$ remains unchanged. The transistors $M_2$ and $M_4$ do not allow the flow of leakage current from the node $x$ to $y$ or vice versa. The existence of leakages would mean modifications in the voltages of the input and output nodes and eventually, extra power dissipation.

The pass gate of the Fig. 2(b) has similar operation to that pass gate of Fig. 2(a).

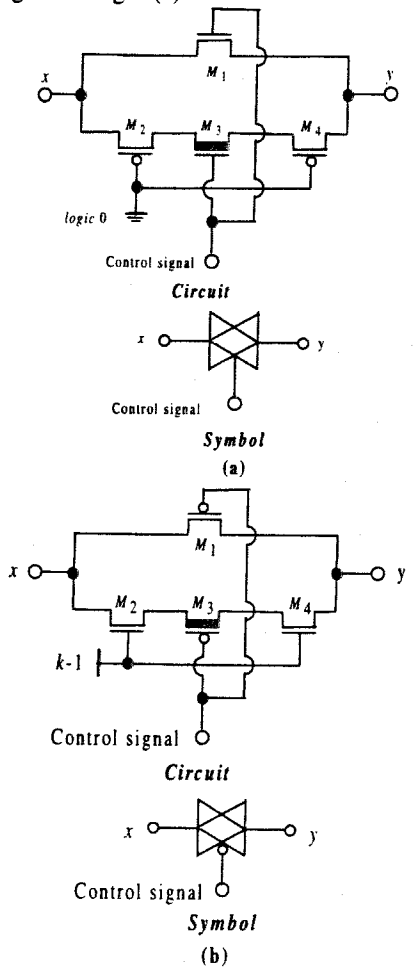



**Figure 2:** The proposed uni-signal controlled pass gates: (a) an input signal passes when the control voltage is in logic level $k$-1 and (b) an input signal passes when the control voltage is in logic level 0.

### 2.1.3 MVL TSPCL-based output units

By definition, the True Single-Phase Clock Logic (TSPCL) avoids the clock race problems. The main features of the TSPCL style can be embodied into the voltage-mode MVL circuits, by adding the introduced TSPCL-based output units to the outputs of the MVL circuits. It can noticed that the clock load of the proposed output units remains the same (two transistors are driven from the clock) with the conventional TSPC binary logic [9]. The general structures of the proposed output units with the appropriate voltage supplies, are shown in Fig. 3(a) and 3(b). The former proposed circuit allows a logic value passing to the output node through the transistor $M_1$ or $M_3$ when clock is high (i.e., $k$-1 logic level). Since the p-type enhancement transistor $M_2$ cannot propagate the logic value 0 unchanged, this value must not pass through $M_2$ to the output. Similarly, the n-type enhancement transistor $M_3$ cannot propagate the logic values $k$-1 unchanged and thus, the logic value $k$-1 must not pass through $M_3$ to the output node. When the clock is low (0 Volts), both transistor $M_1$ and $M_3$ are OFF and thus, they isolate the output node. The role of the transistor $M_2$ is to cease the flow of the leakage current from $M_1$ to output node $z$, when the node $z$ is in logic level 0.

The operation of the TSPC-based output unit shown in Fig. 4(b) is similar to the one Fig. 4(a).

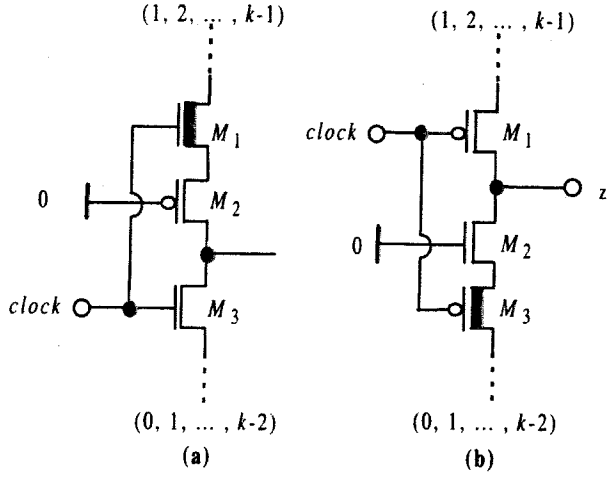
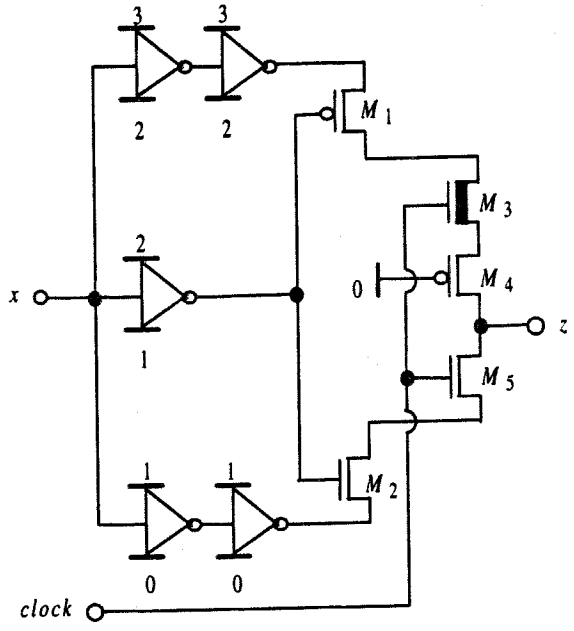



**Figure 3:** TSPCL-based output units when the clock signal is (a) high or (b) low.

### 2.1.4 MVL Latches structure

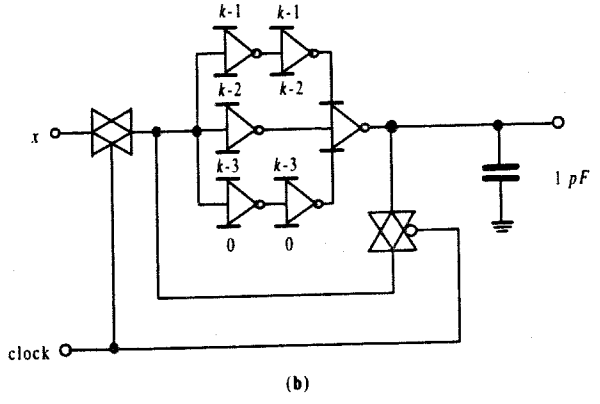
Using the aforementioned building blocks, two kinds of MVL latches can be designed: i) the quaternary dynamic latch and ii) the quaternary pseudo-static latch, as they are shown in Fig. 4(a) and 4(b), respectively. The former latch consists of an inverter-based unit (Fig. 1) and one TSPCL-based output unit (Fig. 3a), while the

latter one consists of an inverter-based unit (Fig. 1) and two uni-signal controlled pass gate (Fig. 2a and 2b). More specifically, a dynamic latch is transparent when the clock is high and it is at the hold mode when the clock is low. Similarly, a pseudo-static latch is transparent when clock signal is high and preserves the last value when clock is low. Simulating with SPICE the pseudo-static latch, the corresponding output waveform is shown in Fig. 5. An output load capacitance of 1 pF (Fig. 4b), which is equal to the fan-in capacitance of three inverters in 0.7 μm technology, is assumed. The resulting worst delay is 3.6 nsec.




(a)

**Figure 4(a):** Quaternary TSPCL-like dynamic latch.




(b)

**Figure 4(b):** Quaternary TSPCL-like pseudo-static latch.

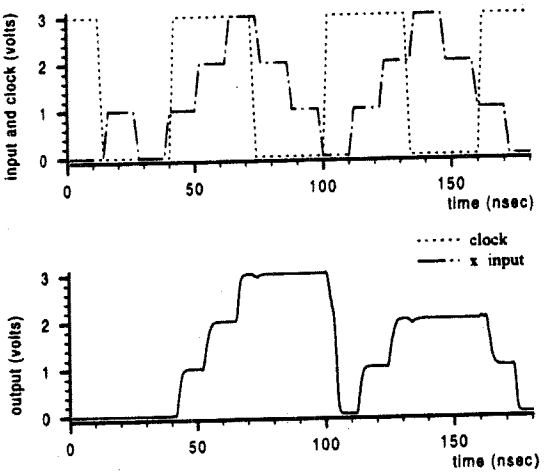



**Figure 5:** SPICE simulation results of the quaternary pseudo-static latch.

## 2.2 QUATERNARY DYNAMIC AND STATIC MASTER-SLAVE STORAGE UNITS

The architecture of the proposed quaternary dynamic master-slave circuit is shown in Fig. 6(a). It consists of two quaternary dynamic latches (total of 30 transistors), the first of which is transparent when the clock is high, while the second one when it is low. Since the proposed structure is TSPCL-based, only one clock is required.

Cascading two pseudo-static latches, a quaternary static master-slave storage unit can be designed. Specifically, the first latch must be transparent when the clock signal is high, while the second one when the clock is low. Substituting the uni-signal controlled pass gate of the output (i.e., feedback loop) of the first latch (i.e., master) and the input pass gate of the second latch (i.e., slave) with TSPCL-based output units, the total of the used transistors is reduced. The circuit design of the introduced master-slave is shown in Fig. 6(b). The function of this circuit is as follows: i) if the clock is high, the first latch is at the evaluation (transparent) mode, while the second one is at the hold mode and ii) if the clock is low, the first latch is at the hold mode, while the second one is at the evaluation (transparent) mode.

Assuming an output load capacitance of 1 pF and using SPICE simulation tools, the derived waveforms of the proposed dynamic and static master-slave circuits are depicted in Fig. 7(a) and 7(b), respectively. Simulation results indicate that the worst delays are 3.2 nsec and 5.5 nsec for the dynamic and static master-slave unit, respectively.

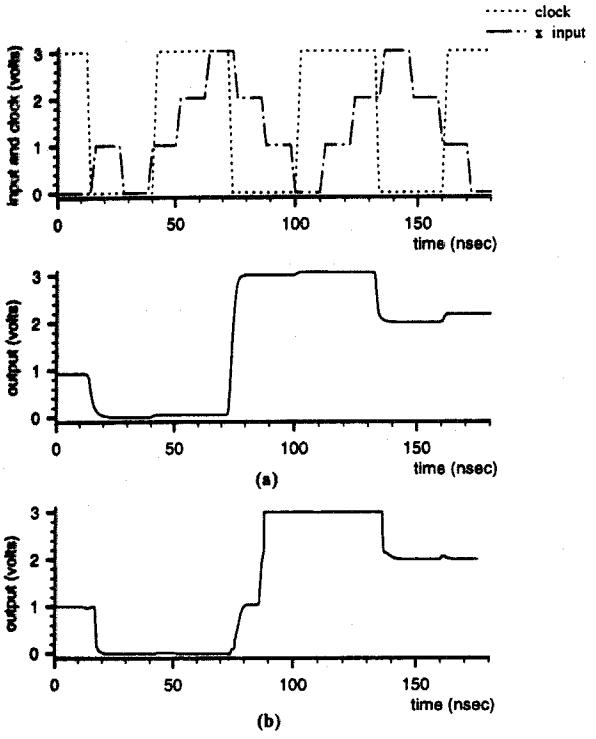



**Figure 7:** SPICE simulation results of (a) the quaternary dynamic master-slave and (b) the quaternary static master-slave storage units of Fig. 6.

## 3. COMPARISON RESULTS

A detailed comparison between the proposed pseudo-static latch and the mixed current-voltage mode quaternary latch reported by Current [11] is shown in Table 3. It is concluded that the proposed latch occupies smaller area (smaller number of transistors), dissipates less power (use of TSPCL and smaller voltage supply) and operates at faster rates.

## REFERENCES


[1] HURST, S. L.: 'Multiple-valued logic - its status and its future', *IEEE Transactions on Computers*, 1984, **C-33** (12), pp. 1160-1179.

[2] ETIEMBLE, D. and ISRAEL, M.: 'Comparison of binary and multivalued ICs according to VLSI criteria', *IEEE Computer Magazine*, April 1988, pp. 28-42.

[3] KAMEYAMA, M.: 'Toward the age of beyond-binary electronics and systems', *20th International Symposium on Multiple Valued Logic*, ISMVL '90, May 1990, Charlotte, NC, pp. 162-166.

[4] HEUNG, A. and MOUFTAH, H.T.: 'Depletion/enhancement CMOS for a low power family of three-valued logic circuits', *IEEE Journal of Solid-State Circuits*, 1985, **SC-20** (2), pp. 609-616.

[5] YASUDA, Y., TOKUDA, Y., TAIMA, S., PAK, K., NAKAMURA, T., and YOSHIDA, A.: 'Realization of quaternary logic circuits by n-channel MOS devices', *IEEE Journal of Solid-State Circuits*, 1986, **SC-21** (1), pp. 162-168.

[6] HUERTAS, J. L., BARRIGA, A., and SANCHEZ-GOMEZ, G.: 'Multivalued dynamic circuits', *Electronics Letters*, 1987, **23** (10), pp. 502-504.

[7] SHANBHAG, N. R., NAGCHOUDHURI, D., SIFERD, R. E., and VISWESWARAN, G. S.: 'Quaternary logic circuits in 2-μm CMOS technology', *IEEE Journal of Solid-State Circuits*, 1990, **25** (3), pp. 790-799.

[8] KRISHNAN, G. and SHIVAPRASAD, A. P.: 'Quaternary multiplexer', *Int. Journal of Electronics*, 1986, **61** (3), pp. 387-396.

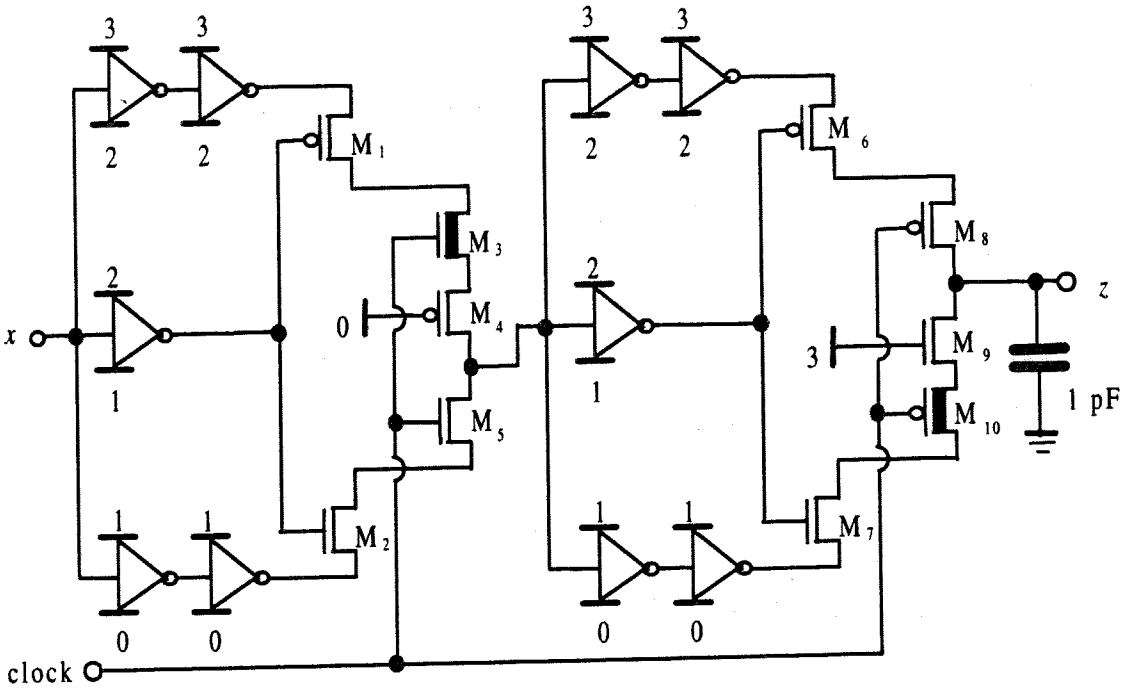
[9] RABEY, J. M.: 'Digital integrated circuits - A design perspective' (Prentice-Hall, New Jersey, 1996) 1st edn.

[10] WATANABE, T., MATSUMOTO, M., and LI T.: 'CMOS four-valued logic circuits using charge-control technique', in Proc. of *18th Inter. Symposium on Multiple Valued Logic*, ISMVL '88, pp. 90-97.

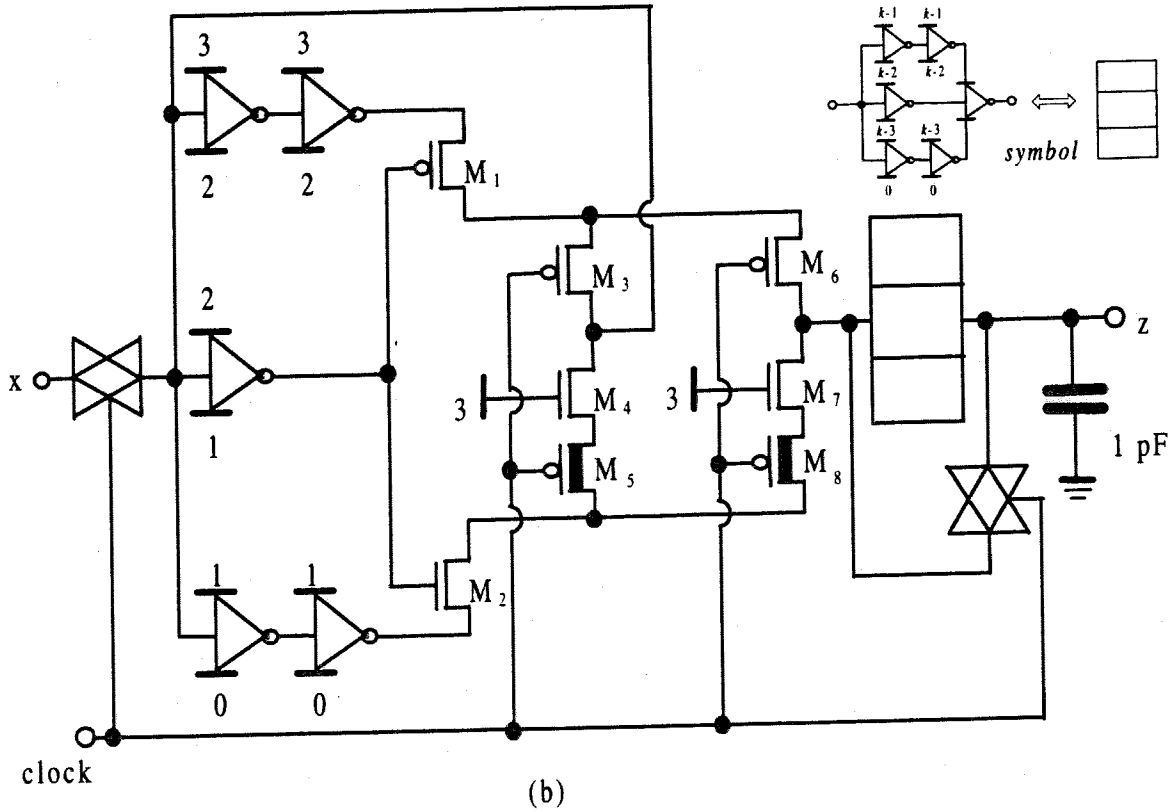
[11] CURRENT, K. W.: 'Multiple-valued logic memory circuit', *International Journal of Electronics*, 1995, **78** (3), 547-555.


| Subject for comparison | Latch [11] | Proposed Latch |
|---|---|---|
| Voltage supply | 5 Volts | 3 Volts |
| Technology | 2 μm | 0.7 μm |
| Number of $V_{TH,0}$ | 1 | 2 |
| Clock pulses used | $\phi$ and $\overline{\phi}$ | only $\phi$ |
| Internal conversion to binary logic | yes | no |
| Transistor count | 73 or 78 | 20 |
| Delay (worst case) | 7 nsec | 3.6 nsec |
| Radix (k) | k = 4 | k ≥ 2 |
| Mode | mixed current-voltage | voltage |
| Static power consumption | yes | no |
| Level correction | - | yes |

**Table 3:** Comparisons between the proposed latch and [11].




(a)




(b)

**Figure 6:** Quaternary (a) dynamic and (b) static master-slave storage units