A New Full Adder Cell for Low-Power Applications

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Abstract — **A new low power CMOS 1–bit full adder cell is presented. It is based on recent design of XOR and XNOR gates [6], and pass-transistors, it has 17 transistors. This cell has been compared to two widely used efficient adder cells; the transmission function full adder cell (16 transistors) [2], and the low power adder cell (14 transistors) [3]. The new cell has no short circuit power and lower dynamic power (than the other adder cells), because of less number and magnitude of circuit capacitances. It consumes 10% to 15% less power than the other two cells. A comparative analysis (using Magic and Hspice) for 8–bit ripple carry and carry select adders shows that the adders based on the new cell can save up to 25% of power consumption.**

I. Introduction

Addition is one of the fundamental arithmetic operations, it is used extensively in many VLSI systems such as microprocessors, and application specific DSP architectures. In addition to its main task, which is adding two numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, ... etc. In most of these systems the adder lies in the critical path that determines the overall speed of the system. That is why enhancing the performance of the 1–bit full adder cell (the building block of the adder) has been of a continuous interest.

Building low power VLSI systems has emerged as a significant performance goal because of the fast growing technology in mobile communication and computation. The advances in battery technology has not taken place as fast as the advances in electronic devices. There is a limited amount of power available for the mobile systems. So the designers are faced with more constraints; high speed, high throughput, small silicon area, and at the same time, consumes as minimal power as possible.

Mainly there are three major components of power consumption in CMOS circuits 1)*Switching Power* due to charging and discharging of the circuit capacitances during transistor switching, 2)*Short Circuit Power* due to short circuit current flowing from power supply to ground when both p-network and n-network are ON, 3) *Leakage Power* due to leakage current. The first component is the dominant one, it accounts for 80–90% of total power consumption in a system [5]. The other two components are not negligible especially the second one since it accounts for about 10–20% of total power consumption in some circuits. The total power is given by the following equation [1]:

$P=\Sigma_i\ V_{dd}.V_{swing}.C_{load}.f.p_i+V_{dd}.\Sigma_i\ I_{i\ sc}+V_{dd}.I_l$

where V_{dd} is the power supply voltage, V_{swing} is the voltage swing of the output which is ideally equal to V_{dd}, C_{load} is the output load capacitance at node i, f is the system clock frequency, p_i is the switching activity at node i, $I_{i\ sc}$ is the short circuit current at node i, and I_l is the leakage current. The summation is over all the nodes of the circuit. Reducing

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any of these components will end up with lower power consumption, although we are always interested in increasing f.

In this paper we present a novel low-power adder cell which is characterized by not having a short circuit power component and having less internal node capacitances than other known standard adder cells. The results are verified by building 8–bit ripple carry and carry select adders based on the proposed adder cell and the other two (commonly used) cells and comparing their power consumption. The rest of this paper is organized as follows, in section II we review standard adder cells known to the literature. In section III we present the new proposed adder cell and analyze its performance. Finally in section IV we build the 8–bit adder cells and compare their performance.

II. Standard Adder Cells

The full adder operation can be stated as follows: given the three 1–bit inputs A, B, and Cin, it is desired to calculate the two 1–bit outputs Sum and Cout, where

$$\text{Sum} = (A \text{ xor } B) \text{ xor } Cin$$
$$\text{Cout} = A \cdot B + Cin \cdot (A \text{ xor } B)$$

The most commonly used adder cells which in current VLSI technology are the conventional CMOS full adder cell shown in Fig. 1(a) (based on CMOS transmission gates and inverters) has 20 transistors [4], and the transmission function full adder cell shown in Fig. 1(b) which is based on the transmission function theory and has 16 transistors [2].

All of the published work show that the transmission function adder (TFA) outperforms the conventional CMOS adder from the power consumption performance point of view. Recently few enhancements were published, one of them is the 14 transistors adder

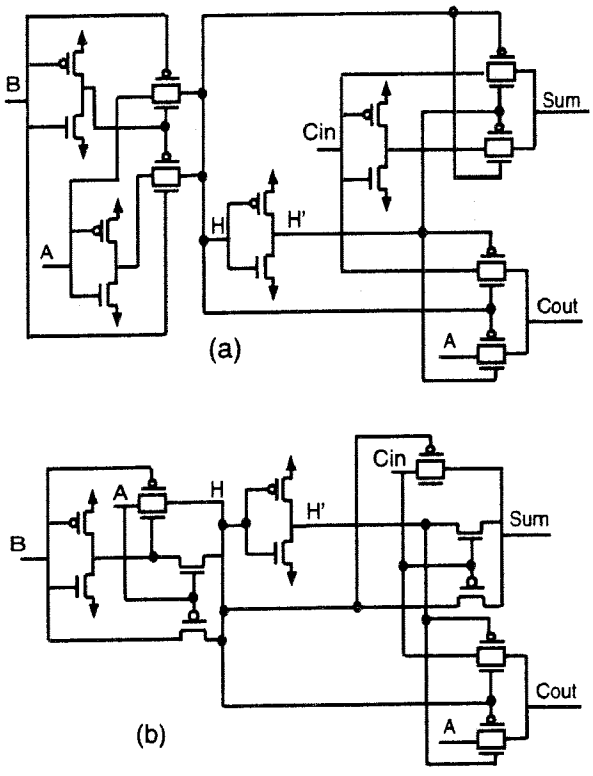

Figure 1 Commonly used full adder cells
(a) The Conventional CMOS full adder.
(b) The Transmission Function full adder

presented in [3] and shown in Fig. 2 which outperforms the other two adders. In this paper we use the transmission function adder (TFA) and the 14 transistors adder (14T) as a reference and we compare them to our new proposed cell.

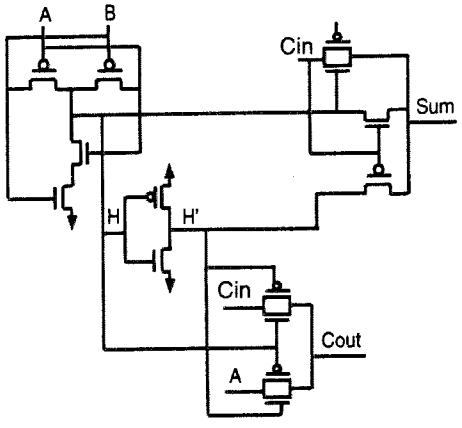

Figure 2 The 14 transistors low power full adder cell.

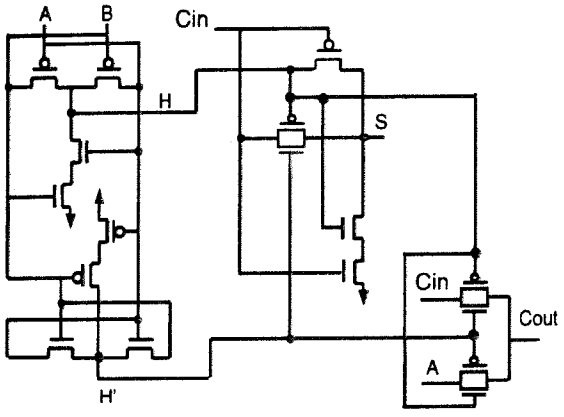

Figure 3 The new 17 transistors adder cell.

III. The New Adder Cell

The new adder cell (NEW) has 17 transistors, and it is based on the low power designs for the XOR and XNOR presented in [6] and on transmission gates and pass-transistors, the cell is shown in Fig. 3. The main reasons which attribute to the low power consumption by NEW (although it has more transistor count than both TFA and 14T) are: first, as we notice from the figure, for any input combination there can never be a direct path from the power supply to the ground, this implies that there is no short circuit current, thus eliminating the short circuit power component which is normally about 10–15% of total power consumption. Second, the SPICE files generated by MAGIC for the new cell has nine capacitances distributed over its inputs, internal nodes and outputs which is equal to the number of capacitances generated for 14T and less than the ten capacitances generated for TFA, although it has 17 transistors, this accounts for having lower power than expected. Third, the cell generates both the XOR and XNOR of inputs A and B (shown as nodes H and H' respectively in all the figures), this is a different style than the other adders which generate the XOR then use an inverter to generate the XNOR. This new style decreases the capacitance at node H since it is not any more loading an inverter, at the same time decreases the capacitance at node H'. The decrease in number (second reason) and magnitude (third reason) of the cell's capacitances account for less dynamic power consumption. A portion of the SPICE files generated for the three cells is shown in Fig. 4. Fourth, the low power designs of the XOR has an incomplete voltage swing for the input pattern (A=0, B=0) while

```
** NODE: 0 = GND!
** NODE: 109 = 6_222_30#
C0 108 0 75F
** NODE: 108 = S
C1 106 0 75F
** NODE: 106 = Cout
C2 107 0 58F
** NODE: 107 = Cin
C3 105 0 12F
** NODE: 105 = 6_74_12#
C4 1 0 11F
** NODE: 1 = Vdd!
** NODE: 103 = 6_124_40#
C5 102 0 37F
** NODE: 102 = B
C6 100 0 72F
** NODE: 100 = H
C7 104 0 49F
** NODE: 104 = H'
C8 101 0 70F
** NODE: 101 = A
```

NEW

```
** NODE: 0 = GND!
C0 108 0 11F
** NODE: 108 = 6_68_79#
C1 107 0 31F
** NODE: 107 = A
C2 106 0 45F
** NODE: 106 = 6_11_107#
C3 1 0 11F
** NODE: 1 = Vdd!
C4 104 0 75F
** NODE: 104 = Cout
C5 105 0 52F
** NODE: 105 = B
C6 103 0 61F
** NODE: 103 = H'
C7 100 0 75F
** NODE: 100 = S
C8 102 0 61F
** NODE: 102 = Cin
C9 101 0 68F
** NODE: 101 = H
```

TFA

```
** NODE: 0 = GND!
C0 107 0 11F
** NODE: 107 = 6_17_107#
C1 1 0 11F
** NODE: 1 = Vdd!
C2 106 0 18F
** NODE: 106 = B
C3 104 0 75F
** NODE: 104 = Cout
C4 105 0 47F
** NODE: 105 = A
C5 103 0 63F
** NODE: 103 = H'
C6 100 0 75F
** NODE: 100 = S
C7 102 0 61F
** NODE: 102 = Cin
C8 101 0 71F
** NODE: 101 = H
```

14T

Figure 4 Capacitance values for the three cells as generated by SPICE.

the XNOR has an incomplete voltage swing for the input pattern (A=1, B=1), by looking carefully at the V_{swing} term in the total power equation we find that it is less than V_{dd} which reduces the dynamic power consumed during these transitions. Finally, the output signals of NEW has less glitches (spurious transitions) than TFA and 14T, as shown in Fig. 5. All these factors account for the low power consumption of the NEW cell.

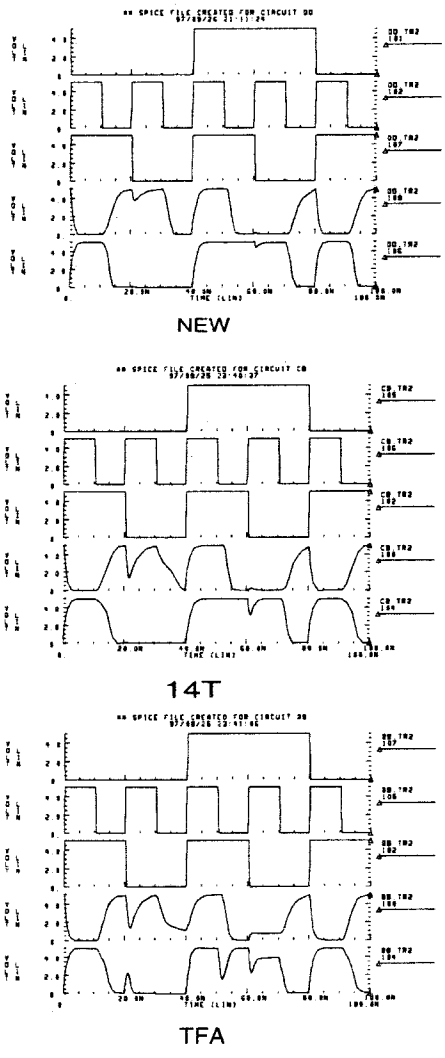

Figure 5 Capacitance values for the three cells as generated by SPICE.

IV. Simulation Results

First we have built the three 1–bit adder cells using minimum sized transistors and their simulation results are shown in Fig. 6. The new cell has 10% less power than 14T and 15% less than TFA. Also from the speed and the power delay product point of views it outperforms the two cells.

	TFA	14T	NEW
Avg. Pw	3.51	3.31	2.98
Delay	4.54	4.97	4.45
Rise time	5.59	5.81	5.64
Fall time	2.56	3.20	1.60
Pw * Delay	15.94	16.46	13.28
Avg. Pw in 10^{-4}Watt, Time in ns			

Figure 6 Simulation results of the three 1–bit adder cells.

Next, we have built 8–bit ripple carry (RC) and 8–bit carry select (CS) adders based on the three cells. The simulation results are shown in Fig. 7. The new cell saves up to 25% of power than TFA, and up to 16% than 14T for ripple carry at different frequencies. While it saves up to 24% of power than TFA, and up to 21% than 14T for carry select.

	TFA	14T	NEW
RC 50 Mhz	2.45	2.17	1.84
RC 40 Mhz	2.08	1.85	1.55
RC 25 Mhz	1.38	1.25	1.06
CS 50 Mhz	4.59	4.20	3.49
CS 40 Mhz	3.82	3.69	2.90
CS 25 Mhz	2.41	2.25	1.91
Avg. Pw in 10^{-3}Watt			

Figure 7 Simulation results of the 8–bit adders.

V. Conclusions

A new low power full adder cell is proposed, it uses the low power designs of the XOR and XNOR functions, transmission gates and pass transistors. It is compared with standard adder cells; the transmission function adder cell [2] and the 14 transistors cell [3]. Although having 17 transistors, simulation results for the 1–bit cells and the 8–bit ripple carry and carry select adders show the superiority of the proposed cell over the other two.

VI. Acknowledgment

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