A Methodology for designing Continuous-time Sigma-Delta Modulators

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Abstract

A methodology for analysis and synthesis of lowpass sigma-delta (ΣΔ) converters is presented in this paper. This method permits to synthesize ΣΔ modulators employing continuous-time filters from discrete-time topologies. The analysis method is based on the discretization of continuous-time model and using a discrete simulator which is more efficient than an analog simulator. Finally, a realistic design of a second-order ΣΔ modulator with a compensation of the non ideal behavior of DAC is given. Moreover, simulation results show a good agreement with the theoretical bases.

I. Introduction

The sigma-delta (ΣΔ) circuits are very attractive analog-to-digital converters because they achieve high accuracy with few critical analog components [1]-[2]. They are composed of a ΣΔ modulator which provides a high speed one bit data string followed by a digital filter and decimator to produce a high resolution data. The lowpass ΣΔ modulator consists of one or more integrator and a one bit quantizer. Nowadays, ΣΔ modulators use integrators built with switched capacitor circuits, which are well suited for VLSI integration. Unfortunately, using a standard technology, the sampling frequency of the modulator is limited by 10 to 50 MHz which results in a signal bandwidth between 50 kHz to a few MHz.

An alternative of discrete-time integrators is the use of continuous-time integrators as it has been used in the first published topologies [3]-[5]. Although continuous-time modulators are not easy to integrate, they possess one key advantage over their discrete-time competitors: the sampling operation is inherently done inside the modulator loop so thqt the restriction of the mentioned maximum sampling frequency is removed. On the other hand, continuous-time circuits are more difficult to design and simulate than discrete-time circuits.

Recently published continuous-time modulators operates between tens of MHz up to a few GHz [6]:[8]. In [6] and [7], the simulations have been done by an analog simulator that takes a considerable computation time. In [8], an equivalent discrete-time model of modulator loop has been described with a continuous filter on the way of input signal. Therefore, we cannot generally use a discrete simulator for these models. Recently, a synthesis method of continuous-time modulators based on the discrete-time ones was described in [8], but the effect of non ideal functionality of the Digital-Analog-Converter (DAC) feedback cannot be systematically studied in order to compensate its effects.

In this paper, an analysis and synthesis of continuous-time modulators based on discrete-time models are presented. In the analysis method, the effect of the removal of sample and hold block and the influence of non ideal functionality of DAC are described. Then based on the equivalent discrete-time model, the compensation of the above mentioned effects can be made.

II. Synthesis Method of ΣΔ Modulators

The behavior of ΣΔ modulators employing discrete-time filters has been widely studied [9]. In this synthesis method, we suppose that a ΣΔ modulator with discrete-time filter has been designed and we would like to transform it to a continuous-time ΣΔ modulator. The continuous-time filters can be resolved by the differential equations [8] & [10]. Nevertheless, it is not well adapted for automatizing the transformation process. In this approach, we use the standard tools available in Maple or Mathematica, such as the Laplace and the *z*-transform.

In throughout of this paper, it is assumed that the input signal *x(t)* is a band-limited signal which respects Shannon theorem, i.e., its bandwidth is less than the half of the sampling frequency. Furthermore, we suppose in this section that the input signal *x* of the modulator is sampled and held and denoted by $x_0(t)$ (Fig. 1).

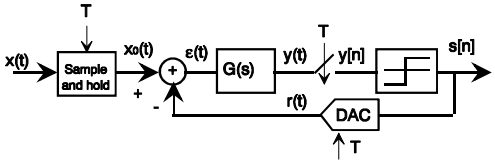

Fig. 1. Continuous time ΣΔ modulator with sampled input signal.

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A. Equivalency between Continuous-time and Discrete-time Filters

The input signals of continuous-time filter $G(s)$ is the sum of the two sampled and held signals $x_0(t)$ and *r(t)*. Now, consider a continuous-time filter $G(s)$ excited by the signal $x_0(t)$ obtained from a sample and hold with sampling frequency $f_s = 1/T$, where f_s denotes the sampling frequency (Fig. 2(a)). The output signal of this filter $y(t)$ is sampled at the same frequency and without any delay, (results $y[n] = y(nT)$). This system can be presented as an equivalent discrete-time system [11] shown in Fig. 2(b), where $F(z)$ denotes the discrete-time transfer function. The relationship between $G(s)$ and $F(z)$ can be expressed as the well-known formula [11]:

$$F(z) = (1 - z^{-1}) Z_T \left\{ L^{-1}\left[G(s)/s \right] \right\}, \qquad (1)$$

where L^{-1} stands for the inverse Laplace transform, Z for the *z*-transform, and $Z_T\{y(t)\} = Z\{y[n]\}$.

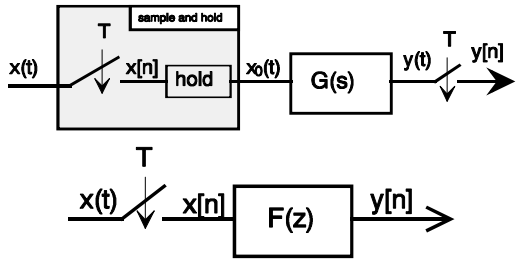

Fig. 2. Block diagram of a continuous filter with a sampled and held input signal and its equivalent discrete-time model.

The results of this transformation for first order and second order integrators are given in Table I. It is important to keep in mind that that if $F(z)$ is the equivalent filter of $G(s)$, then $F^2(z)$ is not the equivalent filter of $G^2(s)$.

Continuous-time filter $G(s)$	**Discrete-time filter** $F(z)$
$\frac{1}{Ts}$	$\frac{z^{-1}}{1-z^{-1}}$
$\left(\frac{1}{Ts}\right)^2$	$\frac{z^{-1}}{1-z^{-1}}\left(\frac{z^{-1}}{1-z^{-1}}+\frac{1}{2}\right)$

Table I. Equivalent discrete-time filter of continuous integrators.

B. Continuous Filter Synthesis

In this section, a method of synthesis of continuous-time filter from a discrete-time one is discussed. It should be noted that there are discrete-time filters for which an equivalent continuous-time filter does not exist.

Let's denote $F'(z) = \frac{F(z)}{1-z^{-1}}$ and $G'(s) = \frac{G(s)}{s}$, Then the Eq. (1) can be rewritten as follows

$$F'(z) = Z_T\left\{ L^{-1}\left[G'(s) \right] \right\}. \qquad (2)$$

After the above assumptions, $F'(z)$ can be decomposed in rational fractions

$$F'(z) = \sum_{k=0}^{N} \frac{\alpha_k}{\left(1 - \beta_k z^{-1}\right)^{\gamma_k}}, \qquad (3)$$

So $G'(s) = \sum_{k=0}^{N} G'_k(s)$ will be a solution of (2) with

$$G_k'(s) = \alpha_k \quad ; \quad \gamma_k = 0, \qquad (4)$$

$$G_k'(s) = \frac{T\alpha_k}{sT - \log(\beta_k)} \quad ; \quad \gamma_k = 1, \qquad (5)$$

$$G_k'(s) = \frac{T\alpha_k\left(sT + 1 - \log(\beta_k)\right)}{\left(sT - \log(\beta_k)\right)^2} \quad ; \quad \gamma_k = 2. \qquad (6)$$

The higher order solutions can be found by using a symbolic calculus software (Maple or Mathematica). Some solutions are given for integrators up to the fourth order in Table II. This table is of course the inverse operation of the Table I.

Equivalency between sampled and continuous filters			
sampled filter $F(z)$	Continuous filter $G(s)$	sampled filter $F(z)$	Continuous filter $G(s)$
1	1	$\frac{z^{-2}}{\left(1-z^{-1}\right)^2}$	$\frac{1}{(Ts)^2} - \frac{1}{2Ts}$
$\frac{z^{-1}}{1-z^{-1}}$	$\frac{1}{Ts}$	$\frac{z^{-1}}{\left(1-z^{-1}\right)^2}$	$\frac{1}{(Ts)^2} + \frac{1}{2Ts}$

Table II. Particular solutions of (1) for integrators.

C. Application to a Second Order ΣΔ Modulator

In this subsection, we want to obtain the equivalent continuous-time ΣΔ modulator of the widely studied second order modulator proposed in Fig. 3. To this purpose, the comparator input *y* must be first decomposed to the sum of the output signal of filters whose inputs are sampled and held. We can then replace each discrete-time integrator by its continuous-time equivalent filter given in Table II. The elements of this modulator can now be recombined to give the usual modulator structure (Fig. 4), which introduces a scaling factor ¾.

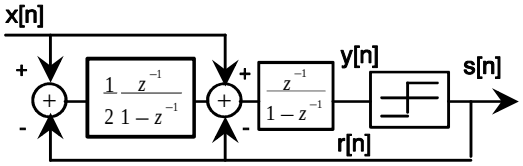

Fig. 3. A second-order discrete-time filter ΣΔ modulator and its transformed representation.

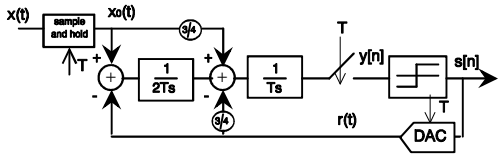

Fig. 4. Equivalent second-order ΣΔ modulator using continuous filters.

Fig. 5(a) gives the Spectral Power Density (SPD) of the output signal of modulator shown in Fig. 3(a) for a low-frequency sinusoidal input signal. Fig. 5(b) shows the SPD of the output of modulator shown in Fig. 4(b) obtained by an analog simulator. Both of the SPD must be theatrically the same. The small differences between both curves are due to the fact that a ΣΔ modulator is a chaotic system, and the analog simulator calculus errors have a considerable effect.

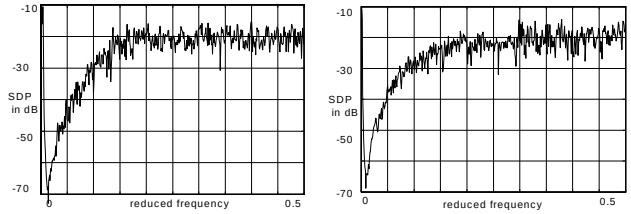

Fig. 5. SPD of output signal S of modulators shown in Fig. 3 and Fig. 4.

III. Realistic Continuous-time Modulators Analysis

In the previous section, an approach of synthesis of ΣΔ modulators employing continuous-time filters was pointed out. The equivalent circuitry of this modulator (Fig. 1(a)) is practically implanted with the following differences:

a) DAC functionality is not ideal,

b) the input sample and hold block is removed.

A time-saving approach for studying this modulator is to use a discrete-time model of the modulator and a discrete-time simulation tool. In contrast to analog circuit simulator, the simulation time can be reduced to a few seconds.

A. Effects of DAC Non Idealities

In practical implementation of the ΣΔ modulator with continuous filter, a realistic DAC circuit is used in the feedback structure. The behavior of a non ideal DAC is illustrated in (Fig. 6). It is assumed that non idealities of DAC can be modelized by a delay and a first degree linear system as shown in (Fig. 7), where $B(s)$ contains the non ideal part of DAC functionality. Consequently, by using well known formula (1), the equivalent discrete-time model of $G(s)$ with non ideal DAC can be expressed as follows:

$$F^*(z) = (1-z^{-1})Z_T\left\{L^{-1}\left[\frac{B(s).G(s)}{s}\right]\right\}. \qquad (7)$$

In what follows, two different modelizations of $B(s)$ are described.

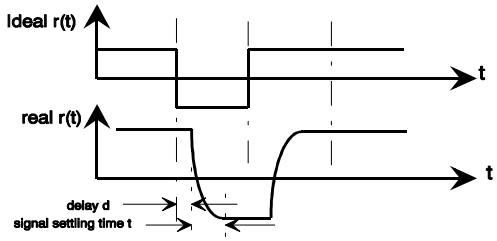

Fig. 6. Functionality of a non-ideal DAC.

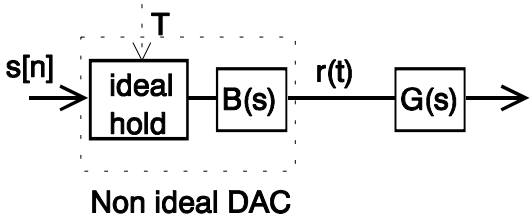

Fig. 7. Modelization of a non ideal DAC.

1) DAC with Linear Dynamics:

If the output stage operational amplifier (op-amp) of DAC circuit works in its linear operation area, the step response of non ideal part of DAC can be approximated by (Fig. 8)

$$r_u(t) = u(t-d)(1-e^{-\frac{t-d}{\tau}}), \qquad (8)$$

where $r_u(t)$ is the output of non ideal DAC.

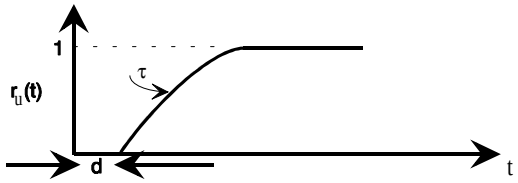

Fig. 8. Output of non ideal DAC for $s[n] = u[n]$.

The delay d can be thought as the result of input and middle stage circuits of DAC, and first degree system as the result of output op-amp stage. The impulse response of $B(s)$ can be derived from (8) and the Laplace transfer

function of $B(s)$ is obtained as $B(s) = \dfrac{e^{-ds}}{(1+\tau s)}$. (9)

For a first-order integrator ($G_1(s) = 1/Ts$), if the rise time or fall time of step response is very smaller than the sampling period, i.e., $\tau << T$ then the equivalent discrete transfer function can be approximated by

$$F_1^*(z) \cong F_1(z) - \delta z^{-1}, \text{ where } \delta = \frac{d+\tau}{T}. \quad (10)$$

Furthermore, it can be shown that for a second-order integrator described by $G_2(s) = 1/(Ts)^2$, the approximated transfer function can be expressed as

$$F_2^*(z) \cong F_2(z) - \frac{\delta}{z-1}. \quad (11)$$

From (10) & (11), it is seen that the non ideality of DAC functionality introduces an approximative additive transfer function which can be considered as a parallel block with the block for which DAC is supposed ideal.

2) DAC with Nonlinear Dynamics:

Here, we suppose that the output stage op-amp of DAC is not sufficiently fast and the slew rate limitation cannot be ignored. A typical step response of DAC is shown in Fig. 9. In the case of a ΣΔ modulator with two levels {1,-1}, the absolute value of input signal is constant and it implies that the delay υ is constant. So the equivalent discrete-time filter will have the following z-transfer function:

$$F_1^*(z) = \frac{z^{-1}}{1-z^{-1}} - \frac{d+\upsilon/2}{T} z^{-1} = F_1(z) - \delta z^{-1}, \quad (12)$$

where δ stands for $\delta = (d+\upsilon/2)/T$.

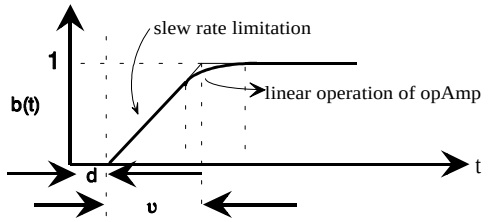

Fig. 9. Step response of B for a current source.

Moreover , for the case of second order integrator, it can be shown that the approximative equivalent filter can be obtained as (11). It should be emphasized that in these formula, δ has the above definition.

B. Effect of Input Sampling

In the synthesis procedure of ΣΔ modulator employing continuous filter, it was pointed that the final schematic of ΣΔ modulator has a sample and hold block on the way of the input signal. In practical implementation, the sample and hold block is removed and input signal is directly applied to the filter $G(s)$.

In practical problem, it is assumed that the module of the frequency response of the corrective term introduced by removing the sample and hold block is comprised between -0.08 and 0 dB which can be practically neglected.

Hence, one can conclude that removing the sample and hold block at the input of the sigma-delta converter has no important influence on the behavior of the modulator as long as the input signal bandwidth is much smaller than the sampling frequency.

C. Simulations of a Second-Order Modulator with Imperfections

In the section II, a second order continuous-time modulator has been synthesized after a discrete-time one (Fig. 4). The equivalent discrete time model of this modulator considering imperfections can be also obtained by using the previous section approach. This model will help to propose a realistic implementation of this modulator with a non-ideal DAC.

The comparator input *y* must be decomposed as the sum of output signal of filters whose input is either the modulator input, or the modulator feedback. We can now replace each continuous-time filter by its realistic discrete-time equivalent which involves the effects of imperfections. Here , the effect of input sample and hold block is ignored. Then all the elements of this modulator can be recombined in order to achieve an appropriate model for the practical implementation (Fig. 10).

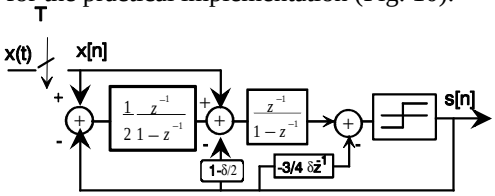

Fig. 10. Normal representation of equivalent modulator with imperfections.

This second order modulator has been simulated with an analog simulator and a discrete-time simulator. The SPD is chosen as a criterion for comparing two models of modulator. The results of simulation for analog and digital model are shown in Fig. 11(a) and Fig. 11(b) respectively . In these simulations, it is assumed that the feedback delay δ is equal to $0.4T$.

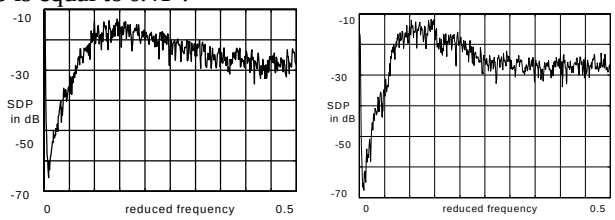

Fig. 11. SPD of output of non-ideal ΣΔ modulator obtained by analog and discrete-time simulator.

From Fig. 11, one can see that the results have a good agreement. The differences between both curves are due to the removal of sample and hold block effect and the chaotic behavior of ΣΔ modulator which intensifies this effect. As long as the calculus errors cumulate, after a few samples, the modulators outputs become different.

D. DAC Non Idealities Compensation

We propose in this subsection a realistic implementation of the modulator shown in Fig. 3 using continuous-time filters and a non-ideal DAC. By using the approach of section III, we have obtained the equivalent discrete-time model of Fig. 4. A compensation for this modulator can be easily made by adding a feedback between the output *s* and the input of 1-bit comparator and changing the coefficient between the output of the DAC and the input of the second integrator. The final realization scheme of the modulator is given in Fig. 12.

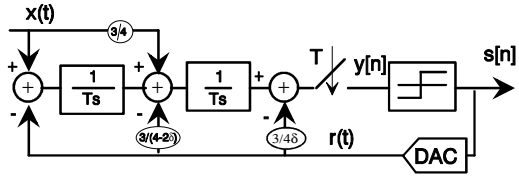

Fig. 12. Block diagram of a continuous filter ΣΔ modulator with feedback errors compensation.

Fig. 13 shows the SDP of the output of this modulator with compensation of non-idealities where the coefficient δ has been exagerately chosen equal to 0.4. This simulation has been done by an analog simulator. This curve can be compared with that of Fig. 5 which is for the ideal modulator. It is seen that the results have a good agreement. Furthermore, one can conclude that the approximations in the discretization procedure are pertinent.

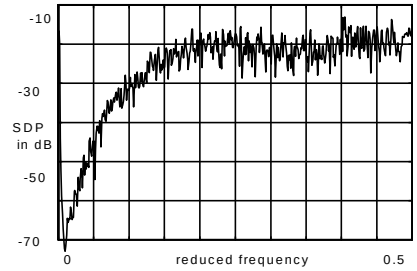

Fig. 13. SDP of output signal S of Fig. 12 compensated modulator.

IV. Conclusions

A novel approach of analysis and synthesis of ΣΔ modulators containing continuous-time filters was described in this paper. It was pointed out that one-bit low-pass modulators employing continuous-filters are equivalent to modulators using discrete-time filters, if their built-in blocks are ideal and the input signal is sampled and held. It was also shown that these models are a good approximation even though the input signal is not sampled and held.

Furthermore some non-idealities such as the feedback DAC delay and rise/fall time can be modelized by an exact discrete-time model. This model permits to simulate a realistic continuous-time modulator by using a discrete-time simulator which is very faster than an analog circuit simulator. This approach can also be used to compensate some of the DAC non-idealities (delay and settling time).

In addition, this approach can be applied to bandpass-modulators topologies. From simulation results, it is felt that the feedback DAC speed is not a restriction for the realization of very fast ΣΔ A/D converters employing continuous-time filters. The sampling frequency over 1 GHz for commercial circuits will be hence reached in the near future.

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