Approaches to On-chip Testing of Mixed Signal Macros in ASICs

Dr. R. A. Cobley,

School of Engineering, University of Exeter, Exeter, EX4 4QF, UK
email: RACobley@exeter.ac.uk

Abstract

This paper initially researches the use of available low-cost analogue CMOS macros to perform simple on-chip tests on the Analogue to Digital Converter macro. The results are evaluated for these tests and then further fuller tests are undertaken. The technique of transient response testing is then applied to three CMOS analogue and mixed submacros to provide more comprehensive test results.

Introduction

An innovative approach to solving problems associated with the testing of mixed ASIC devices has been developed by the author. The frequently mentioned range of problems include: (i) the cost and time of adapting external test equipment to accommodate mixed circuits, (ii) the formulation of tests and generation of the separate signals for the digital / analogue sections, (iii) the lack of a simple functional test for the complete system. Previous investigations by the author [1] have focussed on applying functional mixed signal testing to ASIC devices. The novelty of this approach is the application of on-chip signal generation macros to testing of ADC macros at a simple functional level. More recently this technique has been extended to the generation and evaluation of mixed signal signatures from sub-macros of the ADC macro, notably a switched capacitor integrator macro, using the transient response technique. The major benefit of this is in: (i) avoiding the need for a long test vector development time, (ii) providing a single set of mixed circuit test vectors and (iii) providing faulty chip diagnosis at a functional macro level.

This paper describes the research background to the investigation before concentrating on the evaluation of results from the three main areas: (a) analogue macros for on-chip testing for testing simple ADC macros, (b) full testing of the ADC macro to its specification using on-chip structures, and (c) transient response testing for submacros of the ADC macro. Finally, a brief summary of the work undertaken to date is presented and some further developments outlined.

ED&TC '96
0-89791-821/96 $5.00

Research Background

In recent approaches to testing mixed customised circuits by Fasang [2], Ohletz [3] and Pritchard et al [4], the mixed system is partitioned into digital and analogue sections. These approaches treat the Analogue Section Under Test (ASUT) as the Analogue to Digital Converter (ADC) macro, the Digital to Analogue Converter (DAC) macro and the other analogue macros. The digital section includes scan architecture, so that the test data for the analogue section can be scanned in via scan shift registers and the response monitored and captured on the serial test bus via ADC macros . The converter macros tend to use a larger area of silicon than purely analogue macros. Therefore there is a high probability that most faults will occur in the converters of the ASUT. More importantly detailed fault analysis of the ADC and DAC macros measure their transfer function. This measurement can be used during the final complete ASUT test, to self-calibrate the ADC / DAC macros and formulate the required compensation in the remaining analogue macros.

An alternative approach to mixed system testing by Wagner and Williams [5] involves the use of the internal digital signal processor, to control the synchronisation of tests and analysis of results from the ASUT. Extra on-chip analogue multiplexers, analogue buffers and transmission gates are also required. The system modelling approach adopted by Souders at al [6] requires repeated testing of several devices of the same design to create a functional model for the mixed system. The analysis of the test results reveal a critical number of variables in the system. The required input signature waveform for the system can

then be decomposed into the sum of separate weighted waveforms , which are simpler to generate. As an example a 13 bit ADC device had over 8000 tests applied to 50 different devices. The analysis revealed a set of 18 critical parameters, which related to a final set of only 18 critical tests to evaluate the nonlinearity of the design. The US patent taken out by A.T. & T. [7] describes the technique of using built-in self test circuits to generate a ramp voltage to test the monotonicity of an ADC, whilst a state machine monitors the output. This approach has been adopted for initial ADC macro testing.

An alternative approach by Evans & Shepherd [8] and Taylor et al [9] is to apply transient response analysis to the embedded analogue sections by considering the mixed signal IC as an entity. More recently testing approaches by Binns & Taylor [10] and Arguelles et al [11] have adopted the use of dynamic current testing to detect faults in embedded analogue macros and mixed signal devices. The reference papers cited have demonstrated their testing technique using examples of CMOS and bipolar mixed signal circuits but not those of a switched capacitor nature.

Analogue macros for on-chip testing of mixed ASICs

Initial research into low cost analogue macros considered the devices available. The selected 5 micron CMOS gate array based mixed systems could be fabricated on low-cost devices of approximately 5000 transistors. The analogue macros in the macro library included voltage references, current mirrors, operational amplifiers, voltage and current comparators, oscillators, ADCs and DACs. A selection of the macros were analysed at functional and transistor level. The main performance parameters were identified in each case. The specification of these macros were also studied. Subsequently, example analogue macro test chips enabled a more detailed investigation of the macros and their suitability for on-chip testing. The test results confirmed the operation of the analogue macros within their specification limits.

A gate array device was fabricated containing the CMOS based dual slope ADC macro of 250 gates and approximately 1000 transistors, as shown in Figure 1. Additional on-chip macros were implemented to self-test hte ADC macro. The analogue section of the testing macro had an overhead of 152 transistors. The digital section of the testing macro needed 484 transistors. However the digital test structures could also be used to test further digital areas of a mixed chip.

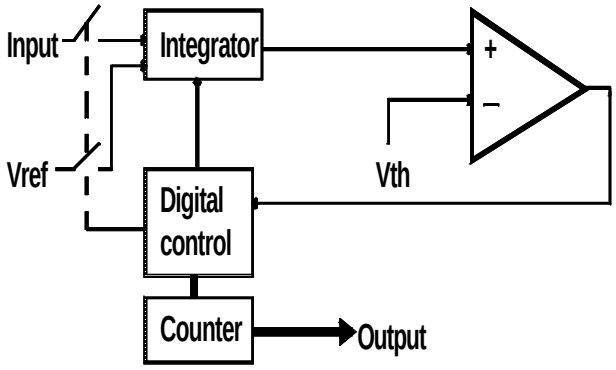

Figure 1. The ADC circuit macro

The ADC macro was partitioned at the functional level. The test signals were then applied at the partitions and the signals at each block measured on-chip where possible. The problem of testing the mixed circuit then becomes one of verifying the operation of the partitioned macros within the system. Three ranges of test were possible using the testing macros added :-

* Step and ramp inputs applied to the analogue sections
* Monitoring of the digital output of the digital sections
* Simple compressed tests of the mixed system

These tests provide a quick check of the ADC operation. Details of the tests are as follows :-

Analogue test results

The step input macro produced voltage steps of 0, 0.59, 0.96, 1.41, 1.8 and 2.5 volts. This gave a measured integrator fall time of 2.6, 2.2, 1.9, 1.2, 0.8, and 0.1 mSec. The ramp signal generator varied from 0 to 2.5 volts over a 1 Sec period, allowing time for 6 measurements at 200mSec intervals. If there was a gain error in the ADC, which was compensated by a gain error in the ramp input, there will be no indication of an error at the output.

Digital test results

The conversion time for the control logic was specified as a maximum of 5.6 mSec. The counter macro was run at 100 kHz clock speed as recommended. The measured time difference in fall time was 10 µSec. This represented 10mv input for each incremented output code change.

Compressed test results

The built-in self test macros were configured to perform a quick functional test of the ADC by compressing the digital output signature from the consecutive application of the DC step input values. The integrator output was also connected to the DC level sensor, which compared the analogue signal to thresholds of 1.9 volts and 3.6 volts. Input to the ADC was then ramped and the maximum integrator voltage signal was compressed into a 2 bit code. This analogue signature gave expected results on all chips.

A batch of 10 devices were fabricated. These comprised the built-in self test macros described and the ADC system. All devices passed the analogue, digital and compressed tests. The results from the quick on-chip tests confirmed the basic operation of the ADC circuit without a catastrophic failure.

Full testing of the ADC macro

The main ADC specification parameters are the quantisation error, zero offset error, gain error, Integral Non Linearity (INL) and Differential Non Linearity (DNL). In the context of the ADC parameters, the operation of the dual slope ADC design was investigated. The switched capacitor integrator section provides a positive or negative ramp depending upon its switch control. In the ADC macro, faults in the comparator submacro will contribute to the offset error and gain error. The integrator submacro faults will affect the linearity errors, the gain error and the offset error. Counter submacro faults will show in the INL or DNL error or as regular missed codes. Faults in the output latch submacro will manifest as multiple incorrect output codes. Finally control circuit faults will stop the conversion process. A full manual test of ADC conversion was also performed. The ADC macro had a specification of: Max Clock rate of 100kHz, Zero offset error < 0.3 Least Significant Bit (LSB), Gain error < 0.5 LSB, INL < 1 LSB , and DNL < 1 LSB. The results from the initial characterisation of the ADC macro gave an overall Gain error of +/- 0.5 LSB,and an Zero offset error of < 0.2 LSB. However there was a maximum INL error value of 1.3 LSB and a maximum DNL error of 1.2 LSB, which is shown in Figure 2.

Transient response testing

The second technique of transient response testing will be described followed by its application to three example circuits and the test results.

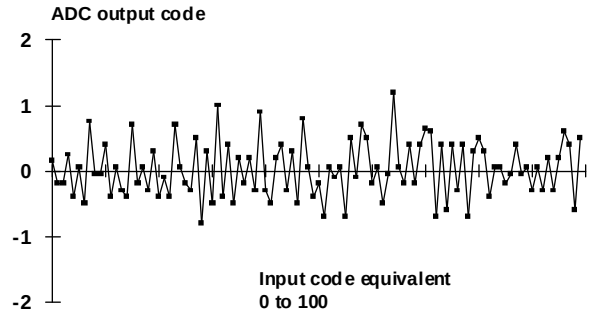

Figure 2. ADC Differential Non Linearity results

Technique details

A transient stimulus vector, propagating in a mixed signal circuit, can be described as the applied stimulus vector, convolved with the impulse response $h_n(t)$ of each circuit block, from which it has propagated. The work by Evans, Al-Qutayri and Shepherd [8], considers the case of an elementary mixed-signal circuit, composed of a single analogue block followed by a digital block. The transient response y(t) of the composite circuit to the applied stimulus vector x(t) will be the convolution of x(t) with the impulse response h(t) of the analogue block and that of the digital block z(t):

$$y(t) = [\ x(t) * h(t) * z(t)\ ]$$

where '*' represents the convolution operator.

In a general mixed-signal device with several external nodes and multiple sections, the response of the system to the stimulus vector set $x_1(t)$ - $x_n(t)$ is the transient signal y(t), which is a logic amplitude signal.

After consideration of the frequency domain for the signal y(t), it can be seen that possible minor changes to the signal spectrum , indicative of circuit faults, can be detected in the presence of the composite noise signal yn(t) by correlating the transient signal y(t) with the specific correlation signal p(t), which was derived from the applied stimulus vector set $x_n(t)$, where n is the number of input signals. This operation produces a correlation function R(y,p) that is identical to the composite impulse response of the IC signal path currently propagating the stimulus vector.

Example circuits

The transient response analysis technique was applied to three example CMOS circuits, which were implemented in 5 micron technology. The first circuit was a CMOS based operational amplifier circuit (OP1) of 13

transistors, which is shown in Figure 3. The input stimulus was a pseudo random binary sequence of 15 bits with a step size of 250µS and amplitude of 0v or 5v. Faults were introduced at the transistor level using voltage generators, which could produce a "stuck-at-0" or "stuck-at-1" fault signal on the three transistor nodes.

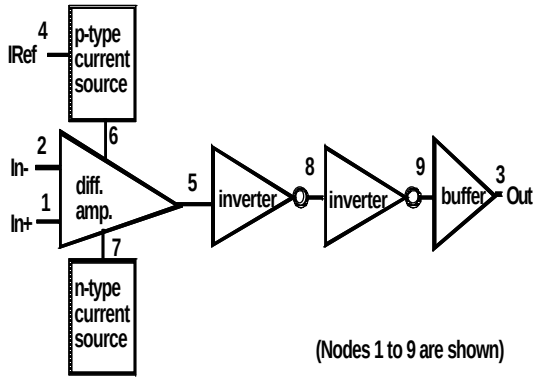

Figure 3. CMOS Operational Amplifier circuit

The HSPICE simulator was used to simulate the transient output vectors for the fault-free circuit. Single separate faults were imposed at the major nodes 4,5,7,8 and 3. Double faults were imposed separately at nodes 8 to 9, nodes 5 to 8 and nodes 4 to 6, which approximated to bridging faults across the MOS transistors. The 16 faulty circuits were then simulated transiently. In a second approach to testing mixed signal circuits, HSPICE was used to determine the poles, zeros and constants for the transfer functions of the fault-free circuit and faulty circuits. Matrices were then created in Matlab to provide a state-space representation of both fault-free and faulty circuits. The impulse response of these circuit representations was determined and compared. The second circuit example of 28 transistors contained a switched capacitor integrator followed by a comparator, which were both modelled using OP1 in Figure 3. The switched capacitor integrator used two non-overlapping clocks with periods of 5µS and the circuit function was simulated for 2mS. In the z domain notation, the integrator was designed for a response:

$$\frac{Vout(z)}{Vin(z)} = H(z) = \frac{z^{-1}}{6.8\ [\ 1 - z^{-1}\ ]}$$

The integrator output signal was compared to a 0.64v reference at the comparator. The impulse response of circuit 2 was compared for separate single "stuck-at" faults at the switched capacitor integrator nodes 4, 5, 7, 8 and 9 and separate bridging faults on nodes 6 to 7 and nodes 5 to 8 of the integrator. A third circuit of the switched capacitor alone, which contained 15 transistors, was also simulated.

Transient response results

The normalised cross-correlation between the input and output signals for the fault-free circuit 1 and for the selected 16 faulty circuits were plotted. The percentage of detection instances of the faulty results are compared in Figure 4.

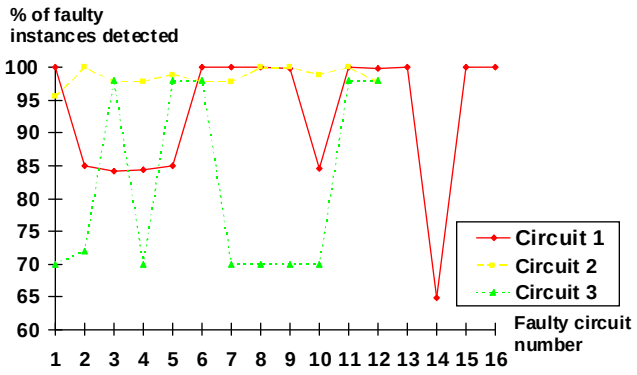

Figure 4. Detection instances for faulty circuits

Under the second testing approach, the impulse responses of the fault-free example circuits 2 and 3 and their 12 faulty circuits were also plotted so that the percentage of detection instances can be derived, as shown also in Figure 4. The 3rd circuit of the switch capacitor integrator shows detection instances of only 70% for some faults. However, all plots show a significant number of time instances when detection is likely during the testing sequence.

Conclusions and Future Developments

The design of simple signal generation and signal measurement macros for an ADC macro have been described. These on-chip testing macros have been applied to an example ADC macro to test the function of its submacros. The technique of transient response testing for analogue and mixed signal submacros has been described, which has been applied to three example analogue CMOS circuits. The results from the technique have been compared using the three example circuits and selected faults. Both techniques revealed sufficient detection instances of the faulty circuits to justify the use of the transient response technique for mixed signal circuit fault detection.

The design of on-chip functional testing macros is under further investigation for larger full-custom ADC devices

designed with sigma-delta modulation architecture, where the switched capacitor integrator forms a major part of the circuit. This work will be complemented by the development of more comprehensive test patterns for fault diagnosis designed to a specific ADC architecture.

Acknowledgements

The work has been supported for device design software by the ESPRIT2 Eurochip Initiative and assisted by M.L. Gambina of Universita Degli Studi di Catania, Sicily. I also acknowledge the comments and suggestions on the work from Dr P Shepherd, Bath University, Dr W Tenten, Robert Bosch GmbHand an anonymous referee of the IEEE.

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