

Hot-Carrier Reliability Enhancement via Input Reordering and Transistor Sizing

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Abstract - *Hot-carrier effects and electromigration are the two important failure mechanisms that significantly impact the long-term reliability of high-density VLSI ICs. In this paper, we present a probabilistic switch-level method for identifying the most susceptible hot-carrier MOSFETs and improving their hot-carrier reliability using two techniques – (i) reordering of inputs to logic gates and (ii) selective MOSFET sizing. We also show that for a given circuit, the best design in terms of hot-carrier reliability does not necessarily coincide with the best design in terms of power consumption.*

1 Introduction

Advances in VLSI fabrication technologies are primarily based on the reduction of device dimensions without a proportional scaling of the power supply voltage. This has resulted in a significant increase in the horizontal and vertical electric fields in the channel region. Electrons and holes gaining high velocities in this electric field get injected into the gate oxide resulting in trapped carriers which degrade the performance of the MOSFET.

Related research at the device level include using high quality oxide and lightly doped drain (LDD) MOSFETs [8]. Redesign techniques targetting hot-carrier reliability have been developed at the circuit level[12], and the logic levels [9]. Finally, reliability analysis tools such as BERT [10] and CREST [11] perform transient analyses to determine hot-carrier degradation of the circuit.

In this paper, we present a fast probabilistic approach to identify MOSFETs in a logic circuit that are most susceptible to hot carrier effects. We account for the hot-carrier effects caused by currents due to charge sharing between the internal nodes of the logic gates[4]. Based on the charging activity, we (i) select an ordering of the inputs to logic gates that improves the hot-carrier lifetime, and (ii) size the appropriate MOSFETs to minimize the hot-carrier susceptibility of the circuits.

2 Switch-Level Model for Hot-Carriers

Hot-carrier injection modifies MOSFET characteristics by degrading transconductance, shifting the threshold voltage, and decreasing drain current capability. In turn, this contributes to the degradation of the overall circuit performance. The hot-carrier lifetime, τ , of a MOSFET k , has been empirically found to be proportional to $\frac{W}{I_k^{avg}}$ [3] where I_k^{avg} is the average drain current and W is the width of the MOSFET. Hence, hot-carrier reliability can be improved either by increasing the width of a MOSFET or by reducing the average drain current which is given by

$$I_k^{avg} = Q_{k,ds}^{avg} \cdot (V_{k,d}^{avg} - V_{k,s}^{avg}) \cdot \mu \quad (1)$$

From Equation 1 computing I_k^{avg} entails computing the average charge ($Q_{k,ds}$) and the average drain and source voltages ($V_{k,d}^{avg}, V_{k,s}^{avg}$) in the MOSFET k (μ is the hole/electron mobility). Towards calculating the average drain current, a switch-level model [2] for a MOSFET is used, and is illustrated in figure 1. Figure 1(b) represents the MOSFETs in figure 1(a) as switches. Also, the nodes corresponding to the source/drain of the MOSFETs are labeled (1)-(6). Each of the switches in figure 1(b) is controlled by an input signal and is assumed to be closed with a given probability. For example, in figure 1(b) the switch corresponding to the p-MOSFET controlled by signal A is closed with a probability $(1-a)$, where a is the probability that the signal A is a logical “1”.

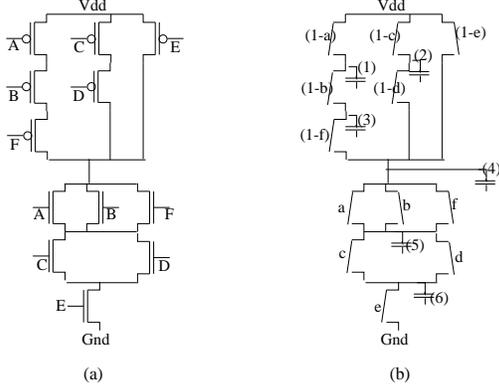


Figure 1: (a) The CMOS gate (b) Representation of the CMOS gate with MOSFETs modeled as switches

We assume that the inputs to the circuit are spatially and temporally independent [5, 6, 9]. With this background, we develop the equations used in estimating the hot-carrier reliability of MOSFETs. For simplicity, the delay of the logic gates is assumed to be zero (zero gate-delay model). This is then extended to a variable gate-delay model.

The zero gate-delay model assumes that the input signals to every logic gate in a combinational circuit arrive simultaneously, Hence the circuit does not have glitches.

2.1.1 Estimation of V_i^{avg}

The derivation of the average voltage, V_i^{avg} of an internal node i of a logic gate is illustrated using an example. The signal probabilities of all primary inputs are known. The signal probabilities of any internal node i , SP_i , can be calculated efficiently using BDDs [7]. Let $P_{V_{dd} \rightarrow i}$ denote sum of the probabilities of all paths from V_{dd} to node i . In figure 1(b), $P_{V_{dd} \rightarrow 1} = SP_1(A' + B'F'C'D' + B'F'E')$. Let $v_i(t)$ be the average voltage at node i at a clock cycle edge at time t , and T be the period of the clock. $v_i(t)$ is dependent on $v_i(t - T)$, the capacitance C_i of the node, and the interaction of node i with its neighbors. The average voltage on the node 1 in figure 1(b) is given by

$$v_1(t) = V_{dd} \cdot [P_{V_{dd} \rightarrow 1}] + v_1(t - T) \cdot SP(AB) + \frac{(v_1(t - T) \cdot C_1 + v_3(t - T) \cdot C_3)}{(C_1 + C_3)} \cdot SP(AB'F) \quad (2)$$

The first term on the right hand side is the fraction of the average voltage when node 5 is electrically connected to V_{dd} . The second term is the fraction of the

average voltage when node 1 is isolated from the remaining nodes in the gate. Finally, the last term accounts for the *charge sharing* [1] between the node 1 and its neighbor 3. Equation 2 can be rewritten as follows.

$$v_1(t) = V_{dd} \cdot [P_{V_{dd} \rightarrow 1}] + \left[\frac{C_3 \cdot SP(AB'F)}{(C_1 + C_3)} \right] \cdot v_3(t - T) + \left[SP(AB) + \frac{C_1 \cdot SP(AB'F)}{(C_1 + C_3)} \right] \cdot v_1(t - T) \quad (3)$$

Let $A_{i,j}$ be the coefficient of $v_j(t - T)$ in the equation to calculate $v_i(t)$. For example, in equation 3, $A_{1,3} = \frac{C_3 \cdot SP(AB'F)}{(C_1 + C_3)}$. $A_{i,j}$'s depend on the node capacitances and the signal probability of some function of the inputs. For any node i in a logic gate, the general expression for $v_i(t)$ can be compactly expressed as $[v(t)] = V_{dd} \cdot [P] + [A] \cdot [v(t - T)]$.

Hence, substituting $v_i(t)$ and $v_i(t - T)$ with V_i^{avg} as $t \rightarrow \infty$, $v_i(t) = v_i(t - T) = V_i^{avg}$, V^{avg} can be expressed as

$$[V^{avg}] = [I - A]^{-1} \cdot V_{dd} \cdot [P] \quad (4)$$

2.1.2 Estimation of $Q_{k,ds}^{avg}$

Let the average charge transferred from the drain to the source of MOSFET k be given by $Q_{k,ds}^{avg}$. Then $Q_{k,ds}^{avg} = \sum_{\forall j} P_j \cdot q_{j,k}$, where P_j is the probability that some set j of MOSFETs are ON and $q_{j,k}$ is the charge that is transferred through MOSFET k due to charge sharing between nodes that are connected when the MOSFETs in set j are ON. The expression for $Q_{k,ds}^{avg}$, is a weighted sum of the charge transferred through MOSFET k due to charge sharing. The weights, P_j , are calculated using the signal probabilities of the inputs to the logic gate. $Q_{k,ds}^{avg}$ and V_i^{avg} can now be used to calculate the average current I_k^{avg} in MOSFET k . For example, the charge flowing through the PMOSFET k connecting nodes 1 and 2 as shown in figure 2, is given by

$$Q_{k,12}^{avg}(k) = P_{a=1,b=0} \cdot V_1^{avg} \cdot C_1 + P_{a=0,b=0} \cdot (V_{dd} - V_2^{avg}) \cdot C_2 \quad (5)$$

Hot-carrier reliability can thus be estimated. The estimation of power is however very different from the estimation of hot-carrier reliability. The average power dissipated in node i will be given by the product of V_{dd} , the frequency and the average charge drawn from V_{dd} by node i , and is given by the expression 6.

$$V_{dd} \cdot \left(\frac{1}{T} \right) \cdot \sum_{\forall i \in nodes} P_{V_{dd} \rightarrow i} \cdot C_i \cdot (V_{dd} - V_i^{avg}) \quad (6)$$

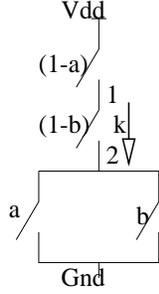


Figure 2: Switch level model of a NOR gate.

2.2 Variable Gate-Delay Model

We now consider the scenario wherein every gate in a circuit has a non-zero finite delay. This results in unequal path delays along the different paths from the primary inputs to the output node of a gate causing glitching activity at the node. These glitches, draw extra current from V_{dd} thereby contributing to the hot-carrier induced damage in the circuit.

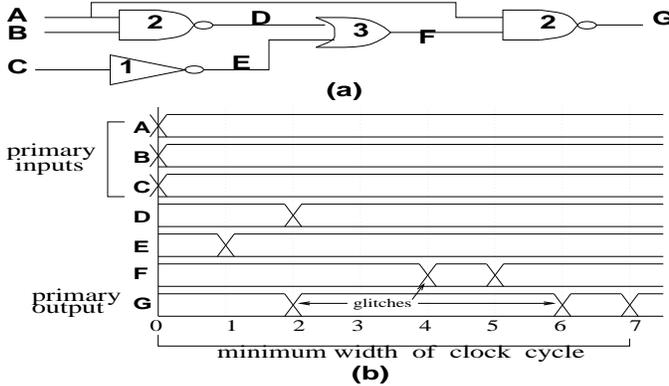


Figure 3: (a) A combinational circuit with delays marked on gates. (b) Possible time units when voltages could change in the circuit.

Consider the circuit shown in figure 3(a), with three logic gates with gate delays. Let primary inputs A , B and C arrive at time $t = 0$ as shown in figure 3(b). The node F changes three time units after inputs D and E change. Since D and E do not both change simultaneously, F could glitch at $t = 4$ before it settles to its stable value at $t = 5$. There should be a delay of atleast 7 time units between successive sets of primary inputs to stabilize the circuit output. A glitch can occur only at an integral number of time units(1 to 6) within a clock cycle.

Due to glitches, current can be transferred through a MOSFET even within a clock cycle. Consequently, the

average charge transferred through a MOSFET k at every time unit t , $Q_{k,ds}^{avg}(t)$, during a clock cycle should be determined. To calculate $Q_{k,ds}^{avg}(t)$, we require the values for $V_i^{avg}(t)$, the estimated voltage at an internal node i during a time unit t .

2.2.1 Estimation of $V_i^{avg}(t)$ and $Q_{k,ds}^{avg}(t)$

The values of $V_i^{avg}(t)$ and $Q_{k,ds}^{avg}(t)$ depend on the values of $V_i^{avg}(t-1)$ and the probability that V_{dd} is connected to an internal node t at t time units (note that a time unit is a division of the clock cycle where a glitch could occur). Such probabilities of the internal nodes at any time unit within a clock cycle is calculated using symbolic simulation described in [5, 6]. A variable gate-delay model differs from a zero gate-delay model in that, a node in the circuit may have several signal probability values depending on the time unit, t , for which the value is calculated.

Returning the figure 1, let the probability of a path from V_{dd} to node 1 at time unit t in a clock cycle be denoted by $P_{V_{dd} \rightarrow 1}(t)$. This is the signal probability value at time unit t denoted by $SP(t, (A' + B'F'C'D' + B'F'E'))$. Using the same principles that were used to derive equation 2, we express $V_i^{avg}(t)$, the average voltage in node i at time unit t , in equation 7.

$$V_1^{avg}(t) = V_{dd} \cdot [P_{V_{dd} \rightarrow 1}(t)] + \left[\frac{C_3 \cdot SP(t, AB'F)}{(C_1 + C_3)} \right] \cdot V_3^{avg}(t-1) + \left[SP(t, AB) + \frac{C_1 \cdot SP(t, AB'F)}{(C_1 + C_3)} \right] \cdot V_1^{avg}(t-1) \quad (7)$$

The coefficients of $V_i^{avg}(t-1)$ depend on the capacitances of the nodes and the signal probabilities of the inputs at time unit t . These coefficients are $P(t)$ and $A(t)$ in equation 8. Equation 8 represents the average voltage of the nodes in the circuit at time unit t .

$$[V^{avg}(t)] = V_{dd} \cdot [P(t)] + [A(t)] \cdot [V^{avg}(t-1)] \quad (8)$$

We now describe how the values of $V_i^{avg}(0)$, the average voltage of a node i at a clock edge (at 0 time units), can be calculated. The stable value of the voltage of a node would occur at a clock edge, regardless of whether a zero or variable gate-delay model is used. As a result, $V_i^{avg}(0)$ of a node in a variable gate-delay model has the same value as V_i^{avg} in the zero gate-delay model. Using the value of $V_i^{avg}(i)$ (from the zero gate-delay model), we estimate the value of $V_i^{avg}(1)$ using equation 8. We then repeatedly use equation 8, to derive the values of

$V_i^{avg}(2), V_i^{avg}(3) \dots V_i^{avg}(T-1)$. Note that, $V_i^{avg}(T)$ will be equal to $V_i^{avg}(0)$.

The average charge transferred from the drain to the source of a MOSFET k at time unit t , $Q_k^{avg}(t)$, is given by equation 9.

$$Q_{k,ds}^{avg}(t) = \sum_{\forall j} P_j(t) \cdot q_{j,k}(t) \quad (9)$$

In equation 9, $P_j(t)$ is the probability that a set j of MOSFETs are ON at time unit t . Similarly, $q_{j,k}(t)$ is the charge transferred through MOSFET k when the set j of MOSFETs are ON at time unit t .

2.2.2 Estimation of Hot-Carrier Reliability

Following the ideas used to derive $Q_{k,ds}^{avg}(t)$, the average current through a MOSFET k at time unit t denoted by $I_k^{avg}(t)$, is calculated using equation 10.

$$I_k^{avg}(t) = Q_{k,ds}^{avg}(t) \cdot (V_{k,d}^{avg}(t) - V_{k,s}^{avg}(t)) \cdot \mu \quad (10)$$

The net average current through a MOSFET k , in a clock cycle, given by I_k^{avg} , can be obtained by summing $I_k^{avg}(t)$ over all time units t in a clock cycle. This is expressed in equation 11.

$$I_k^{avg} = \sum_{t=0}^{T-1} I_k^{avg}(t) \quad (11)$$

Similarly, equation 12 can be used to arrive at the total power dissipated in a CMOS gate subject to a finite delay. Equation 12 is derived from equation 6 after modifying it to account for the power dissipated at every time unit in a clock cycle.

$$V_{dd} \cdot \left(\frac{1}{T}\right) \cdot \left[\sum_{t=0}^{T-1} \sum_{\forall i \in nodes} P_{V_{dd} \rightarrow i}(t) \cdot C_i \cdot (V_{dd} - V_i^{avg}(t)) \right] \quad (12)$$

As in the case of zero gate-delay, $V_i^{avg}(t)$ is not independent of $P_{V_{dd} \rightarrow i}(t)$, but are related by equation 8.

3 Input Reordering for Hot-Carriers

We now propose an algorithm for gate-input reordering at the switch level to improve hot-carrier reliability. For a gate, there are usually a few *functionally equivalent gate-input* orderings. For example, in figure 1(a), the two sets of primary inputs {A, B and F} and {C and D} could be reordered within themselves without affecting the functionality of the gate. Maximizing hot-carrier reliability entails arriving at the gate-input order that minimizes the maximum drain current I_i^{avg} (equation 1)

1. Calculate $SP_i, \forall nodes i$ (using BDDs[7]).
2. Calculate $P_{V_{dd} \rightarrow i}, \forall internal nodes i$, in all gates
3. Determine $V_i^{avg} \forall nodes i$
4. For every gate j in the circuit
 - Begin**
 - For each functionally equivalent gate-input order, O_g
 - begin**
 - If objective is hot-carrier reliability
 - Determine $\max I_i^{avg}$ among the MOSFET $i \forall O_g$
 - Select the O_g , for which $\max I_i^{avg}$ is minimum
 - Reconnect inputs of gate j to the gate-input order O_g .
 - If objective is Power dissipated
 - Determine the power dissipation $\forall O_g$
 - Select the O_g , for which power dissipation is minimum
 - Reconnect inputs of gate j to the gate-input order O_g .
 - end**
 - End**

Figure 4: The gate-input reordering algorithm

among all MOSFETs i in the circuit. An outline of the algorithm used is shown in the figure 4.

The input to the algorithm is a technology-mapped circuit after logic synthesis. We merely enforce an ordering of the gate-inputs to maximize hot-carrier reliability without affecting any of the metrics during synthesis. Note that the number of functionally equivalent gate orders for a gate with n inputs, is upper bounded by $n!$ (in the case of n -input NAND or NOR gate) but is usually much less. For example, for the complex gate with 6 inputs in figure 1(a), there are $6 \cdot 2 = 12$ functionally equivalent gate-input orders. Since the average number of functionally equivalent gate-input orders for a gate does not depend on the number of gates in the circuit, the complexity of the proposed algorithm is proportional only to the number of gates in the circuit.

4 Results

Results of the proposed algorithms on MCNC91 combinational benchmark examples for hot-carrier reliability are shown Tables 1 - 3. The signal probability of the inputs was assumed to be 0.5.

The circuits were synthesized for minimum delay and then mapped using cells from the standard cell library. The capacitance of an internal node i of a logic gate is approximated by $C_{(i)} = C_{diff(i)} + C_{jsw(i)} \cdot l_i + C_{j(i)} \cdot A_i$ where $C_{diff(i)}$ is the capacitance of the source/drain diffusion provided in the file extracted from the MAGIC layout of the gate. $C_{jsw(i)}$ and C_j , the junction-bulk sidewall capacitance and the junction-bulk capacitance,

respectively. The values of $C_{jsw(i)}$ and C_j obtained from the technology file (model file). l_i and A_i are obtained from the layout of the gate and are the perimeter and area of the source/drain regions, respectively.

circuit	H Carrier		Power		% imprvt.	
	τ ($10^8 s$)	Pow. (μW)	τ ($10^8 s$)	Pow. (μW)	in τ	in Pow
C17	0.70	2.9	0.29	2.4	144.76	22.92
9symm	0.66	477.4	0.66	369.0	0.00	29.36
b1	0.43	17.9	0.39	14.9	10.26	19.87
b9	0.16	415.9	0.14	384.5	14.29	8.17
c8	0.10	566.8	0.09	522.9	11.11	8.38
cc	0.83	105.9	0.20	84.6	315.00	25.14
cht	0.23	651.0	0.21	611.8	9.52	6.41
cm138	0.18	45.4	0.16	44.1	12.50	3.04
cm150	0.29	384.5	0.27	339.0	7.41	13.42
cm151	0.88	194.9	0.80	181.5	10.00	7.38
cm162	0.56	240.3	0.10	205.5	460.00	16.90
cm163	0.19	78.2	0.16	66.6	18.75	17.40
cm42	0.22	92.3	0.19	91.3	15.79	1.07
cm82	0.21	89.7	0.17	77.7	23.53	15.39
cm85	0.57	282.9	0.55	244.8	3.64	15.58
cmb	0.23	124.4	0.23	108.2	0.00	14.97
cordic	0.07	387.3	0.06	340.2	16.67	13.84
count	0.35	689.6	0.33	484.1	6.06	42.46
frg1	0.45	540.8	0.04	455.6	971.43	18.70
Aver.	0.39	283.6	0.26	243.6	108.00	16.0
SD.	0.06	50.2	0.05	42.5	54.10	2.19

Table 1: Hot-carrier lifetime and Power values for circuits optimized for hot-carrier reliability and power.

The results of hot-carrier lifetime (τ) and power dissipation for circuits assuming a variable gate-delays is shown in table 1. Hot-carrier lifetime of a circuit, τ , is defined as the time required to accumulate $0.05 \cdot 10^{12}/cm^2$ trapped carriers in any MOSFET in the circuit. In columns 2 and 4, the lifetime values, τ , of the circuit is shown for circuits synthesized for hot-carrier reliability and minimum power dissipation. Similarly, in columns 3 and 5, the power dissipated in circuits synthesized for hot-carrier reliability and minimum power dissipation are shown. An average lifetime improvement of 108% and an average improvement of 16% in the power dissipated was found, between the hot-carrier optimized and power optimized designs.

We now present results in table 2 showing how the % increase in delay is affected by hot-carrier induced damage to the MOSFETs in a circuit. The delay of the gates in a circuit are obtained from the standard cell

circuit	50 Coulombs		300 Coulombs	
	time ($10^8 s$)	% increase in delay	time ($10^8 s$)	% increase in delay
C17	0.20	8.30	1.20	13.1
9symm	0.75	7.86	4.53	34.2
b1	0.25	10.20	1.52	16.6
b9	1.01	1.68	6.09	3.9
c8	15.09	4.27	90.54	13.8
cc	0.76	3.70	4.53	6.9
cht	0.42	7.20	2.55	36.4
cm138	0.79	18.10	4.75	30.9
cm150	0.25	83.20	1.52	171.9
cm151	0.25	32.90	1.51	58.0
cm162	4.82	6.07	28.95	11.4
cm163	3.00	4.40	18.02	7.8
cm42	0.79	9.70	4.75	15.6
cm82	0.25	3.53	1.52	6.2
cm85	2.74	43.73	16.44	78.8
cmb	1.40	47.92	8.43	86.0
cordic	3.84	142.11	23.06	312.1
count	0.49	2.16	2.92	5.1
frg1	0.66	2.15	4.00	5.1
Aver.	1.99	23.1	11.93	48.1
SD.	0.77	7.99	4.616	17.0

Table 2: Hot-carrier lifetime and the percentage increase in delay for two different amounts of charge that flows through any MOSFET in the circuit.

library. The delay-package in SIS was used to estimate the delay of the circuits. The delay of the circuits is affected by the decrease in drive current capability of the MOSFETs as a result of the hot-carrier induced damage to the oxide caused by trapped charge. We calculate the operation time and the % increase in delay of the circuits caused due to three different maximum amounts of trapped charge in the oxide of the MOSFETs, for a clock cycle of $400ns$. The second and the third columns stand for the operation time required and the resultant % increase in delay when a maximum of 50 coulombs of charge passes through any MOSFET. Similarly, fourth and fifth columns represent the operation time and % increase in delay values when a maximum of 300 coulombs of charge flows through any MOSFET. The % increase in delay is derived from the experimental results shown in [8] relating drain current degradation (from which delay degradation is derived) and the total charge that flows through the MOSFET (from which the operation time can be derived). When a maximum of 300 coulombs of charge

circuit	Impact of MOSFET Sizing			
	1 MOSFET		4 MOSFETs	
	$\frac{W_{new}}{W_{old}}$	% increase in τ	$\frac{W_{new}}{W_{old}}$	% increase in τ
C17	1.28	22.4	1.83	45.5
9symm	1.05	0.0	1.35	26.3
b1	1.10	9.7	1.91	47.4
b9	1.23	18.8	1.47	32.0
c8	1.13	12.2	1.52	34.6
cc	1.33	25.2	1.41	29.1
cht	1.10	9.6	1.31	11.6
cm138	3.37	70.3	10.93	90.8
cm150	1.07	7.1	2.96	66.2
cm151	1.44	30.9	1.62	37.7
cm162	1.18	15.9	1.37	27.0
cm163	1.21	17.8	1.61	38.0
cm42	1.23	18.7	2.45	59.2
cm82	1.67	40.3	2.47	59.1
cm85	1.00	0.0	3.67	72.8
cmb	1.21	17.8	1.35	25.9
cordic	1.51	33.9	1.89	24.1
count	1.06	6.0	1.31	24.1
frg1	1.05	5.0	1.40	28.6
Aver.	1.33	19.0	2.31	41.1
S.D.	0.12	3.7	0.49	4.5

Table 3: Impact of sizing of the most susceptible MOSFETs on circuit lifetimes, when a variable gate-delay model is used.

has been transferred through any MOSFET, the average increase in delay of the entire circuit was estimated to be as high as 48%.

In table 3, we show the impact on the hot-carrier lifetime by resizing the most susceptible MOSFETs. Very few MOSFETs have to be sized to increase the lifetime of the most susceptible MOSFETs. For example, an average increase in *MTF* of 41% can be obtained by sizing only 4 MOSFETs. This approach will not affect the performance if the sized MOSFETs do not belong to a gate on the critical path.

5 Conclusions

We present an algorithm for *probabilistic switch-level estimation of MOSFETs susceptible to hot-carrier effects* in a technology-mapped circuit. This method considers the hot-carrier degradation in the MOSFETs due to switching activity at the output of the logic gates and the charge sharing between the internal nodes within logic gates. *The inputs to the logic gates are then ordered to maximize hot-carrier reliability.* Results on

benchmarks indicate that an average of 108% improvement in *MTF* and 16.0% improvement in power dissipated can be obtained by suitably ordering the inputs to logic gates. *MOSFET resizing* experiments demonstrate that by sizing very few MOSFETs significantly decrease in hot-carrier susceptibility (up to 41.1% for 4 MOSFETs). *The results also indicate that a design optimized for hot-carrier reliability is not necessarily the best design in terms of power.*

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