Synthesis Tools for Mixed-Signal ICs: Progress on Frontend and Backend Strategies

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Abstract

Digital synthesis tools such as logic synthesis and semicustom layout have dramatically changed both the *frontend* (specification to netlist) and *backend* (netlist to mask) steps of the digital IC design process. In this tutorial, we look at the last decade's worth of progress on analog circuit synthesis and layout tools. We focus on the frontend and backend of analog and mixed-signal IC design flows. The tutorial summarizes the problems for which viable solutions are emerging, and those which are still unsolved.

1 Introduction

The microelectronics market and in particular the markets for ASICs, ASSPs and high-volume commodity ICs are characterized by an ever increasing level of integration complexity. In recent years, complete systems that before occupied one or more boards are increasingly being integrated on a few chips or even one single chip. Examples of such "systems on a chip" are the single-chip TV or the single-chip camera, as presented at the 1996 International Solid-State Circuits Conference. Although most functions in such integrated systems are implemented with digital or DSP circuitry, the analog circuits needed at the interface between the electronic system and the "real" world are also being integrated on the same die for reasons of cost and performance. The booming market share of mixed-signal ASICs in modern electronic systems for telecom, consumer, computing, and automotive applications is a direct result of this. Since the early 1990s, the average growth rate of the mixed-signal IC market has been between 15 and 20% per year.

Together with this increase in circuit complexity, also the design complexity has increased drastically. At the same time, many present ASIC application markets are characterized by shortening product life cycles and time-to-market constraints. These constraints can only be met by using advanced computer-aided design (CAD) tools. In the digital world, logic synthesis and semi-custom layout have emerged as the *de facto* strategies for managing the *frontend* (specification to gate-level netlist steps) and the *backend* (netlist to mask steps) of the design process. Unfortunately, we do not (yet) have robust circuit synthesis and layout tools in the analog domain. The design cycle for analog and mixed-signal ICs remains long and error-prone.

This tutorial attempts to address this lack of mature, commercial analog CAD tools. Our central purpose is to suggest that the news is *not* all bad here: the circuits research community has been working aggressively for over a decade to solve the difficult design problems posed by analog and mixed-signal ICs. Given the success of synthesis and semi-custom layout in digital designs, we focus our tutorial also on tools to support the *frontend* and *backend* of the analog design process, *i.e.*, custom circuit synthesis and layout. Given space limitations, this necessarily means that our review of relevant efforts in each area is brief and some interesting work is omitted. Two omissions we note specifically. We do not treat any analog hardware description behavioral modeling languages. The topic is extremely important and is likely to have a substantial impact on how analog synthesis moves forward, but as of this writing the dust has not yet settled on any of the proposed standards. And, we do not cover analog and mixed-signal simulation strategies. These are much more mature than the comparable synthesis and layout tools, and there are numerous commercial offerings. With those caveats, this tutorial strives to give an overview of the state-of-the-art in the field of analog circuit and layout synthesis, where we are today, and where we are going tomorrow.

2 Frontend Solutions: Analog Synthesis

In this section we present the hierarchical design methodology used in most analog CAD systems today, followed by a survey of the different approaches undertaken towards analog circuit synthesis. This frontend synthesis consists of two steps: topology selection and circuit sizing.

2.1 Hierarchical Design Methodology

For the design of a complex analog macroblock like a phase-locked loop or an analog-to-digital converter, the analog block is typically decomposed into smaller subblocks (e.g. a comparator or a filter), each of which is then designed separately. In such a hierarchical scheme, most experimental analog CAD systems presented today use a performance-driven design strategy, that consists of the alternation of the following steps in between two levels of the design hierarchy [1,2,3]:

- **Top-down path:**
  - topology selection
  - specification translation (circuit sizing)
  - design verification
- **Bottom-up path:**
  - layout generation
  - detailed design verification (after extraction)

Throughout the design constraints have to be passed down the hierarchy in order to make sure that the top-level block at the end meets its specifications. Redesign iterations are needed when the design fails to meet the specifications at some point in the design

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flow.

In this design process topology selection is the step of selecting the most appropriate circuit topology out of a set of alternatives, that can best meet the given specifications. A topology can be defined hierarchically in terms of lower-level subblocks. For an analog-to-digital converter for instance, this could be selecting between a flash, a successive approximation, a Delta-Sigma or any other topology. Specification translation is then the step of mapping the specifications for the block under design at a given level (e.g. converter) into individual specifications for each of the subblocks (e.g. comparator) within the selected block topology, so that the complete block meets its specifications, while possibly also optimizing the design towards some application-specific design objectives (e.g. minimal power consumption). The translated specifications can then be verified by means of (behavioral or circuit) simulations. At the lowest level in the design hierarchy, the subblocks are single devices and specification translation reduces to circuit sizing (or dimensioning), which is the determination of all bias parameters, element values and device sizes in the circuit tuned to each specific application.

2.2 Approaches Towards Analog Circuit Synthesis

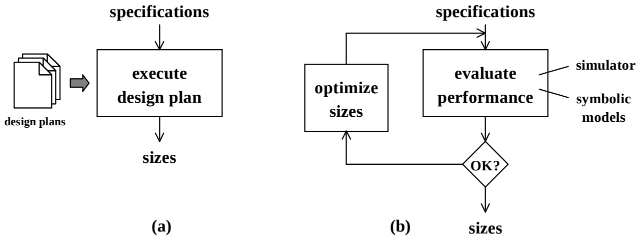
Circuit synthesis is the inverse operation of circuit analysis, where the subblock parameters (such as device sizes and bias values) are given and the resulting performance of the overall block is calculated, as is done in SPICE. During synthesis, the block performance is specified and values for the subblock parameters needed to meet these specifications have to be determined. This inverse process is not a one-to-one mapping, but usually is an underconstrained problem with many degrees of freedom. The different analog circuit synthesis systems that have been explored up till now can essentially be classified in the way how they eliminate these degrees of freedom.

The first class of analog synthesis systems presented in the mid to late eighties were *knowledge-based*. Specific heuristic design knowledge about the circuit topology under design was encoded explicitly in some computer executable form, that was then executed during the synthesis run for a given set of input specifications to obtain the design solution. The knowledge was encoded in different ways in different systems. The IDAC tool [4] used manually derived and prearranged design plans or design scripts to carry out the circuit sizing. The design equations specific for a particular circuit topology had to be derived and the degrees of freedom in the design had to be solved explicitly during the development of the design plan using simplifications and design heuristics. This approach is illustrated schematically in Fig. 1a.

The big advantage of using design plans is their fast execution speed, which allows for fast performance space explorations [1]. The big disadvantages are the lack of flexibility and the large time needed to develop a plan for each topology and design target, as analog design heuristics are very difficult to formalize in a general and context-independent way. It has been reported [5] that the creation of a design script or plan typically takes 4 times more effort than is needed to actually design the circuit once. Considering the large number of circuit schematics in use in industrial practice, this essentially restricted the commercial usability of the tool and limited its capabilities to the initial set of schematics delivered by the tool developer. Also the integration of the tool in a spreadsheet environment under the name PlanFrame did not fundamentally change this [6]. The selection of the topology had to be carried out by the designer himself in IDAC.

OASYS [1] adopted a similar design plan based sizing approach, but explicitly introduced hierarchy in the design of analog circuits and also added a heuristic approach towards topology selection to the system. Hierarchy allowed to reuse design plans of lower-level cells while building up higher-level cell design plans, and therefore also leveraged the number of device-level schematics covered by one top-level topology template. Collecting and ordering all the design knowledge in the design plan however still remained a time-consuming job. The approach was later on adopted in the commercial MIDAS system [5]. Other ways to encode the knowledge have been explored as well, such as in BLADES which is a rule-based system to size analog circuits.

Figure 1. The two basic approaches towards analog circuit synthesis: a) knowledge-based, b) optimization-based.



In order to make analog design systems much more open for new circuit schematics, an alternative solution was sought since the late eighties in using optimization techniques to implicitly solve for the degrees of freedom in analog design while optimizing the performance of the circuit under the given specification constraints. This approach is illustrated schematically in Fig. 1b. At each iteration of the optimization routine, the performance of the circuit has to be evaluated. Depending on which method is used for this, two different subcategories can be distinguished.

In the subcategory of *equation-based optimization approaches* (simplified) analytic design equations are used to describe the circuit performance. In OPASYN [8] and later also CADICS [9] the design equations still had to be derived and ordered by hand, but the degrees of freedom were resolved implicitly by optimization. The tool performed rule-based topology selection. The OPTIMAN program [10,11] added the use of a global simulated annealing algorithm, but also tried to solve two remaining problems. The symbolic simulator ISAAC [12] was developed to automatically generate the (simplified) design equations needed to evaluate the circuit performance and in this way to reduce the introduction time for new circuit schematics. Computer-aided symbolic analysis is now possible for the ac behavior (both linear and weakly nonlinear) of analog circuits up to the complexity of an entire 741 opamp. The symbolic equations can also be used to provide a designer insight into the behavior of an analog circuit. The second problem of ordering the design equations into an application-specific design or evaluation plan was then tackled using constraint programming techniques in the DONALD program [13,14]. Together with a separate topology selection tool based on boundary checking and interval analysis [15], all these tools are now integrated into the AMGIE analog circuit synthesis system from K.U. Leuven [16]. Table 1 shows the results of a recent synthesis experiment for a pulse detector frontend (consisting of a charge-sensitive amplifier and a 4-stage pulse-shaping amplifier). A reduction of the power consumption with a factor of 6 was achieved by the synthesis system compared to the solution generated by an expert designer.

Several other equation-based tools exist as well, such are for instance STAIC [17] and ISAID [18]. An application of this technique to the high-level synthesis of data converters can be found in AZTECA/CATALYST [19] and SDOPT [20], the two tools targeting different types of converters.

Table 1. Example of synthesis experiment.

performance	**specification**	**manual**	**synthesis**
peaking time	< 1.5 µs	1.1 µs	1.1 µs
counting rate	> 200 kHz	200 kHz	294 kHz
noise	< 1000 rms e^-	750 rms e^-	905 rms e^-
gain	20 V/fC	20 V/fC	21 V/fC
output range	> -1..1 V	-1..1 V	-1.5..1.5 V
power	minimal	40 mW	7 mW
area	minimal	0.7 mm^2	0.6 mm^2

A drawback of the equation-based approach is that the design equations still have to be derived, which for certain characteristics such as transient or large-signal responses can be quite tedious to do with sufficient accuracy. Therefore, in recent years and with improving computer power, a second subcategory of approaches has been presented that perform a *full SPICE simulation* run at every iteration of the optimization. For a limited set of parameters this was already possible in DELIGHT.SPICE [21]. However, the challenge was to solve for all degrees of freedom, in case no good initial starting point could be provided. The FRIDGE tool [22] calls the SPICE simulator throughout a simulated annealing optimization loop, and is in this way capable of synthesizing low-level analog circuits (e.g. opamps). The introduction of a new circuit schematic in such an approach is relatively easy, but the drawback are the long run times, especially if the initial search space is large.

An in-between solution was therefore explored in the ASTRX/OBLX tool from CMU [23], where the linear small-signal characteristics are simulated efficiently using AWE [61], whereas equations have to be provided for all other characteristics. ASTRX compiles the initial synthesis specification into an executable cost function whose minimum represents a good solution; OBLX then numerically searches for a good minimum of this function via annealing. For efficiency, the tool also uses a dc-free biasing formulation of the analog design problem, where the dc constraints are solved by relaxation throughout the optimization run. ASTRX/OBLX has been successful in a wide variety of cell-level designs [24]. Other simulation-based approaches can be found in tools such as OAC [25], which is based on redesign starting from a previous design solution stored in the system's database.

Other tools have attempted to integrate the topology selection step as part of the optimization loop. This was done using a mixed optimization formulation with boolean variables representing topological choices [26], or by using a genetic algorithm to find the best topology choice [27,28].

A recent application of the simulation-based optimization approach to the high-level optimization of analog RF receiver frontends was presented in [29]. A dedicated RF front-end simulator was developed and used to calculate the ratio of the wanted signal to all kinds of unwanted signals (noise, distortion, aliasing...) in the frequency band of interest. An optimization loop then determines the optimal specifications for the receiver subblocks such that the desired signal quality for the given application is obtained at the lowest possible power consumption for the overall front-end topology. Behavioral models and power estimators are used to describe the different subblocks at this high level.

In summary, the initial design systems like IDAC were too closed and therefore failed on the market place. The trend towards open analog design systems that allow the designer to easily extend and/or modify the design capabilities of the system without too much software overhead has been evident. The research progress over the last ten years has resulted in the development of several experimental analog synthesis systems, with which several designs have successfully been synthesized, fabricated and measured; this includes not only operational amplifiers but also filters [30] and data converters.

Finally, it has to be added that industrial design practice not only cares for a fully optimized nominal design solution, but also expects high robustness and yield in the light of varying operating conditions (supply voltage or temperature variations) and statistical process tolerances and mismatches. Precautions for this were already hardcoded in the design plans of IDAC [4], but are more difficult to incorporate in optimization-based approaches. The ASTRX/OBLX tool has been extended with these manufacturability considerations [31]; the strategy uses a nonlinear infinite programming formulation to search for the worst-case “corners” at which the evolving circuit should be evaluated for correct performance. The approach has been successful in several test cases but does increase the CPU time required (e.g., by roughly 4X-10X). More work in this direction is clearly needed.

3 Backend: Analog Cell and System Layout

Perhaps unsurprisingly, analog layout is a bit more mature than analog circuit synthesis, in large part because it has been able to leverage mature ideas from digital IC layout. In our review we distinguish two different layout problems: *cell layout*, which transforms a transistor-level schematic with 10-100 devices into a mask layout, and *system assembly*, in which large, basic functional blocks are laid out, and the goal is to floorplan, place, and route them.

3.1 Cell Layout Strategies

The earliest approaches to custom analog cell layout relied on procedural module generation. These approaches are a workable strategy when the analog cells to be laid out are relatively static, *i.e.*, necessary changes in device sizing or biasing result in little need for global alterations in device layout, orientation, reshaping, *etc*. In such instances, a procedural generation scheme which starts with a basic geometric template and completes it by correctly sizing the devices and wires can be quite satisfactory. [32] is an often cited early example. The more recent system at Philips [5] is a good example of practical application of these ideas on complex circuits.

Often, however, changes in circuit design require full custom layout, which can be handled with a *macrocell-style* strategy. The terminology is borrowed from digital floorplanning algorithms, which manipulate flexible layout blocks, arrange them topologically, and then route them. For analog cells, we regard the flexible blocks as devices to be reshaped and reoriented as necessary. Module generation techniques are used to generate the layouts of the individual devices. A placer then arranges these devices, and a router interconnects them—all while attending to the numerous parasitics and couplings to which analog circuits are (unfortunately) sensitive.

ILAC from CSEM was an important first attempt in this style [33]. It borrowed heavily from the best ideas from digital layout: efficient slicing tree floorplanning with flexible blocks, global routing via maze routing, detailed routing via channel routing, area optimization by compaction. The problem with the approach was that it was difficult to extend these primarily-digital algorithms to handle all the low-level geometric optimizations that characterize expert manual design. Instead, ILAC relied on a large, very sophisticated library of device generators.

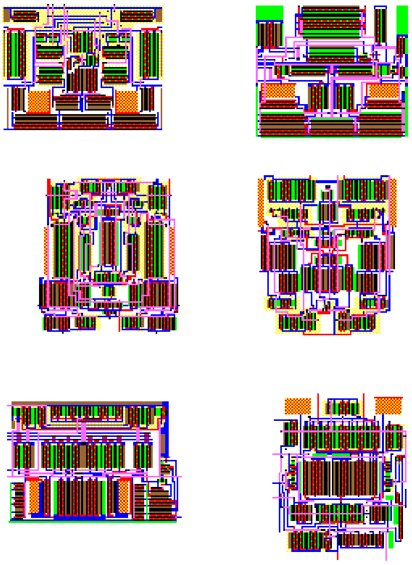
ANAGRAM and its successor KOAN / ANAGRAM II from CMU kept the macrocell style, but reinvented the necessary algorithms from the bottom up, incorporating many manual design optimizations [34,35,36]. For example, the device placer KOAN relied on a very small library of device generators, and migrated important layout optimizations into the placer itself. KOAN could dynamically fold, merge and abut MOS devices, and thus discover desirable optimizations to minimize parasitic capacitance during placement. KOAN was based on an efficient simulated annealing algorithm. Its companion, ANAGRAM II, was a maze-style detailed area router capable of supporting several forms of symmetric differential routing, mechanisms for tagging compatible and incompatible classes of wires (*e.g.*, noisy and sensitive wires), parasitic crosstalk avoidance, and over-the-device routing.

Other device placers and routers operating in the *macrocell-style* have appeared (e.g., [37,38]), confirming its utility. Results from tools using this approach can be quite impressive. For example, Figure 2 (from [36]) shows six analog cell layouts—four manual and two from KOAN/ANAGRAM II. The automatic layouts compare favorably to the manual ones.

In the next generation of cell-level tools, the focus shifted to quantitative optimization of performance goals. For example, KOAN maximized MOS drain-source merging during layout, and ANAGRAM II minimized crosstalk, but without any specific, quantitative performance targets. The routers ROAD [39] and ANAGRAM III [40] use improved cost-based schemes that route instead to minimize the deviation from acceptable parasitic bounds derived from designers or sensitivity analysis. The router in [41] can manage not just parasitic sensitivities, but also basic yield and testability concerns. Similarly, the placer in [42] augments a KOAN-style model with sensitivity analysis so that performance degradations due to layout parasitics can be accurately controlled.

In the newest generation of CMOS analog cell layout tools, the device placement task has been separated into two distinct phases: device *stacking*, followed by *stack placement*. By rendering the circuit as an appropriate graph of connected drains and sources, it is possible to identify natural clusters of MOS devices that ought to be merged—called *stacks*—to minimize parasitic capacitance. [43] gave an exact algorithm to extract all the optimal stacks, and the placer in [44] extends a KOAN-style algorithm to dynamically choose the right stacking and the right placement of each stack. [45] offers another variant of this idea: instead of extracting all the stacks (which can be time-consuming since the underlying algorithm is exponential), this technique extracts one optimal set of stacks very fast. The idea is to use this in the inner loop of a placer to evaluate fast *trial* merges on sets of nearby devices.

Figure 2. ***KOAN/ANAGRAM II Cell Layouts.*** **Six layouts of the identical CMOS opamp are shown. The two middle layouts are automatic, the rest manual.**



The notion of using sensitivity analysis to quantify the impact on final circuit performance of low-level layout decisions (*e.g.*, device merging, symmetric placement / routing, parasitic coupling due to specific proximities, *etc.*) has emerged as the critical glue that links the various approaches being taken for cell level layout and system assembly. Several systems from U.C. Berkeley are notable here. An influential early formulation of the sensitivity analysis problem was [46] which not only quantified layout impacts on circuit performance, but also showed how to use nonlinear programming techniques to map these sensitivities into constraints on various portions of the layout task. In related work, [47] showed how to extract critical constraints on symmetry and matching directly from a device schematic.

One final problem in the macrocell style is the separation of the placement and routing steps. In manual cell layout, there is no effective difference between a rectangle representing a wire and one representing part of a device: they can each be manipulated simultaneously. In a place-then-route strategy, one problem is estimating how much space to leave around each device for the wires. One solution strategy is *analog compaction*, *e.g.*, [48,49], in which we leave extra space during device placement and then compact. A more radical alternative is *simultaneous device place-and-route*. An experimental version of KOAN [50] supported this by iteratively perturbing both the wires and the devices.

We expect to see *macrocell-style* custom cell layout schemes maturing over the next few years. Of course, there are still problems to solve. The wirespace problem remains, though simultaneous place-and-route seems to offer an elegant solution. As we noted in [51] an open problem is “closing the loop” from cell synthesis to cell layout, so that layouts which do not meet specifications can, if necessary, cause actual circuit design changes (via circuit resynthesis). How to control this loop, and how to reflect layout concerns in synthesis and synthesis concerns in layout remain difficult.

3.2 Mixed-Signal System Assembly and Layout

A mixed-signal system is a set of custom analog and digital functional blocks. *Assembly* means floorplanning, placement, global and detailed routing (including the power grid). As well as parasitic sensitivities, the new problem at the chip level is coupling between digital switching noise and sensitive analog circuits.

Just as at the cell level, procedural generation remains a viable alternative for well-understood designs with substantial regularity (*e.g.*, switched capacitor filters [52], or data converters [5]).

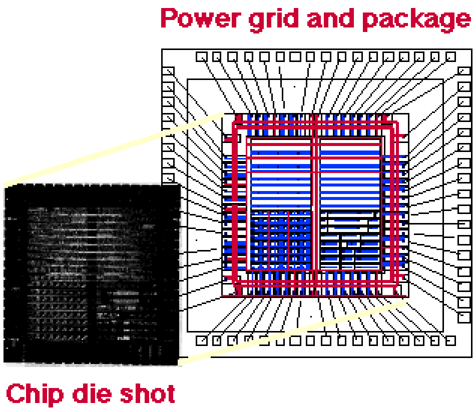
More generally though, work has focussed on custom placement and routing at the block level. For row-based layout, an early elegant solution to the coupling problem was the *segregated channels* idea of [53] to alternate noisy digital and sensitive analog wiring channels in a row-based cell layout. The strategy constrains digital and analog signals never to be in the same channel, and remains a practical solution when the size of the layout is not too large. For large designs, analog channel routers were developed. In [54], it was observed that a well-known digital channel routing algorithm could be easily extended to handle critical analog problems that involve varying wire widths and wire separations needed to isolate interacting signals. Work at Berkeley substantially extended this strategy to handle complex analog symmetries, and the insertion of shields between incompatible signals [55].

The WREN [56] and WRIGHT [57] systems from CMU generalized these ideas to the case of arbitrary layouts of mixed functional blocks. WREN comprises both a mixed-signal global router and channel router. WREN introduced the notion of *SNR-style* (signal-to-noise ratio) constraints for incompatible signals, and both the global and detailed routers strive to comply with designer-specified noise rejection limits on critical signals. WREN incorporates a constraint mapper (influenced by [46]) that transforms input noise rejection constraints from the across-the-whole-chip form used by the global router into the per-channel per-segment form necessary for the channel router (as in [55]). WRIGHT uses a KOAN-style annealer to floorplan the blocks, but with a fast substrate noise coupling evaluator so that a simplified view of substrate noise influences the floorplan. (We should mention here that substrate coupling is an increasingly difficult problem as more and faster digital logic is placed side-by-side with sensitive analog parts. See [58,59] for detailed treatments on substrate coupling.)

Another important task in mixed-signal system layout is power grid design. Digital power grid layout schemes usually focus on connectivity, pad-to-pin ohmic drop, and electromigration effects. But these are only a small subset of the problems in high-performance mixed-signal chips which feature fast-switching digital systems next to sensitive analog parts. The need to mitigate unwanted substrate interactions, the need to handle arbitrary (non-tree) grid topologies, and the need to design for transient effects such as current spikes are serious problems in mixed-signal power grids. The RAIL system from CMU [58,60] addresses these concerns by casting mixed-signal power grid synthesis as a routing problem that uses fast AWE-based [61] linear system evaluation to electrically model the entire power grid, package and substrate during layout. Figure 3. shows an example RAIL redesign of the data channel from [62] in which a demanding set of dc, ac and transient performance constraints were met automatically.

Most of these system layout tools are fairly recent, but because they often rely on mature core algorithms from similar digital layout problems, many have been prototyped both successfully and quickly. Several full, top-to-bottom prototypes have recently emerged (*e.g.* [63,64]). We believe there is still much work to be done to enhance existing constraint mapping strategies and constraint-based layout tools to handle the full range of industrial concerns, and to be practical for practicing designers.

Figure 3. RAIL power grid design for IBM data channel



4 Conclusions

Despite the dearth of commercial offerings, there has been substantial progress on tools for custom analog circuit synthesis and layout over the last decade. Cast mostly in the form of numerical and combinatorial optimization tasks, linked by various forms of sensitivity analysis and constraint mapping, leveraged by ever faster workstations, some of these tools are beginning to show glimmers of practical application. We are not “there” yet, but we are making real progress.

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