PANEL: A COMMON STANDARDS ROADMAP

Chair: Alain Hanover - Viewlogic Systems, Inc., Marlboro, MA
Organizer: Jennifer Smith - Synopsys, Inc., Mountain View, CA

EDA users and suppliers have invested in a number of standards and standards organizations in the past decade; however, the requirements of next generation designs and deep submicron silicon capability call for even more planning and collaboration on standards. This panel will showcase perspectives on the recently published EDA Standards and Technology Roadmap (sponsored by CFI, EDAC, and Sematech) from representatives of high performance semiconductor, academia, international standards, industry consortia, and EDA suppliers.

Every major industry at some point of maturity has had to define and/or redefine a common platform or infrastructure enabling significant sustained growth. The EDA industry and its customers are facing major challenges now with the advent of 0.25µ silicon capability, the need for reusable design content, and multiple EDA systems and tools from different vendors.

The panelists will discuss, among other topics, the critical technologies called for by the roadmap, scope of future versions, implications for the user, and a process for credible adoption by the industry.

Panel Members:

Rich Goldman - Synopsys, Inc., Mountain View, CA
Andy Graham - Cad Framework Initiative, Inc., Austin, TX
Randolph E. Harr - ARPA/ESTO, Arlington, VA
Gregory W. Ledenbach - Sematech, Austin, TX
A. Richard Newton - Univ. of California, Berkeley, CA
Robert Rozeboom - Texas Instruments, Dallas, TX
Kinya Tabuchi - Mitsubishi Electric, Kanagawa, Japan