The SPICE FET Models: Pitfalls and Prospects
(Are you an educated model consumer?)

Daniel Foty
Gilgamesh Associates
Fletcher, Vermont 05444 USA
dfoty@sover.net
http://www.sover.net/~dfoty

Although they are very important for design success, the basic structure of the analytical FET models available in the SPICE circuit simulator have received little attention from the circuit design community. However, a number of factors are forcing a change in this situation. The rapid growth of analog and signal processing applications, along with mixed digital/analog functions on the same integrated circuit, are forcing renewed interest in the details of the FET models. These designs require more stringent model accuracy, and it has been found that FET models which were "good enough" for digital circuit design are inadequate in these new cases. In addition, the increasing use of low power technology has also begun to impose a greater need for accuracy. Finally, with the growth of the fabless design industry, the designers and their fabrication facilities are separated in both the geographic and business senses. It behooves the circuit designer to take a more detailed interest in the models which are provided, as these models serve as the critical communication "vehicle" between a circuit designer and the foundry.

This presentation will review the current "state of the art" of analytical FET modeling in SPICE. The target audience is the *circuit design user* of these models. It is noted that final model quality is influenced by two separate factors: 1) the model equation set, and 2) the quality of parameter extraction for that model; the model formulation represents an "upper limit" of what is possible from each type of model, while parameter extraction determines how close to that "limit" the final model will be. Models currently in use are examined in this light; the focus is on clearly noting the strengths and weaknesses of each model, its applicability for various types of circuit design, and how a circuit designer can determine if the provided models properly represent the underlying fabrication technology and are "the best that they can be" for a given type of model. The overall goal is to help make the circuit designer an "educated model consumer." A circuit designer must work within the available modeling and design "infrastructure" and employ techniques which are available today, rather than wait for potential improvements which may appear in the future.

Various issues in model implementation will also be discussed, with emphasis on the *practical* implementation of FET models for the most effective circuit design. Finally, some of the present problems, directions, and opportunities in analytical FET modeling for circuit simulation will be examined.

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