PANEL: PCB SYNTHESIS - IS THE TECHNOLOGY READY FOR HIGH SPEED DESIGN?

Chair: Gary Smith - Dataquest, San Jose, CA
Organizer: Shelley Boose - Viewlogic, Marlboro, MA

Today's technology imperative demands faster products with greater data bandwidths and an increasing number of complex devices. Responding to these demands while meeting today's time to market pressures limits engineers' tolerance for traditional design processes that depend on an unmanageable number of iterations between design and layout.

A panel of industry experts led by Gary Smith, Senior EDA Analyst from DataQuest, will focus on the changing issues and challenges facing engineers in the design of high speed circuits. Focus areas include:

• Traditional tools for high speed design fall into two categories; one group focuses on the verification process at the end of the design cycle and the other group is limited to a physical layout focus. Implementation of either approach limits the consideration of signal integrity issues to late in the design cycle. The panel will discuss the relationship between tools and design methodologies and the impact on overall design efficiency.

• Timing is the single biggest factor affecting signal integrity. Ten years ago components accounted for up to 80% of the delay in a system.

Today interconnect alone accounts for the majority of the delay. Implementations and drawbacks of various timing solution will be discussed with particular attention to their resulting impact on signal integrity.

• As logical and physical worlds collide, engineers are forced to consider interconnect as an integral part of circuit design. The traditional solution to this problem is to constrain the physical layout of interconnect through overly conservative design practices. Other emerging solutions require the design engineer to become proficient with physical layout software. As many engineering organizations re-evaluate their design tools and methodologies relative to tomorrow's design requirements interconnect design is a critical factor.

Model availability is a significant barrier affecting the implementation of analysis and verification tools. Given the severity of the problem the response from the EDA industry to date has not been sufficient. Today, each company is required to solve the model problem for themselves, often at significant expense. Panel members will discuss modeling solutions and future industry initiatives.

Panel Members:

Robert Gonzales - Omniview, Pittsburgh, PA
Mark Leonard - Compaq Computers, Houston, TX
Fred Saal - Quad Design, Camarillo, CA
John Schoenfeld - Picturetel Corp., Danvers, MA
Jonathan Weis - Interconnectix, Portland, OR
Mike White - Intel Corp., Hillsboro, OR