Package and Interconnect Modeling of the HFA3624, a 2.4GHz RF to IF Converter

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Abstract

This paper demonstrates the use of three-dimensional electromagnetic field solvers to accurately model the interconnect for a 2.4 GHz RF to IF Converter integrated circuit under development at Harris Semiconductor. Lumped element RLC models for the package leads, bondwires, die attach plane, and on-chip interconnect are shown to provide accurate simulation versus measurement and prove the importance of modeling the entire packaged IC.

1 Introduction

As analog circuits operating at RF frequencies are integrated on silicon, the package and interconnect structures become an integral part of the functional design used for matching and tuning networks. At the same time, these structures introduce highly complex parasitic coupling effects. For these reasons accurate modeling of the package and interconnect becomes vital for predicting circuit performance. Yet, these advanced devices are not modeled well with analytical or empirical methods which are based on ideal geometric and/or electromagnetic field assumptions.

In this paper 3-D electromagnetic field solvers are used to accurately model the interconnect for a 2.4 GHz RF to IF Converter integrated circuit under development at Harris Semiconductor. The HFA3624 shown in Figure 1 is a bipolar device that provides up/down conversion between a 2.4 - 2.5 GHz RF signal and 40 - 400 MHz IF operation for wireless communication with the PRISM^{TM} chipset. In particular, we show that modeling the resistance, capacitance, and inductance of the package leads, bondwires, die attach plane, and on-chip interconnect is required for accurate circuit simulation. We also demonstrate the relative importance of each type of interconnect model on simulation results compared with measurement.

The analysis will focus on accurately predicting the gain, |S21|, and return loss, |S11|, as a function of frequency of one section of the converter, the transmit amplifier or TXA. While the simulation focuses on one section of the circuit, the interconnect external to the die will be modeled for the entire device to more fully capture coupling effects associated with the packaging.

The modeling approach taken is to analyze sections of geometry with a 3-D field solver, develop lumped element models, construct an equivalent circuit, and simulate the circuit in Spice. The 3-D

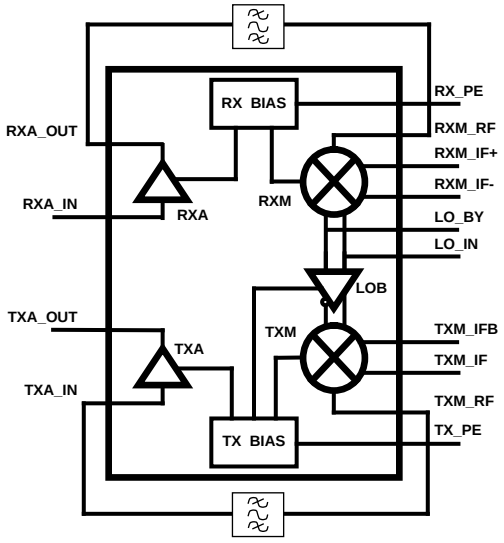

Figure 1: HFA3624 RF/IF Converter Block Diagram

field solvers used were FastCap and FastHenry [2, 4] except where noted. FastCap and FastHenry employ multipole-accelerated Method-of-Moments techniques [1, 3] which require the discretization of only the surfaces of conductors and dielectric interfaces for capacitance extraction, and only the volume of conductors for inductance extraction. The circuit simulation was performed in the Harris Fastrack Design System which employs a modified version of cdsSpice from Cadence Design Systems. All simulations were performed on a scientific workstation.

In the following three sections we investigate the effects of modeling the package leads and bondwires, the on-chip interconnect, and the grounded die attach plane, respectively. The final two sections describe possible modeling improvements with further work and our conclusions.

2 Modeling of the Package and Bondwires

The HFA3624 is packaged in a 28 lead SSOP and the die attach (DA) plane is grounded. The external ground leads of the package are fused to the edges of the DA and the internal ground connections are made by down bonding from bond pads to the DA.

The package capacitance was modeled using MSC/EMAS, a finite element analysis tool from MacNeal-Schwendler Corporation. The model was built by forming a 3-D solid geometry of 1/4 of the package including the metal leadframe and DA, plastic mold compound, PCB, and surrounding air. The geometry was then meshed using 2nd order tetrahedron and a static capacitance matrix was

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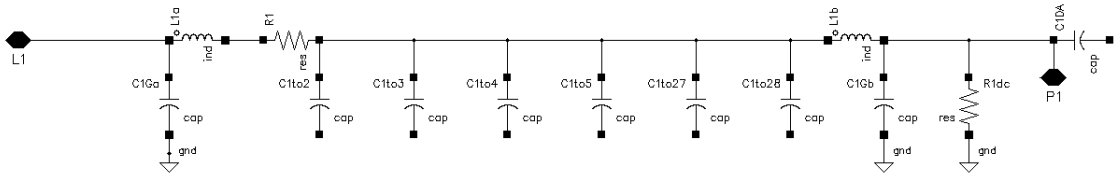

Figure 2: Lumped Element Model of a Single Package Lead

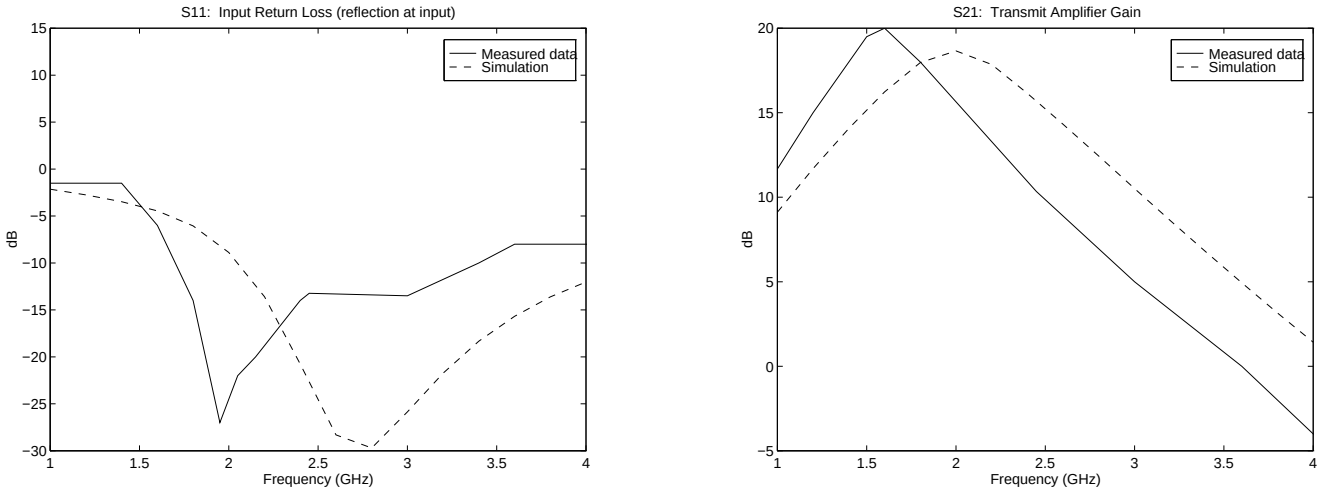

Figure 3: Simulation with Package and Bondwire Models

computed. The system ground plane reference on the PCB was modeled with a perfect-electric-conductor (PEC) boundary condition. The full capacitance matrix was extracted by applying symmetrical boundary conditions along the two planes of symmetry on the 1/4 model and running an even-odd mode analysis. The low frequency package resistance and inductance matrices were computed by discretizing the leads into straight sections of rectangular cross-section which were analyzed in a few minutes using FastHenry.

The equivalent lumped element model in Figure 2 was constructed for each package lead by deriving the circuit parameters from the RLC matrices. The L1 terminal is the external connection to the PCB and the P1 terminal is the internal connection to the bonding post. The capacitance to ground of each lead was divided into the two capacitors, C1Ga and C1Gb. The self inductance was similarly divided between L1a and L1b. The small series resistance was lumped into a single element R1, and a large resistance, R1dc, was provided to allow the lead to be left unconnected with a DC path to ground. The capacitance between the internal end of the lead and the DA was captured in C1DA. The remaining capacitors represent the significant coupling capacitances between the package leads. The mutual inductance was also modeled but is not shown here.

The bondwires were modeled by automatically generating a 3-D filament discretization for FastHenry from the circuit bond diagram using a proprietary Harris Design-For-Packaging tool [5]. Due to the small surface area of the bondwires compared to the separation, capacitance was neglected and a simple network of RL circuits was used for the lumped element model.

At this point all connections to the DA were modeled as a single node. The distributed currents in the DA will be modeled later in Section 4. The simulation results with only package and bondwire models matched poorly to measurement, as shown in Figure 3.

Sweeping the frequency from DC to 10GHz, the inductance values in the package leads are shown in Figure 4 to drop by roughly ten percent due to skin effect. The resistance was also shown to rise considerably however it is still less than one ohm. The off-diagonal resistance, or “mutual” resistance, shown in the figure results from current in a package lead influencing the cross-sectional current distribution of an adjacent lead and thus its resistance. A similar experiment with the bondwires showed an even smaller variance in inductance due to the smaller starting cross-sectional area of the bulk material. In both cases, the original low frequency estimations for the package and bondwire inductances were kept in the model. These values ranged from 1 to 2 nH. The small resistor values were less significant and served more to prevent loops of inductors (voltage sources) in Spice.

To appreciate the influence of inductance in the package leads and bondwires, consider simulation with and without the mutual inductance terms in both models. This is shown in Figure 5. It can be seen that while neither result gives good agreement with measurement at this point, the inductive effects have a strong influence on the waveforms. Interestingly, even though the gain seems to have improved, this is merely coincidental and will be shown to have no correlation later.

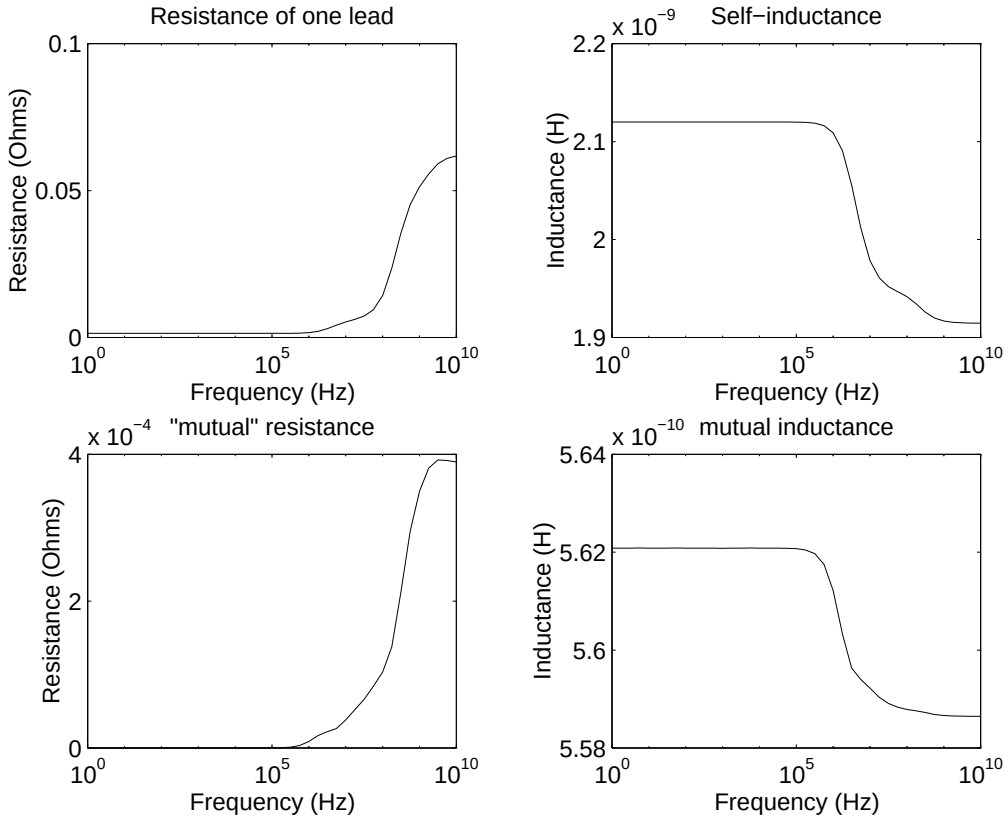

Figure 4: Inductance and Resistance of Package Leads as a Function of Frequency

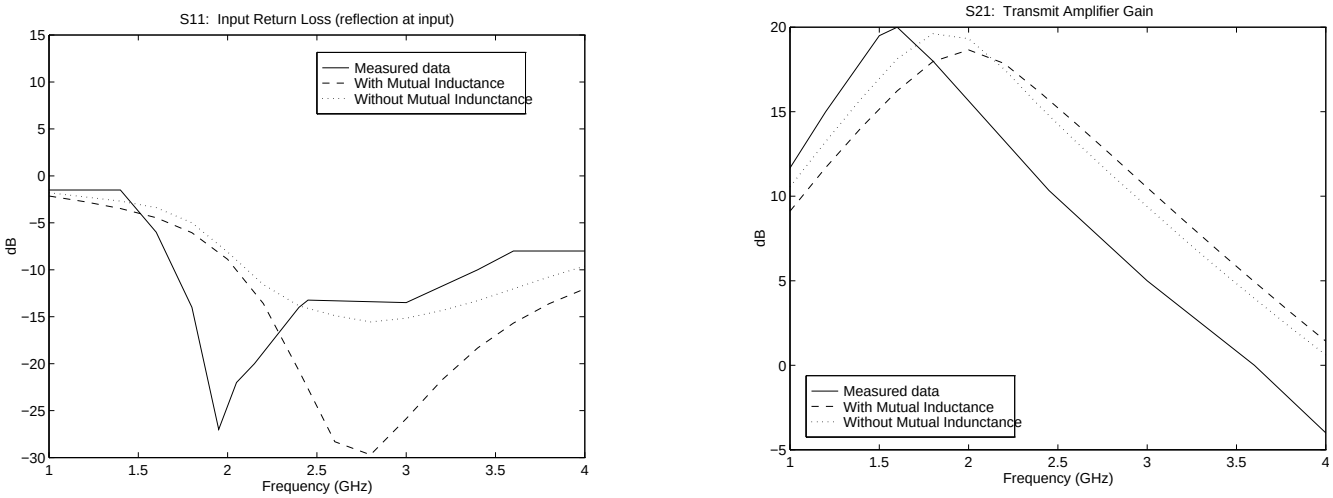

Figure 5: Simulation with Package and Bondwire Models, with and without Mutual Inductance

3 Modeling of the On-Chip Interconnect

As observed from the results of the previous section, it is clear that with only package and bondwire models the simulation is unacceptably far from the measured data. While the final goal is to match the measured data over the whole frequency range, for this product we are especially interested in the results at 2.4 GHz. At this frequency, the predicted gain is 6 dB above the actual gain and the input return loss curve is significantly shifted in frequency. Next we show improvements in the simulation by including models for the on-chip interconnect. The layout of the TXA with the interconnect lines of interest is shown in Figure 6.

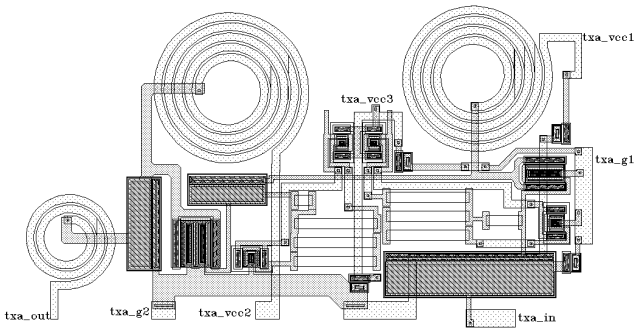

Figure 6: Layout of the TXA

3.1 On-chip Inductance and Resistance

From the influence of the inductance seen in Figure 5, we can expect that the on-chip interconnect inductance will also play a significant role. For instance, while the length of a given segment of on-chip interconnect is considerably shorter than a bondwire, the full path of current can be on the order of the bondwire length and therefore cannot be neglected. To compute the inductance and resistance, the geometries of selected lines were extracted from the layout in a partially automated process and read into FastHenry. In some cases, the interconnect inductance values were found to be as much as ten percent or more of the fabricated spiral inductor values. In addition, coupling ratios for simulating mutual inductance were as high as 50 percent between adjacent lines.

Unlike the package leads and bondwires, the thickness of the on-chip interconnect is still much less than the skin depth in the frequency range of interest. Therefore, a low frequency analysis was used to improve the computational efficiency without loss of accuracy. For this circuit a partial element model with 108 filaments was solved in 3 seconds on a Sparc 20. The lumped elements were added to the circuit schematic and additional nodes were generated for branches in the layout.

The effect on simulation of adding only on-chip RL is shown in Figure 7 by the dotted line. As seen here, adding resistance and inductance models improved the prediction of the gain at 2.4 GHz, but there was no appreciable improvement in the simulated return loss.

3.2 On-chip Capacitance

For capacitance calculation, the fourteen largest sections of interconnect were modeled in FastCap. The capacitance discretization was automatically created from the inductance discretization to produce 8300 panels covering the conductor surfaces and a substrate ground plane. For the process used in this product, it has been shown that in the gigahertz range, the epitaxial layer is too resistive to act as a ground reference for capacitance calculation [6]. For this reason, the doped bulk substrate was used as the ground reference. The capacitances were computed in 768 seconds. The maximum capacitance to ground was 0.17 pF and the maximum coupling capacitance was 0.03 pF.

The effect on simulation of adding capacitance to the on-chip RL model is again shown in Figure 7. The added capacitance greatly improved the prediction of the gain at 2.4 GHz. For the return loss the improvement is still not as drastic. The simulated minimum is approaching the measured data, but the overall S11 curve is still very inaccurate.

4 Modeling of the Die Attach Plane

As mentioned in Section 2, the DA plane was assumed ideal and all ground connections to the plane were shorted together in the Spice model to this point. However, in the partial inductance approach, it

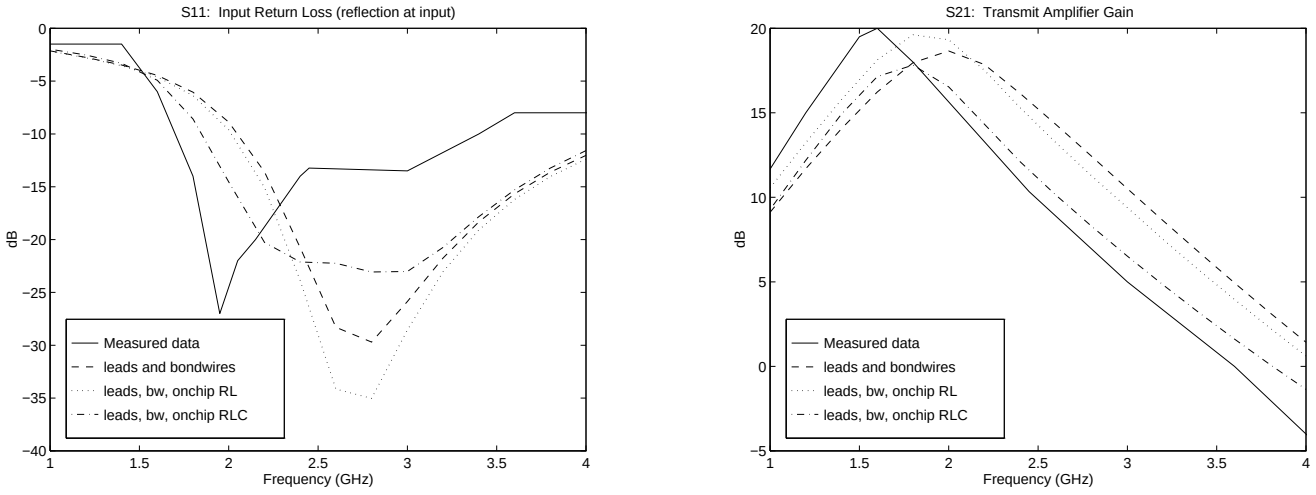

Figure 7: Simulation with Package, Bondwire, and On-chip Interconnect Models

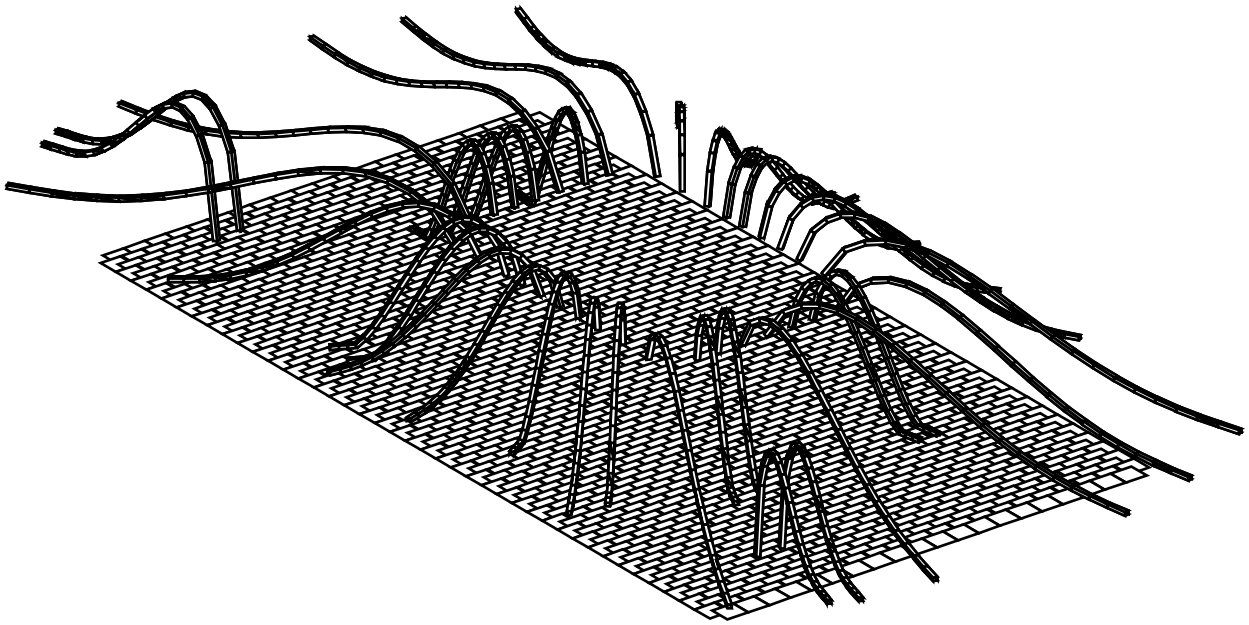

Figure 8: Bondwires with Ground Connections to the DA Plane

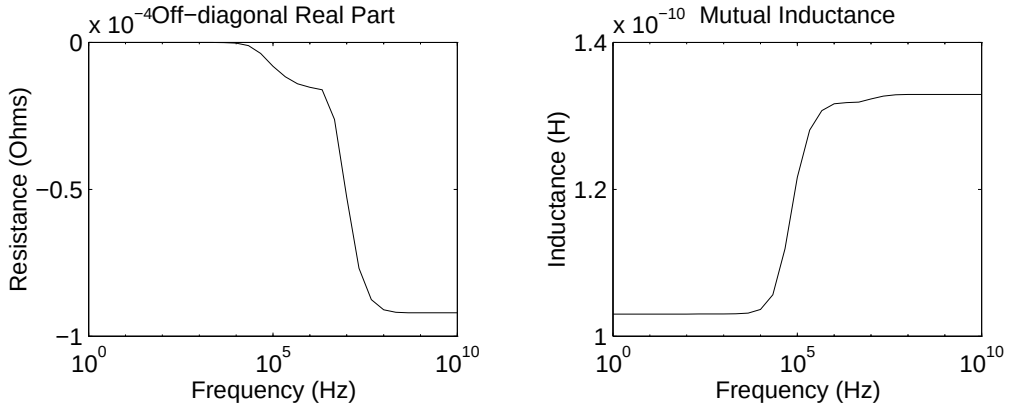

Figure 9: Mutual Inductance and Resistance Between Two Bondwires in Presence of Die Attach Plane

is necessary to model the full path of current flow. Note that even if the plane were perfectly conducting, it would still have inductive effects.

For this reason, a more accurate model for the bondwire current paths and ground connections was implemented by treating the DA as a distributed plane. The plane was discretized into a grid of roughly 4800 partial inductance elements: 800 sections on a 20x40 grid in the x direction, and similarly 800 in the y direction where each section is three partial elements thick to model skin effects. With the bondwires, the total element count was 5746 and the computation completed in 8500 seconds. This solution was for a 35x35 impedance matrix representing a 35-port network of the bondwires and DA at 2.4 GHz. The discretization is shown in Figure 8.

A Spice sub-circuit model was automatically generated from the port model and consisted of inductors, resistors, mutual inductance coupling coefficients, and current-controlled voltage sources for the off-diagonal resistance terms. This model replaced the previous bondwire model used in Section 2.

To gauge the accuracy of the new model, the frequency dependence of the mutual inductance and off-diagonal resistance for a sample pair of bondwires was analyzed, as shown in Figure 9. The leveling off the resistance at 100 MHz indicates the need to change the discretization to capture the skin effect at higher frequencies. However, the inductance appears to have already leveled off at 1 MHz and the resistance is still small, so further modeling of the skin effect would have minimal benefit.

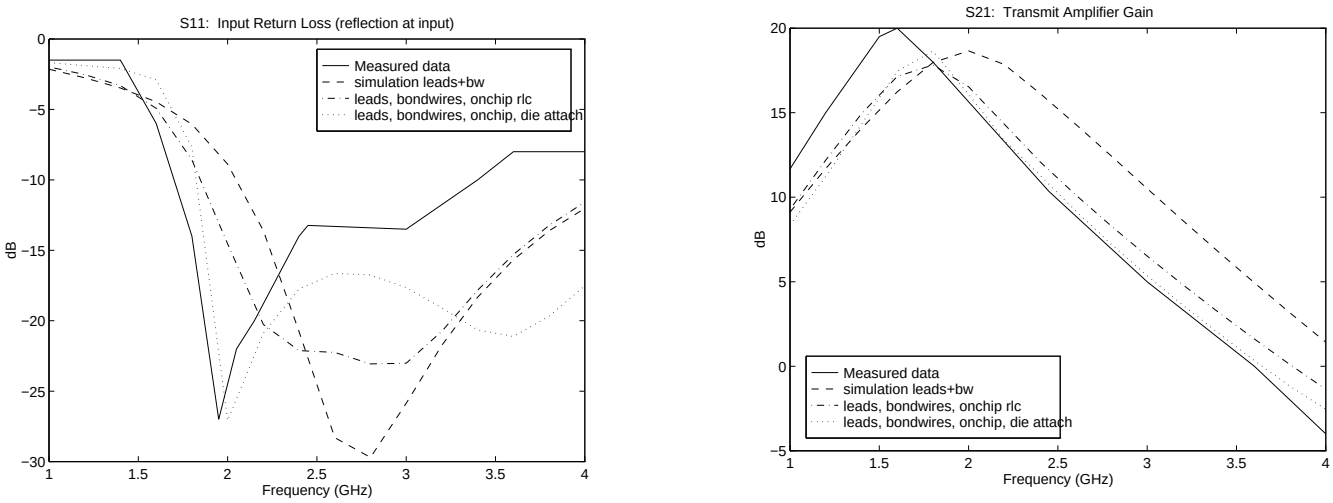

Figure 10: Simulation with Package, Bondwire, On-chip Interconnect, and Die Attach Models

Simulation with the new bondwire model including the DA showed excellent results as seen in Figure 10. The gain matches very closely at 2.4 GHz and the minimum in the return loss occurs at nearly the same frequency as in measurement.

5 Modeling Improvements with Future Work

The above modeling provides an encouraging level of simulation accuracy, however there is room for refinement. The return loss, |S11|, does not match well above 2 GHz and the gain, |S21|, is off below 2 GHz. Some of the discrepancies might result from the fact that the package leads, bondwires plus die attach, and on-chip interconnect models were all built separately. Thus, the coupling between a package lead and a bondwire was not captured.

Not all of the metal traces on the die were included in the model and substrate losses were neglected. Plus, the shrinkage of the width of the traces from etching was not accounted for. This reduction in width from the drawn dimensions is on the order of 2 - 3 microns and results in an underestimation of the inductance and overestimation of the capacitance. These factors can be corrected by improving the level of automation in the extraction of geometry from the layout.

Another issue with the entire circuit is the frequency dependence of the models. We used isolated experiments to try to understand these effects, but a complete analysis is lacking. This is complicated by the fact that the entire circuit does not operate at 2.4 GHz. While these results did not affect the simulation of the TXA, which does operate at 2.4 GHz, when the IF portion is included the constant lumped element model parameter values may become less accurate. If this is true, a means of modeling the parasitic elements over a large frequency range is possible using algorithms for generating reduced order models directly from the quasistatic governing equations [7].

6 Conclusions

Adding lumped element RLC models for the package leads, bondwires, DA plane, and on-chip interconnect provided accurate simulation results for the transmit amplifier of the HFA3624. It shows the importance of modeling the entire packaged IC and the effectiveness of the 3-D field solver codes. In particular the multipole-accelerated method-of-moments capacitance and inductance codes were utilized extensively and proved to be an accurate means for characterizing interconnect.

As a result of this work, Harris Semiconductor has established a comprehensive package and interconnect modeling strategy based on 3-D electromagnetic simulation for all RF product developments. As part of this strategy, the public domain codes FastCap and FastHenry from MIT have been completely integrated into the design flow to provide fully automated extraction of bondwire, die attach, and on-chip interconnect models from layout data.

7 References

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