Panel: Best Ways to use Billions of Devices on a Chip

Moderator:

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Abstract:

We all know that Moore's law is good for at least a few more generations of silicon process, and this will give rise to many integrated circuits having billions of transistors on them. The leading 45 nm processors being announced are getting close to a billion transistors as of 2007. But how can we best use these devices in the future? Integrating more and more features and functions onto SoCs may not be the optimal use for all of these billions of resources. Indeed, to even have a working device at 45, 32, 22 and 16 nm may require new architectures and new structures to be incorporated. Among the many ideas that can be advanced to best use the 'billions and billions served' are:
- multicore and multiprocessor systems
- yet more memory, to hold the embedded software and data required by multiprocessor architectures
- more and more elaborate on-chip interconnect and network structures
- redundant structures for defect tolerance
- structures and architectures for dynamic error recovery
- a variety of schemes to allow lower and lower power and energy consumption

At the same time, billions of transistors on a chip will pose increasing challenges to our design methodologies, integration approaches and design tools. How can we best conceive of, architect, design, integrate, verify and manufacture such devices?

This panel draws on several academic and industry experts who will discuss their views on the best things to integrate into future ICs, and the best ways to do that integration. It will give an excellent opportunity to the audience to challenge and discuss these ideas and to advocate their own views. As well as considering the 'best' ways to use these resources, the panel will also be a good opportunity to discuss the 'worst' ways to proceed. What architectural dead-ends should be avoided as we move through each silicon process generation?

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