NBTI Induced Performance Degradation in Logic and Memory Circuits: How Effectively Can We Approach a Reliability Solution?

Kunhyuk Kang, Saakshi Gangwal, Sang Phill Park, and Kaushik Roy
School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA
Email: {kang18,sgangwal,sppark,kaushik}@purdue.edu

Abstract – This paper evaluates the severity of negative bias temperature instability (NBTI) degradation in two major circuit applications: random logic and memory array. For improved lifetime stability, we propose/select an efficient reliability-aware circuit design methodologies. Simulation results obtained from 65nm PTM node shows that NBTI induced degradation in random logic is considerably lower than that of a single transistor. As a result, simple delay guard-banding can efficiently mitigate the impact of NBTI in random logic. On the other hand, NBTI degradation in memory shows much severe effect especially when combined with the impact of random process variation, NBTI can dramatically reduce the READ stability of memory cells. Hence, aggressive design techniques such as stand-by V_{DD} scaling or adaptive body biasing (ABB) are required in memory application to minimize the impact of NBTI.

I. Introduction

Successful design of digital integrated circuits has often relied on complicated optimization among various design specifications such as silicon area, speed, testability, design effort, and power dissipation. Such traditional design approach inherently assumes that the electrical and physical properties of transistors are deterministic and hence, predictable over the device lifetime. However, with the silicon technology entering the sub-100nm regime, transistors no longer act deterministically over time. One of the most important phenomenon that causes such a change is the temporal reliability degradation in MOSFETs due to the Negative Bias Temperature Instability (NBTI) [1,2].

NBTI is a PMOS specific transistor aging effect which increases the device threshold voltage (V_t) and reduces the carrier mobility (μ) as a function of time and stress condition. A number of experimental analyses [3-7] have shown that NBTI can result from continuous trap generation in Si-SiO_2 interface of transistor. These traps usually originate from Si-H bonds generated after the Hydrogen passivation process to remove dangling Si atoms at the Si-SiO_2 interface [8]. However, under stressed operating condition (i.e., ON-state, negative gate bias under elevated temperature for PMOS), these bonds can easily break with time and generate positive interfacial traps (donor-like state) which contribute to an increase in device V_t.

Physical explanations of NBTI process have been known for decades in the device reliability community. However, it has recently gained attention, mostly due to the wide usage of ultra-thin oxide devices. Specifically, International Technology Road Map for Semiconductor (ITRS) projects oxide thickness of less than 10Å in sub-32nm technology nodes [9]. These thin oxides substantially increases the vertical oxide field (E_{ox}) to the range of few MV/cm, which in turn can result in more severe NBTI degradations and corresponding V_t increase of a transistor [3]. It was also shown that heavily nitrided oxides (mainly employed to alleviate gate leakages) can further expedite the degradation process [39].

The severity of NBTI degradation at the device level calls for an immediate investigation of the problem at the circuit level. However, depending on the specific topology and operating condition, circuit level degradations under NBTI can show a wide variation. In this work, we have thoroughly examined the NBTI induced performance degradation in two major circuit applications: random logic and memory arrays. Based on a quantitative analysis, we determine the severity of NBTI in such circuits, and further propose efficient *reliability-aware design techniques* to potentially mitigate or minimize the impact of NBTI. Compared to the existing works, our proposed methodology considers real benefit of reliability-aware design techniques with respect to the actual design effort and complexity. Our study provides a comprehensive understanding of NBTI degradation in circuits, and further draws a general design guideline for NBTI-tolerant logic and memory design.

We first introduce an analytical NBTI model based on the Reaction Diffusion (RD) framework [2-6] to determine performance degradation in single transistor. We will show how this single device level model can be adopted to higher level simulation model for circuit-level estimation. The model is then applied to evaluate the impact of NBTI degradations in both logic and memory circuits. Simulation results obtained from several ISCAS'85 benchmark circuits designed in 65nm PTM [21] node show that the impact of NBTI in random logic circuit is minimal compared to a single device level degradation. Furthermore, considering the relative magnitude of degradation in random logic, we will show that the effectiveness of complex reliability-aware design techniques such as gate sizing [24,25] and logic synthesis [26] can be easily undermined by simple delay guard-banding at the initial design phase. However, for memory arrays, mismatch among transistors is the critical source of stability problems. Hence, the effect of NBTI is more detrimental. We will show that the impact of NBTI degradation in combination with the random process parameter variation [10] can cause a significant amount of parametric failures in ICs. As a result, memory arrays will require more sophisticated circuit design techniques such as stand-by V_{DD} scaling or adaptive body biasing (ABB) to minimize the impact of NBTI over its lifetime.

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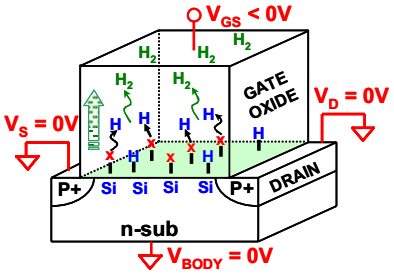

Fig. 1. NBTI degradation process in PMOS transistor based on the RD model.

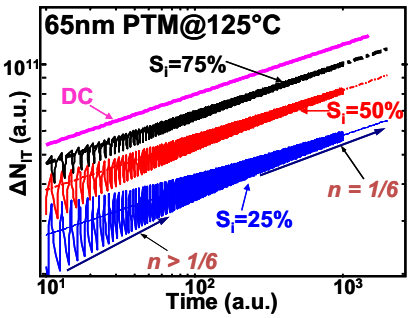

Fig. 2. NBTI degradation under DC and AC stress with various signal probabilities.

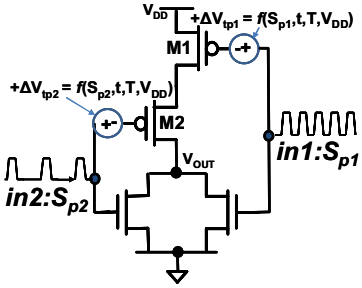

Fig. 3. Circuit simulation model for NBTI degradation in 2 input NOR gate.

The rest of the paper is organized as follows. In section 2, we introduce circuit simulation compatible NBTI models using RD framework. In section 3, we will review and propose reliability-aware circuit design techniques for random logic circuits. Section 4 describes the impact of NBTI degradation in memory arrays and discusses potential solutions. We conclude the paper in section 5.

II. Compact Circuit Simulation Models for NBTI

In this section, we review the temporal V_t model under NBTI degradation using the Reaction Diffusion (RD) framework [2-6]. We will then show how the basic V_t models are adopted for SPICE level circuit simulations.

A. Temporal V_t Model based on RD Framework

NBTI results in a temporal increase of V_t due to the generation of traps at the *Si-SiO*$_2$ interface. In the past decades, numerous experiments [3-7] have empirically shown that increase in V_t due to NBTI under constant DC stress closely follows a power law with respect to time t with a fixed exponent n (i.e., $\Delta V_t \sim t^n$). Time exponent n represents the experimental dependency of the degradation process. On-the-fly based measurement showed that value of n to be close to 1/6 [11,12], whereas n~1/4 for measure-ements with delay [2,5,7].

One of the most promising physical models that explains the phenomena discussed above is the Reaction Diffusion (RD) framework [2-6] (note that there exists other models based on the hole-trapping dynamics [13-15]). The RD based model interprets the degradation process as a consequence of the interaction of inversion layer holes with hydrogen-passivated *Si* atoms as shown in Fig. 1. Under negative gate bias condition, cold holes from the inversion layer can break the *Si-H* bonds, creating interface traps (in donor-like state) and neutral *H* atoms. Neutral *H* atoms can form H_2 molecules, which can diffuse away from the interface (through oxide) or can anneal existing traps. Generated interface trap account for an increase in device V_t as follows,

$$\Delta V_t(t) \simeq \frac{qN_{IT}(t)}{C_{ox}} \simeq f_{AC}(S_p) \times K_{DC} \times t^n \qquad (1)$$

, where N_{IT} is the density of interfacial trap and C_{ox} is the oxide capacitance. K_{DC} is a technology-dependent constant which depends on temperature, V_{DD}, device geometry, oxide nitrogen concentration, etc [2-5]. f_{AC} function represents the AC dependency of the process, which will be discussed in the following context.

Note that in reality, transistors are seldom applied with a constant DC stress. Rather they experience a series of AC stress with varying signal probability (S_p). Here, S_p is defined as the fraction of time when the PMOS is negatively biased. As explained above, during negative bias, PMOS experiences a constant degradation process. However, when the stress is removed (i.e., OFF condition), a reverse annealing process takes place and recovers the device toward the original V_t value. It was experimentally shown [3,5,6,16,17] that NBTI degradation under AC stresses are independent or weakly dependent on operating frequency. Various groups have also shown that AC degradation has similar time exponent (i.e., n~1/6) as the DC degradation. However, absolute magnitude is scaled down by a constant factor which is represented by a signal probability (S_p) dependent function f_{AC} in Eq. (1). AC dependency function f_{AC} can be computed using the same RD framework. Fig. 2 depicts NBTI degradation for AC stress condition with different signal probabilities. As can be observed, due to the recovery process, AC degradation is significantly lower than DC degradation. Later, we will observe that the AC effect leads to lower temporal performance degradation in digital logic circuits.

B. Circuit Simulation Model for NBTI

RD based V_t models have been widely adopted in various circuit-compatible simulations proposed in the literature [18-20]. Most of these models are based on a compact form of Eq. (1) for circuit level simulations. Fig. 3 shows a simple example of a 2-input NOR gate. For given bias condition (V_{DD}), operating time (t), stress temperature (T), and signal probability (S_p), V_t degradation in each PMOS transistor is calibrated (using Eq. (1)) and applied to the gate input as a voltage source. Given this setup, one can apply any type of circuit simulation to obtain delay and power dissipation).

It has been shown that this simple approach can be applied to any existing CAD tools (e.g., SPICE, Static Timing Analysis) with minimum effort while assuring sufficient accuracy [18-20]. However, it also shows some limitations. Since V_t degradation depends on the signal probability (i.e., Fig. 2), signal probability itself can largely affect the overall accuracy. In reality, an accurate estimation of signal probability is a difficult problem, and hence, there is a need to provide certain amount of guard-banding to assure correct functionality using this approach.

III. Reliability-Aware Design Techniques for Random Logic Circuits

In this section, using the RD based compact NBTI model proposed in the previous section, we will first estimate performance degradation in random logic circuits under NBTI. Then in the later part of the section, we will review and present reliability-aware design techniques and compare them with a simple delay guard-banding approach to determine its effectiveness. Finally, we will discuss an alternative design method using on-chip reliability sensor circuit.

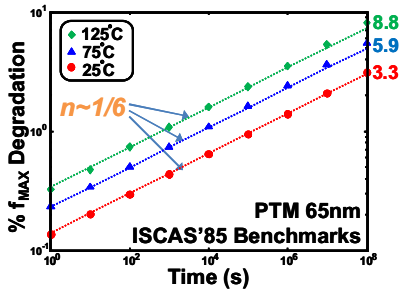

Fig. 4. Average f_{MAX} degradation in ISCAS benchmarks circuits at different temperatures.

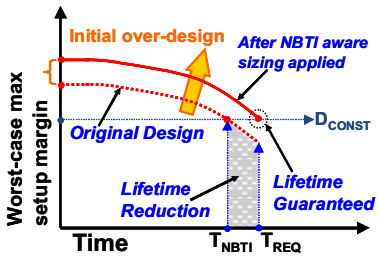

Fig. 5. Reliability-aware gate sizing can guarantee T_{REQ} lifetime [24].

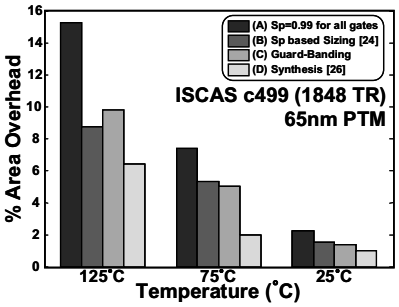

Fig. 6. Comparison between different reliability aware design techniques and simple guard-banding method.

Circuits	# of gates	Nominal Design (um)	Area overhead @125C				Area overhead @75C			
			WC-Sizing	Opt-Sizing	Guardbanding	Synthesis	WC-Sizing	Opt-Sizing	Guardbanding	Synthesis
c432	184	225.7	**8.59**	**6.13**	**7.98**	**4.25**	**5.35**	**4.03**	**4.57**	**1.14**
c1908	466	537.2	**13.79**	**9.17**	**10.21**	**10.38**	**7.62**	**5.72**	**5.70**	**4.40**
c499	534	567.7	**15.25**	**8.75**	**9.81**	**6.45**	**7.39**	**5.34**	**5.04**	**2.02**
c2670	686	801.5	**7.16**	**5.33**	**5.55**	**5.01**	**5.07**	**2.26**	**2.45**	**2.54**
c3540	1134	1392.7	**6.36**	**3.41**	**4.27**	**0.40**	**2.85**	**1.98**	**1.92**	**0.20**
Average			***10.23***	***6.56***	***7.56***	***5.30***	***5.66***	***3.87***	***3.94***	***2.06***

Table 1. Area overhead of reliability-aware sizing, synthesis, and guard-banding (WC: worst-case, Opt: optimal)

A. Performance Degradation in Random Logic Circuits under NBTI

The impact of NBTI in random logic circuits is most evident in its delay degradation. Increased V_t reduces the drive current, hence increases the individual gate delays. In order to estimate the delay degradation in logic circuits, first a standard cell library is characterized considering NBTI degradation. Delay for each cell is then represented in terms of input signal probability, temperature (T), and operation time (t) as follows,

$$Delay = f_D(S_{p1},...,S_{pn},t,T) \quad (2)$$

where S_{pi} represents signal probability at the i'th input.

Once the cell library is obtained, delay degradation in circuits can be computed using standard Static Timing Analysis (STA) tools. Fig. 4 shows the simulation result obtained using STA and NBTI aware standard cell library. Simulation was performed at three different temperature stress of 25°C, 75°C, and 125°C on a set of ISCAS'85 benchmark circuits synthesized using 65nm PTM [21]. Signal probability of 0.5 was assumed at the primary input and properly propagated to each and every node inside the circuit. For each simulation, the average percentage degradation in maximum operating frequency (f_{MAX}) of the nine different benchmark circuits were compared to its initial value (at $t=0$) from 1 sec to 3 years (~10^8 sec). As can be seen, depending on the stress temperature, NBTI can result in an f_{MAX} degradation of up to 8.8% in 3 years (at 125°C). However, as the operating temperature is lowered down to 25°C, the degradation process significantly slows down [3,20] and results in only 3.3% reduction of f_{MAX}. This result suggests that for a realistic estimation of long-term degradation, it is essential to consider the expected temperature profile along the lifetime. Simply applying a constant high temperature might be too pessimistic in most cases.

Aforementioned simulation result also shows that compared to single device level degradation, overall performance degradation in large circuits are relatively small. This is due to the following reasons.

1. NBTI degradation mainly affects the rising transition of CMOS gates. Hence, in normal timing paths where rising and falling transitions occurs consecutively, the impact of NBTI nearly reduces by half.
2. Different gates have different sensitivities with respect to NBTI. NOR type gates with stacked PMOS networks experience more degradation since multiple transistors in the stack simultaneously affects the transition.
3. Due to a wide variation of signal probability at different nodes, overall effect of NBTI is minimal considering a realistic AC input pattern.

This difference will also affect the effectiveness of different logic design techniques under NBTI which we will introduce in the following section.

Also from Fig. 4, it can be observed that the degradation of f_{MAX} retains a power relation with respect to time with a fixed exponent of 1/6, which is identical to the single device degradation shown in Eq. (1). This is unique to NBTI induced performance degradation which has been analytically shown [18] and experimentally validated [22,23] in the literature.

B. Reliability-Aware Circuit Design Techniques

As shown in the previous section, NBTI can slow down the circuit throughout the lifetime, and can possibly result in a timing failure. Numbers of design techniques to handle this problem have been proposed in the literature, some of which are described below:

Gate/TR sizing: One of the first approaches for reliability aware design was based on an optimal gate sizing [24,25]. For example, the method proposed in [24] uses modified Lagranzian Relaxation (LR) algorithm to compute optimal size of each gate under NBTI degradation. The basic idea of this approach is conceptually described in Fig. 5. As can be seen, the setup timing margin of the design reduces with time due to NBTI, and after certain stress period (T_{NBTI}), the design may fail to meet the given timing constraint (D_{CONST}). To avoid such failure, the authors over-designed (transistor up-sizing considering signal probabilities) the circuit to ensure right functionality even after the required product lifetime T_{REQ}. The results from [24] reported an average area overhead of 8.7% for ISCAS benchmark circuits designed in 70nm

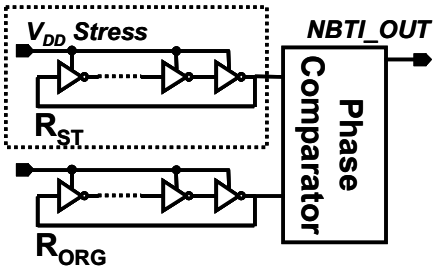

Fig. 7. Reliability sensor circuit using dual ROSC [28].

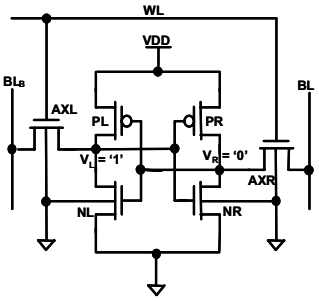

Fig. 8. 6T SRAM cell schematic.

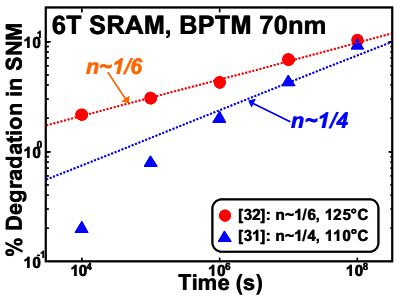

Fig. 9. Degradation in SRAM READ stability under NBTI [31,32].

technology file to ensure 3 year lifetime functionality. An alternative method of transistor-level sizing was also proposed in [25]. In this approach, rather than sizing both the PMOS and NMOS at the same time, the authors applied different sizing factor for each of them. This method could effectively reduce unnecessary slacks in NMOS network (which is not affected by NBTI) and lower the overall area overhead. The results from [25] reported that the average overhead reduced by nearly 40% compared to [24].

Technology mapping & logic synthesis: An alternative method is to consider NBTI at the technology mapping stage of the logic synthesis [26]. This approach is based on the fact that different standard cells have different NBTI sensitivity with respect to their input signal probabilities. With this knowledge, standard cell library is re-characterized with an additional signal probability dependency [19]. During logic synthesis, this new library is applied to properly consider the impact of NBTI degradation. An average of 10% reduction in area overhead compared to the worst case (i.e., not considering the AC dependency of degradation process) logic synthesis was reported using this method.

In order to compare the effectiveness of the aforementioned design methods, we implemented both the sizing and synthesis methods proposed in [24,26] for ISCAS benchmark circuits in PTM 65nm node. A lifetime of 3 years was targeted at 125°C and 75°C temperature respectively, with random AC stress (S_p=0.5) applied at the primary inputs. Table 1 summarizes the simulation results. Sizing algorithm was implemented in two different versions. WC-sizing method in column 4 and 8 represents the worst-case sizing results assuming all nodes in the circuits degrade based on signal probabilities of 0.99. On the other hand, for Opt-sizing (results shown in columns 5 and 9), a realistic estimate of signal probability at each node was obtained from Monte-Carlo simulations [27] and applied during the sizing. As can be observed, the area overheads can be considerably reduced using Opt-sizing approach. Finally, results obtained from the NBTI-aware synthesis are shown in columns 7 and 11.

To better understand the effectiveness of the sizing and the synthesis techniques, we also designed circuits using a simple guard-banding method. Here, during the initial sizing, the delay constraints are tightened with a fixed amount of delay guard-banding. The guard-band is selected as average delay degradations in these circuits for 3 years. Results from section 2.A predicted these values to be 8.8% and 5.9% at 125°C and 75°C, respectively (Fig. 4). Sizing results using guard-banding are shown in columns 6 and 10. Typical result obtained from the c499 circuit is shown in Fig. 6. Interestingly, these results do not show much of a difference compared to that of Opt-sizing (1%@125°C) or the synthesis method (2.06%@125°C). Possible reasons for this negligible difference are,

1. Though guard-banding ignores the sensitivity of individual gates with respect to NBTI, delay degradation is weakly dependent on how the circuits were originally designed. With a well-selected delay constraint, guard-banding indeed produced comparable result.
2. Synthesis method shows slightly better results mostly because logic gates that are less sensitive to NBTI degradations are used/selected. (section 2.A)
3. Delay degradations in non-critical paths do not have impact on sizing. Even with minimum size, these paths will have enough timing margins to avoid failures after NBTI degradation.

Also, note that as the operating temperature is lowered down to 75°C, the difference between guard-banding and other methods further goes down.

These results show that our proposed delay guard-banding technique (during sizing) can be as effective as other existing computationally complex techniques to alleviate NBTI issues in random logic circuits. Nonetheless, note that there still exist extreme situations such as 1) very high operating temperature, 2) very high signal probability, and 3) large numbers of near-critical paths, where more aggressive designs become essential.

C. *Self-correction using on-chip sensor circuits*

In practice, both the sizing and the synthesis methods introduced above require an accurate estimation of NBTI induced performance degradation. This estimation may produce errors due to unpredictable temperature, activity (signal probability), or process parameter variations. One way to handle these problems is to employ an active on-chip reliability sensor [28-30]. For example, a reliability sensor circuit introduced in [28] employs a dual ring oscillator (ROSC) based structure as shown in Fig. 7. One of the ROSC (R_{ST}) is applied with a stressed condition during the operation. The frequency of the degraded R_{ST} is compared with the un-degraded R_{ORG} through phase comparator. Another approach proposed in [29] utilizes the on-chip phase locked loop (PLL) to perform reliability sensing. The unique nature of PLL enables accurate detection of reliability degradation. In these approaches, detected signals (e.g., *NBTI_OUT* in Fig. 6) can be used for further corrective actions. For example, in [29] the detected signal is efficiently transformed into an optimal body-bias signal to avoid possible timing failures in the target circuit. However, it is also essential to consider the additional design overhead (e.g., increased area, power, interconnections, etc.) induced by body biasing and the sensor circuits.

IV. Reliability Analysis and Reliability-Aware design methodology in 6T SRAM arrays

In the previous section, the impact of NBTI degradation in logic

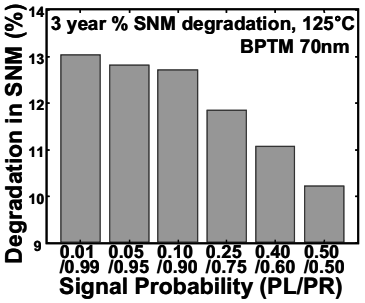

Fig. 10. Degradation in SRAM SNM under unmatched signal probability between PL and PR.

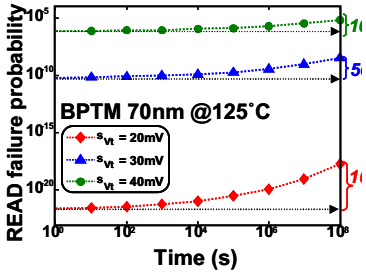

Fig. 11. READ failure probability of SRAM cell under various σ_{Vt}

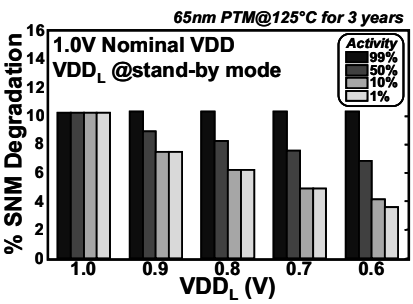

Fig. 12. V_{DD} scaling in SRAM and its impact on cell READ stability degradation under NBTI.

circuits and corresponding reliability-aware design methods were considered. In this section, we will explore the impact of NBTI in basic 6T SRAM type memory arrays and propose efficient design techniques.

A. Impact of NBTI degradation in 6T SRAM cell

Fig. 8 shows the schematic of a basic 6T SRAM cell. In contrast to the logic circuits, parametric failures in memory arrays due to local mismatches among 6 transistors in a cell can lead to failures. As a result, NBTI degradation, which only affects the PMOS transistors (PL and PR in Fig. 8) can have a prominent effect in SRAM parametric failures. For example, in [31,32], it was reported that NBTI induced V_t degradation can severely damage the read stability of an SRAM cell (though WRITE properties are slightly improved). Simulation results obtained for a constant AC stress at a high temperature (110°C and 125°C) show that Static Noise Margin (SNM) [33] of an SRAM cell can reduce by more than 9% in 3 years. Fig. 9 summarizes the results shown in these reports. While the results are based on a V_t model with different time exponents (i.e., n in Eq. (1). 1/4 in [31] and 1/6 in [32]), they commonly show a significant degradation in SNM over time.

Note that the results shown in Fig. 9 are obtained from an identical stress condition applied to PL and PR. In certain cases, signal probabilities at PL and PR can differ from each other. A typical example is a bit cell storing a constant data for a long period of time. Considering the dependency of degradation with respect to signal probability (shown in Fig. 2), in such cases, one PMOS can experience more degradation than the other, which further increases the mismatch. A simulation was performed using the framework proposed in [31,32] to determine the impact of unmatched signal probability between PL and PR. As can be observed from the results shown in Fig. 10, SNM degradation severely increases with unmatched signal probabilities. Nearly 30% increase in SNM reduction was observed when signal probabilities at PL and PR are 0.99 and 0.01, respectively.

In reality, the major portion of transistor mismatches originates from random intra-die variations (e.g., Random Dopant Fluctuation (RDF)) in V_t of each transistor [34]. Several statistical analysis techniques have shown the significance of RDF induced parametric failures in SRAM arrays [34-36]. Under such circumstances, it is more meaningful to observe the impact of NBTI in combination with the random process variation. Simulation methodology proposed in [32] is one of the earliest works which emphasized the combined effect of NBTI and process variation in SRAM cell. They have modeled the transistor V_t as a temporal random variable as follows,

$$\begin{aligned} &V_t = V_{t0}(t_{op}) + \Delta V_t \\ &\Rightarrow \mu_{Vt} = V_{t0}(t_{op}),\ \sigma_{Vt} = \sigma_{\Delta Vt} = \sigma_{NBTI} \end{aligned} \quad (3)$$

where μ_{Vt} and σ_{Vt} represent the mean and the standard deviation (STD) of V_t. Eq. (3) shows that mean V_t depends on the operation time t_{op}, while STD of V_t is fixed with respect to time and is only affected by the RDF. This temporal V_t model was applied to the statistical framework [36] to compute the READ failure probability of an SRAM cell as shown in Fig. 11. As can be observed, NBTI induced temporal degradation severely increases the chance of READ failures in SRAM cell. For example, when the initial σ_{Vt} is 20mV (due to RDF), 3 year NBTI degradation at 125°C can increase the READ failure probability by more than 1000X. Such an increase in READ failure probability can drastically reduce the parametric yield of the memory arrays [35]. This result indicates that the analysis of NBTI in SRAM arrays is to be considered in combination with the impact of random process variation.

The analyses and results introduced in this section clearly show that the impact of NBTI in memory is much more significant compared to that in random logic circuits. Hence, in the following section we will propose efficient design techniques to minimize the NBTI effect in memory arrays.

B. Reliability-Aware Design in Memory Circuits

In contrast to random logic circuits, primary design target in memory array is to minimize the cell area and to improve stability. In this section, we consider the 6-T cell configuration and discuss techniques to improve NBTI related reliability.

Periodic cell flipping: One of the first reliability-aware design methods for memory was proposed by Kumar in [31], known as the cell-flipping technique. This method utilizes the fact that an unbalanced signal probability at a single bit cell can increase the failure probability as shown in the previous section (Fig. 10). Hence, they have designed the memory structure to periodically flip the cell state in order to balance the signal probability at both side of the cell (PL and PR in Fig. 8) and reduce the NBTI-induced cell failures. However, even with this method, there is a significant possibility of memory failures due to NBTI. For example, even when the signal probabilities at PL and PR are matched to 0.5, READ SNM can degrade by more than 10% (Fig. 9 and 10).

Stand-by V_{DD} scaling: Memory cells are often put into a long period of stand-by mode, where cell V_{DD} is reduced from its nominal value to minimize the leakage power consumption. Since NBTI degradation is highly dependent to the vertical oxide field, such V_{DD} scaling can be also very effective in minimizing the impact of NBTI during the stand-by mode. Results shown in Fig. 12 were obtained from a set of HSPICE simulation to show the impact of V_{DD} scaling in SRAM READ stability under NBTI degradation. Nominal V_{DD} is fixed at 1.0V, while stand-by low V_{DD} (VDD_L) is varied from 0.6 to 0.9V. Stability of the cell is measured as the % degradation in READ SNM. Activity factor is defined as the portion of time when the cell is in normal operating mode with

nominal V_{DD}. Results show that as the activity factors gets lower (i.e., more time being spent in stand-by mode), V_{DD} scaling significantly improves the cell stability under NBTI. One advantage of this technique is that it can be easily incorporated to existing memory structures [37] without additional overhead.

Reliability sensing & corrective action: Similar to the methods proposed in section 3.C, on-chip reliability sensors can be used to detect reliability degradation in memory circuit. Based on the detected signals, one can apply corrective actions (e.g., adaptive body biasing (ABB)) to remove potential failures from the memory array.

Based on the above discussions, we compared various memory design techniques for improved NBTI-reliability. We observed that stand-by V_{DD} scaling can be an effective method to minimize the impact of NBTI. However, the effectiveness of V_{DD} scaling largely depends on the activity factor. Hence, for high activity memories, adaptive approaches employing reliability sensor can be a better candidate.

V. Conclusions and Future works

In this paper, we examined the severity of NBTI degradation in two major circuit types: random logic and memory array. It has been widely shown that NBTI induced performance degradation at single device can be very significant. However, our analysis shows that for random logic, corresponding impact at the circuit level is relatively low. Hence, we propose a simple delay guard-banding technique as a design method to mitigate the impact of NBTI in random logic. Comparison with other complex design techniques such as gate sizing and logic synthesis have shown that our proposed method efficiently handles the problem with less complexity and design effort. On the other hand, for memory arrays, we have shown that NBTI in combination with the random sources of process variation can severely degrade the stability of the design. Simulation results showed 1000X degradation in READ stability of an SRAM cell under a severe NBTI degradation. As a result, more aggressive design technique such as stand-by V_{DD} scaling and adaptive body biasing are proposed to improve temporal reliability in memory arrays.

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