Floating-Point Reconfiguration Array Processor for 3D Graphics Physics Engine

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Riding on horseback of SOC (system-on-chip) technology, mobile multimedia has reaped a great deal of success in the market.

Dedicated hardware IPs were regarded as powerful solutions for accelerating speed of applications with low power consumption and small chip size but they begin to reveal limitations due to lack of reusability as digital convergence is now transitioning into a new paradigm. In order to catch both rabbits of performance and reusability, various novel programmable architectures have been proposed and reconfigurable array processors are one of such effective alternatives.

A reconfigurable array processor consists of a reconfigurable array, a context configuration memory and a frame buffer. The reconfigurable array is a 2 dimensional array of PEs (processing elements) and calculates arithmetic operation in a row or column-basis mode. The context configuration memory is a cache memory for storing context layers which control PE arrays by row or column. The frame buffer is a fast memory from which a reconfigurable array read data and to which it write the result.

Reconfigurable array is able to handle multiple data in a SIMD structure so fast with sufficient flexibility that it can be efficiently applied in hardware acieration of unified video/audio CODEC. However, major applications for a reconfigurable array are still based on integer operations but there emerges new applications based on floating-point number operations such as 3D graphics. In the rendering level, research on 3D GPU already achieved a lot so far but in higher level, there still exists so much room for study. Physics engine is one of such areas; it is critical part of game engine since it gives realistic kinetic effects to animated objects. In our experiments, software physics engine occupies more than 90% of total execution time of 3D contents in ARM9 (without FPU) and 3D GPU.

We thus propose novel architecture of reconfigurable array processor which supports both integer and floating-point arithmetic operations. The proposed RA (reconfigurable array) is basically an 8x8 array of integer PEs but it can be also a 4x8 array of floating-point PEs by coupling a pair of integer PEs into a single floating-point PE.

Internal operations of floating-point arithmetic are divided into exponent and mantissa calculations. One PE is used for exponent calculation and the other PE is used for mantissa calculations. Each coupled PEs has linked paths for some interactions such as normalization. The floating-point RA is able to calculate 4-way SIMD FADD/FMUL operations and other functions such as FDIV/FSQRT. Most commercial mobile devices embedding 3D GPU support not only 3D graphics but also video/audio CODECs and so the proposed hybrid structure of RA is actually more efficient in hardware utilization than the one dedicated to floating-point number.

We implemented an RTL model of the proposed RA and perform simulation in RealView™ co-verification environment by executing examples using physics engine. We discovered if the physics engine part is accelerated by RA, the workloads run over 20 times faster than the pure software without FPU and over 4 times faster than the pure software with FPU. If codes are well partitioned and optimized for the proposed RA, which now remains for future study, even more improvement can be expected.

The proposed RA thus proves to be suitable for current design trends of SOCs since it covers not only integer operations but also floating-point operations and so it extends shareable hardware blocks to 3D graphics and enhance reusability of hardware IPs greatly.

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